

Monolithic integration of quantum dot lasers and amplifiers in silicon photonic circuits with high coupling efficiency

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Silicon photonics constitutes the cornerstone technology of on-chip optical interconnects. However, silicon cannot generate or amplify light, and the seamless integration of gain elements with passive waveguides on silicon substrates remains a critical challenge. In this work, we propose a strategy to effectively address the waveguide coupling bottleneck between III/V gain regions and silicon photonic circuits to establish a scalable, monolithic, and CMOS-compatible linked platform. Our approach exploits silicon nitride waveguides deposited at low temperature and coupled through anti-reflective layers to epitaxially grown InAs/GaAs quantum dot gain regions on a silicon wafer. The fabricated junctions exhibited coupling losses below 1.5 dB and back-reflections close to -15 dB for a normal interface. Continuous-wave lasers with distributed Bragg reflectors were experimentally demonstrated with threshold currents below 215 mA at room temperature and a maximum single-port output power exceeding 2 mW. To the best of our knowledge, the first waveguide-coupled monolithically integrated electrically pumped optical amplifiers on silicon substrate are also demonstrated, with net gains greater than 5 dB and a 3 dB optical bandwidth of 46 nm. This advance enables the cost-effective co-integration of positive net gain amplifiers and broadband passive components on silicon, paving the way for next-generation data center interconnects.

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1. INTRODUCTION

The unprecedented growth of global internet traffic has created an urgent demand for interconnect technologies that can sustain ever-higher data rates while minimizing energy and cost burdens. Some of the main drivers behind this data flow jump stem from the evolution in optical communication infrastructure [1], the growth in remote working and the widespread adoption of internet of things (IoT) [2] smart devices. Recently, further impetus has come from growth in the use of generative artificial intelligent (genAI) large language models (LLMs) [3]. Data centers are continuously challenged by big-data applications, driving a relentless advancement of their performance and energy-efficiency metrics. In this context, optical interconnects are pivotal to meeting these demands, harnessing their unparalleled bandwidth capacity [4], minimal energy consumption [5], and ultra-low latency

characteristics [6]. Currently, silicon photonics serves as the foundational platform for on-chip optical interconnects. Leveraging CMOS-compatible manufacturing at ultra-large scales, it supports 300 mm wafers densely integrated with photonic circuitries [7]. However, despite its inherent strengths in passive routing [8] and modulation [9–11], the indirect bandgap of Si prevents its use for electrically pumped amplification and emission [12].

To address the absence of an on-chip light source, stratified group III/V material stacks are integrated onto silicon substrates, creating localized gain regions for laser functionality [13]. This has been widely implemented via the heterogeneous bonding of III/V wafers on larger Si wafers [14] and through the micro-transfer printing (μ TP) of dedicated III/V coupons onto Si substrates [15]. To further boost fabrication yield, monolithic hetero-epitaxial growth of III/V stacks directly on silicon necessitates precise

interface engineering to accommodate lattice and thermal mismatches and minimize defect formation [16]. This mitigation is further enhanced by incorporating quantum-dot layers, whose topology isolates dislocations and thereby protects the active gain region [17]. III/V-based quantum dot lasers on Si have shown remarkable results, with their first practical implementation from Chen *et al.* in Ref. [18] with low threshold current density of 62.5 A cm^{-2} and more than 100 mW output power in continuous wave (CW) operation. Since then, a plethora of demonstrations exhibited convergence to the performance of the III/V lasers on their native substrates [19], achieving output power levels higher than 150 mW [20] and improved thermal tolerance with operation up to 150°C [21].

Nevertheless, the employment of thick micrometer-scale defect filtering and buffer III/V layers complicates the coupling with the standard nanometer-scale passive silicon-on-insulator (SOI) devices. One possible pathway is the growth of the III/V stack inside pre-etched pockets in SOI wafers [22]. Therefore, with appropriate layer thicknesses for both the active and the passive sections, the waveguide alignment with the SOI can be achieved as first demonstrated by Wang *et al.* in Ref. [23]. However, the III/V layers tend to be of poor quality near the pocket sidewalls, while growth on amorphous layers outside the pockets generates polycrystalline material layers. To date, both challenges have been partially overcome by a combination of wet [23–26] and dry etching [24–27], focused ion beam (FIB) milling [23,28] and filling of the etched area with an index-matched polymer layer [25]. This process results in waveguide interfaces that cannot be precisely controlled and ultimately results in several micro-meter wide gaps, affecting significantly the coupling loss and the reflections back to the laser. It must also be noted that growth inside pre-patterned cavities leads to dependencies of the laser response on the size and the shape of the trenches [29,30], hence a thoroughly developed design is of critical importance.

Similarly to the laser, a semiconductor optical amplifier (SOA) is essential for high-density photonic integrated circuits (PICs). The increased number of passive elements and interfaces between different components on-chip causes either poor output power level or imbalances in the signal amplitude profiles for multi-channel applications, such as beam-steering [31] and optical switching [32]; these can be remedied by incorporating SOAs. Furthermore, SOAs can act as booster sections for tunable lasers, enhancing their output power, along with assisting in the fine-tuning of the emitted wavelength. To date, the integration of SOAs on PICs has been accomplished employing methodologies analogous to those utilized for laser integration [33]. Multiple works of bonded III/V quantum well active regions on silicon waveguides for operation in the O- [34] and C- [35,36] frequency bands have demonstrated gain levels greater than 14 dB, saturation output powers up to 2.95 dBm, and large 3 dB optical bandwidths up to 69 nm [36]. Furthermore, the printing of O-band gain coupons on SiN [37] and C-band amplifiers on Si [38] and SiN [39] platforms has been shown, achieving remarkable results with optical bandwidths close to 30 nm [37–39], as high as 23 dB gain and high output saturation power up to 9.64 dBm [38]. However, to the best of our knowledge, the integration of an SOA with a silicon photonic circuit under a monolithic process has not yet been demonstrated, despite stand-alone demonstrations which exploit InAs/InGaAs quantum dot active regions [40].

The integration challenges for a monolithic gain area on silicon outlined above can be mitigated using the coupling strategy

proposed by Skandalos *et al.* as described in Ref. [41] and [42]. Specifically, by introducing plasma-enhanced chemical vapor deposited (PECVD) silicon nitride (SiN) waveguides within pre-etched trenches into the target wafer, it facilitates an efficient butt-coupling with less than 0.5 dB losses and better than -18.7 dB back-reflections. This approach avoids growing the III/V stack onto the passive wafer and instead deposits SiN directly onto the III/V-on-Si wafer. It is noted that the planar III/V-on-Si configuration adopted in this work is not an intermediate step toward pocket growth. The direct III/V epitaxy on Si maximizes the crystalline quality of the gain stack, and it is the preferred implementation whenever the passive circuit is realized in SiN. As discussed in the Discussion Section, the same interposer concept can additionally be applied to III/V stacks grown inside pre-etched SOI pockets, when co-integration with sub-micrometer SOI waveguides is required. Due to its low deposition temperature ($<350^\circ\text{C}$), PECVD SiN does not affect the III/V layers, while its amorphous structure enables a defect-free and thickness adaptive layer with conformal coverage inside the trenches. This ensures interface integrity and wafer-scale uniformity, supporting reliable optical coupling. Moreover, the tunable refractive index of SiN (1.7–2.9), from nitrogen-rich to silicon-rich compositions, enables both improved mode matching with the III/V waveguide and integration of index-matched anti-reflective coatings. Leveraging this technique, Ge/SiGe quantum-confined Stark effect (QCSE) modulators [43] integrated with SiN waveguides on 200 mm Si wafers have been demonstrated with speeds of 100 Gb s^{-1} under sub-dB coupling losses. A robust and low-loss waveguide interface is therefore possible, allowing a two-fold role for the SiN layer. Primarily, it can serve as the main passive platform on a Si substrate. Propagation losses of 1–2 dB/cm in the O-band have been demonstrated for the same NH_3 -free composition in dedicated passive fabrication runs [44], while the waveguides of the integrated chips reported here exhibit $3.04 \pm 1.37 \text{ dB/cm}$, a value attributed to this first, chip-scale iteration of the combined process rather than to a platform limit (see Supplement 1, Section IV). SiN can also act in a synergistic way alongside an SOI layer through evanescent coupling [45]. Hence, complex waveguiding functions can be implemented exploiting the best characteristics of each platform (e.g., temperature insensitive (de)multiplexers in SiN and tight bendings in SOI).

In this work, we introduce and demonstrate a monolithic integration method for InAs/GaAs quantum dot lasers and amplifiers coupled to SiN waveguides on Si substrates. The coupling concept is schematically depicted in Fig. 1 and is implemented on $2 \times 2 \text{ cm}^2$ dies diced from 3 inch Si (001) substrates having a 4° offcut angle to [1–10], as shown in Fig. 2(a). Infra-red (IR) imaging under CW electrical driving confirms efficient light transfer from the III/V laser into the SiN waveguide. A cross-sectional scanning electron microscope (SEM) image of the interface after FIB milling is depicted in Fig. 2(b). It is noted that the FIB was performed only for imaging purposes. The cut direction is indicated with a blue dashed arrow on the top-view SEM image of the laser. A smooth and defect-free junction between the SiN and III/V waveguides is revealed with measured coupling losses as low as 1.45 dB and back-reflection less than -14.8 dB . Both anti-reflective coating (ARC) layers of TEOS (ARC layer 1) and Si-rich SiN (ARC layer 2), the SiO_2/TEOS cladding, the underlying Si substrate, and the laser top/bottom metal pads are resolved. The detailed interface design and the

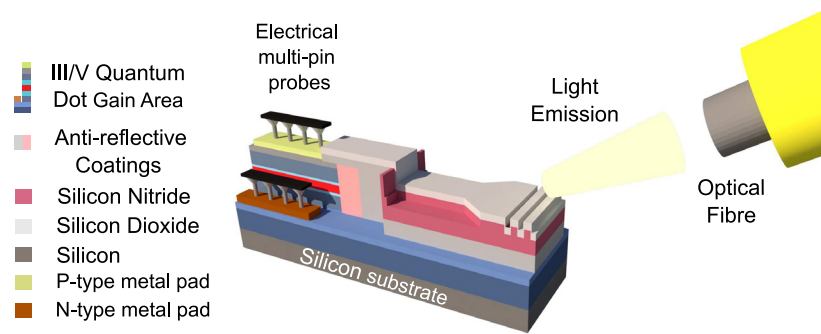


Fig. 1. Monolithic coupling concept between the III/V gain area and the silicon nitride (SiN) waveguide. The III/V gain section is seamlessly emitting light to the SiN waveguide through a low-loss and low-reflection junction, exploiting two anti-reflective coating layers. Optical fibers and grating couplers are utilized for the measurement of the emitted power.

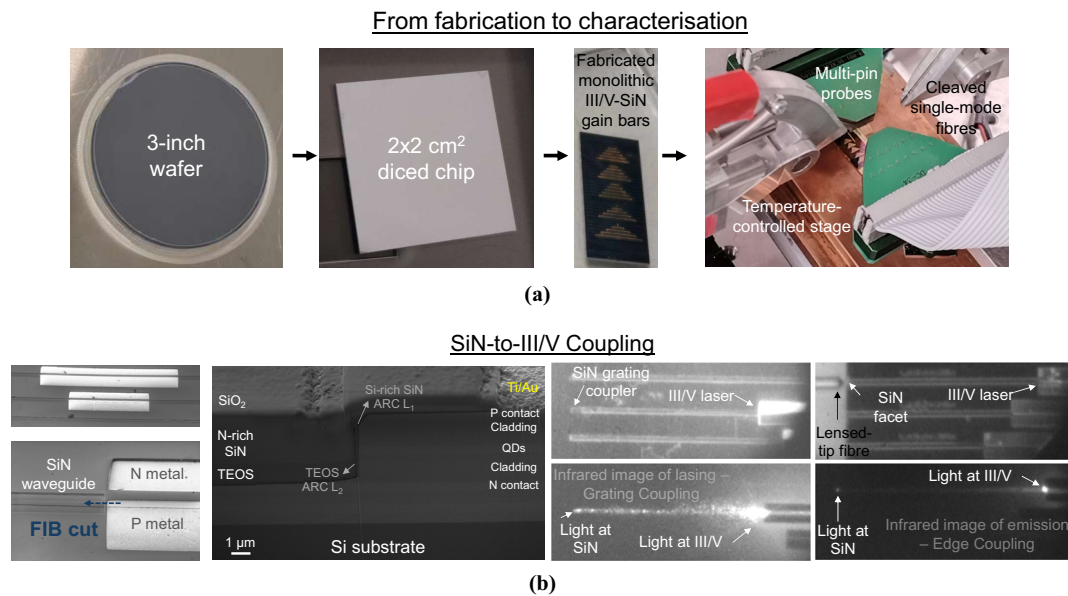


Fig. 2. Integration of the III/V gain sections with the SiN waveguides from fabrication to characterization. (a) A 3-inch Si wafer with the III/V stack was diced in 2×2 cm² chips. The fabrication of the devices was done on chip-scale. Gain bars were characterized electro-optically under continuous wave operation. (b) The interface between the two waveguides was accessed through focused ion beam (FIB) milling and imaged with scanning electron microscopy (SEM). The emitted light spot was captured using a camera with an infra-red (IR) detector.

coupling performance metrics are provided in [Supplement 1](#), Figs. 3–5 and Table 1.

2. RESULTS

A. Laser

The integrated laser was characterized in the O-band by varying the injection current in CW and the temperature of the heat-sink stage on which it was placed. A schematic illustration of the measurement arrangement is shown in Fig. 3(a). The SiN waveguides were designed to achieve an optimized interface (see [Supplement 1](#), Section IV) and interconnection with optical fibers through grating couplers (see Electro-optical Measurements sub-section from [Supplement 1](#), Section III and Section V). Distributed-Bragg reflectors (DBRs) were imprinted on the SiN sections to enhance the intentional reflectivity back to the gain area. Low and high-reflectivity DBRs were implemented at the two output ports of the laser, in order to boost the reflectivity in the cavity through one port and allow the light to escape via the other port. A detailed version of

the integrated laser with geometrical annotations is given through the top-view diagram of [Supplement 1](#), Fig. 7 of Section VI.

The power emitted from the low-reflectivity port is shown in Fig. 3(b) against the injected current density, which is the injected current normalized by the area of a $7 \mu\text{m} \times 3000 \mu\text{m}$ laser. The single-port output power was measured through a SiN grating coupler and a single-mode optical fiber, while it was normalized by the insertion loss of a reference structure containing an identical grating coupler and SiN waveguide section (see [Supplement 1](#), Section V). All laser powers quoted in this work are therefore single-port powers referenced to an on-chip SiN reference waveguide at the laser output. At 25°C, the threshold current density was 1015 A cm^{-2} (213 mA), while the minimum threshold current density achieved was 634 A cm^{-2} (133.25 mA) at the temperature of 15°C. The power at 25°C reached a maximum of 2.08 mW at 1943 A cm^{-2} (408 mA). Lasing is achieved for temperatures up to 35°C. The spectral response of the laser spanning a 15°C–35°C temperature range is shown in Fig. 3(c) for a current 2.5% above the threshold. The degradation of the power level is observed with the temperature increase, alongside a shift of the

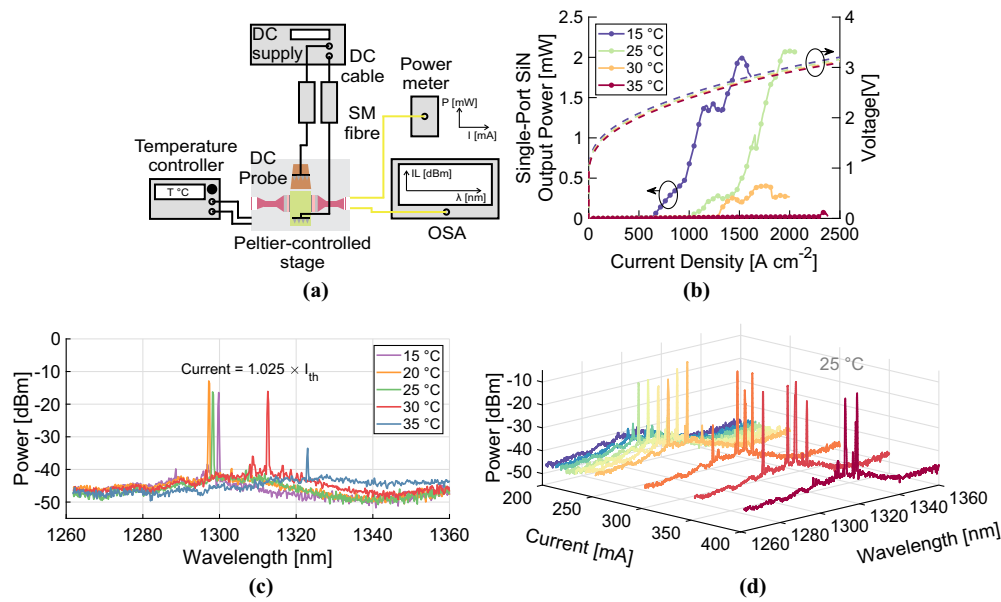


Fig. 3. Characterization of the quantum dot lasers integrated with the silicon nitride waveguides. (a) The measurement system used for the characterization of the lasers. The optical power emitted by a 7 μm wide and 3000 μm long laser is measured by a power meter and is shown in (b) for different CW injection currents and multiple temperatures. The I-V curve of the device is plotted on the same graph. (c) O-band spectra captured by an optical spectrum analyzer (OSA) for different temperatures at an injection current level 2.5% above the threshold. The evolution of the emitted mode with increasing injection current at 25°C is shown in (d). DC, direct current; I_{th} , threshold current; and SM, single-mode fiber.

emitted mode toward longer wavelengths. It is noted that with minimized self-heating under pulsed operation, the device can lase up to 70°C, as shown in Supplement 1, Fig. 9. A three-dimensional (3-D) view of the emitted power at 25°C versus the wavelength and the injection current is plotted in Fig. 3(d). A threshold current of 213 mA can be seen with an emitting mode at the wavelength of 1298.2 nm. As the current increases, more modes appear, based on the mode superposition formed by the multiple waveguide cavities. A fast Fourier transform (FFT) analysis on the amplified spontaneous emission (ASE) spectrum reveals the multiple sub-cavity contribution, as described in Supplement 1, Section VI, Tables 2–3, and Fig. 8.

The step-like features in the L-I curves of Fig. 3(b) correlate with this multi-cavity behavior. Specifically, as the injection current and junction temperature increase, the lasing mode hops between the mode families of the sub-cavities identified in Supplement 1, Section VI, redistributing power among the modes, while the decrease at the highest currents reflects self-heating. Multi-mode operation is not a fundamental property of the architecture. The parasitic sub-cavities are sustained by the residual -14.8 dB reflectivity of the normal III/V–SiN interfaces. When the laser is operated near the threshold, the lasing occurs at a single longitudinal mode matching the DBR wavelength design operation and indicating that the DBR dominated the spectral filtering and mode selection although with a relatively low DBR reflection. Then, as the injection current increases up to 400 mA, the carrier-induced index change and gain band broadening as well as the thermal-induced index change reduced the DBR selectivity, allowing the F-P effect from III/V–SiN interfaces to change the oscillation condition. Thus, we observed the multi-mode lasing spectrum with a mode spacing (over 2 nm) much higher than typical F-P (sub-nm level), which suggests that to be a beating and Vernier effect between multiple cavities, as shown

in the FFT analysis. An angled double-layer anti-reflective coating (DLARC) interface, predicted to maintain reflections below -60 dB across the O-band even in the presence of fabrication variations [Supplement 1, Fig. S4(g)], together with a narrower-band reflector design, is expected to leave the DBR-defined cavity as the only feedback path and thereby enable single-mode operation. A systematic study of narrower ridges and multiple cavity lengths, enabling extraction of the modal gain and internal loss, is the subject of the next fabrication iteration.

B. Amplifier

The amplifiers share the same epitaxial stack and were fabricated in the same flow with the lasers. However, there are no DBR gratings imprinted on the SiN waveguides connected to them and their waveguide geometry is different. A 15 $\mu\text{m} \times 1350 \mu\text{m}$ gain section was selected for the amplifier, as the shorter cavity limits the round-trip amplification of residual interface reflections, suppressing self-lasing, while the wider ridge increases the active volume available for amplification. No amplifier-specific optimization of the epitaxial structure or of the waveguide geometry, such as tilted or tapered gain sections, has been applied at this stage.

The gain of the integrated devices was measured by using the characterization arrangement shown in Fig. 4(a). The die was put on a temperature controlled stage and the current was injected through a DC source. An O-band tunable laser was used in combination with an amplifier to provide the input signal through single-mode fibers to the integrated amplifier via a silicon nitride grating coupler. The polarization of the light was set to transverse electric (TE) through a polarization controller. At the output, another single-mode fiber was used to collect the light, which was fed to a power meter and an optical spectrum analyzer (OSA). The angle of the fibers was tuned in order to align the maxima of the grating coupler response and the gain spectrum of the amplifier. In

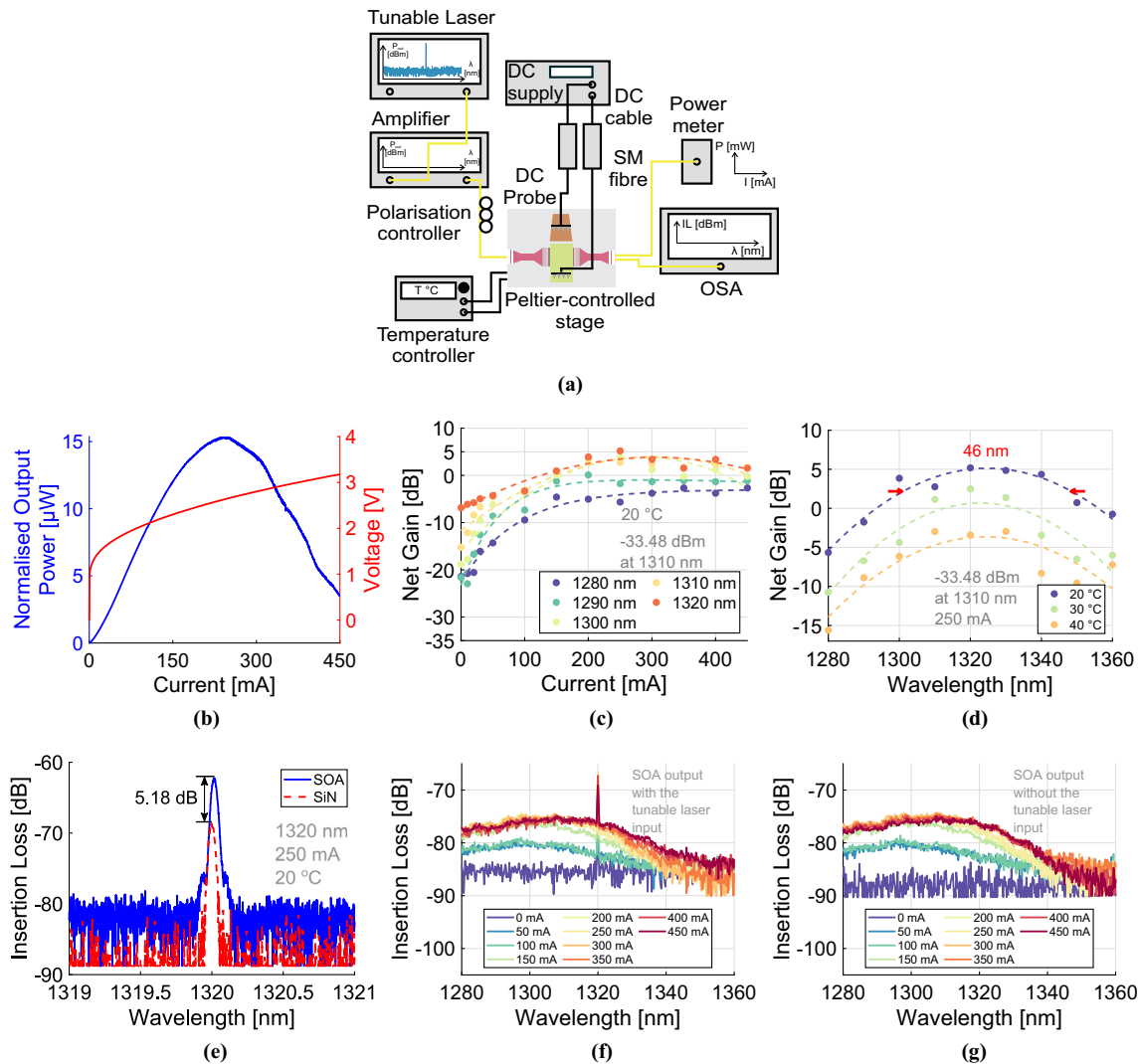


Fig. 4. Characterization of the quantum dot amplifiers integrated with the silicon nitride waveguides. (a) Measurement setup. (b) Output power from the amplifier without any input signal (left axis) and voltage across the device (right axis) against the injected current. (c) The gain of the amplifier against different injection current levels and for different wavelengths at 20°C. The input power at 1310 nm was -33.48 dBm. The gain of the amplifier at 250 mA (d) as a function of the wavelength for different temperatures with a -33.48 dBm input power at 1310 nm. (e) The spectra of the tunable-laser input peak and the corresponding output SOA peak at 1320 nm, 250 mA, and 20°C. In (f) and (g) the output spectrum of the SOA as a function of the injection current is shown with and without the tunable-laser input, respectively, at 1320 nm and 20°C.

Fig. 4(b), the measured output power against the injected current for a $15 \mu\text{m} \times 1350 \mu\text{m}$ device is shown, along with the generated voltage across the device. The output power increased with increasing current reaching its maximum at around 250 mA, showing a roll-off response for currents up to 450 mA. It is noted that this is the normalized power as calculated by using a SiN reference waveguide placed close to the integrated amplifier. At 250 mA, the device dissipates approximately 0.625 W (1235 Acm^{-2} at $\sim 2.5 \text{ V}$, Fig. 4(b)) within a mesa surrounded by thick TEOS blocks and separated from the silicon substrate by the Ge-on-Si virtual substrate and buffer layers. The resulting junction heating enhances the thermal carrier escape from the quantum dots and non-radiative recombination, causing the amplified-spontaneous-emission output to saturate and roll off, consistent with the 35°C ceiling of CW operation.

The net gain against the injected current is plotted in Fig. 4(c). Multiple wavelengths were examined at 20°C and under a small signal input. An increase of the gain with increasing current is

observed with a maximum value around 5.18 dB at 1320 nm, exhibiting convergence and degradation for values above 250 mA. For this value of current, the variation of the gain with wavelength is shown in Fig. 4(d) at different temperatures of 20°C, 30°C, and 40°C. The 3 dB optical bandwidth of the amplifier at 20°C is around 46 nm. With the increase of the temperature the gain was decreased due to non-radiative recombination processes [37], with a maximum value of 5.18 dB at 1320 nm and 20°C, which was degraded to -3.41 dB at 1320 nm and 40°C.

It is worth noting that both the laser and the SOA show a CW operation for temperatures up to around 35°C. The temperature dependence of these devices is primarily attributed to heat dissipation in the III/V gain region rather than to the quantum dot material itself. The III/V regions are surrounded by bulky TEOS blocks, which hinder heat flow around the active area, the thermal path to the silicon substrate is lengthened by the Ge-on-Si virtual substrate and buffer layers and the chip-scale dies were

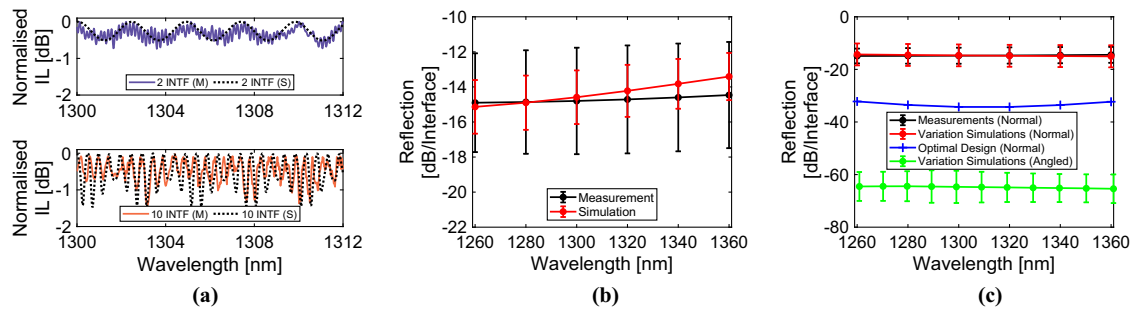


Fig. 5. In (a) the normalized spectral response around 1300 nm for two and ten interfaces is plotted, along with the scattering-matrix circuit simulated and fitted graph. The characterized reflection based on the simulated fit of (a) is plotted in (b), along with propagation simulations. In (c), the measured reflection is compared with the simulated values under an ideal normal design and for geometric and material parameter variations. The simulated reflection under an angled junction is also plotted. The characterized reflection is plotted with black dots, the ideal simulated reflection is plotted with blue crosses, and the simulated normal and angled interface response based on material and geometric variations is plotted with red and green dots, respectively. The dots represent mean values, accompanied by a standard deviation error bar.

probed on a temperature-controlled stage without solder bonding or heat-spreading metallization. Consistently with a thermal rather than material origin, pulsed measurements with minimized self-heating show lasing up to 70°C with a characteristic temperature $T_0 = 51.81$ K in the 20°C–50°C range (Supplement 1, Section VII). This limitation can be mitigated by reducing the TEOS block thickness via an additional etching step, without compromising the optical confinement of the III/V mode, by introducing thermal vias or heat-spreading metal near the mesa, by narrower ridges that reduce the power dissipated at threshold and by modulation co-doping of the quantum dots, which has enabled InAs/GaAs QD lasers operating at heat-sink temperatures above 200°C under pulsed injection [46]. Moreover, temperature variations can alter the optical properties of the DLARC, thereby affecting the coupling efficiency. This effect can be effectively minimized by implementing an angled DLARC interface, which is tolerant to variations in both the optical and geometric parameters of the constituent layers, as shown in Supplement 1, Fig. 4(g). Furthermore, it is noted that the gain of the amplifier was not assessed under high waveguide input power conditions, due to the high insertion loss of the grating coupler (see Supplement 1, Section V).

In Fig. 4(e), the spectra of the tunable-laser input peak and the corresponding output SOA peak are shown for the case of 1320 nm at 250 mA and 20°C. The difference between the peak values is used for the evaluation of the 5.18 dB gain. Moreover, the output spectrum of the SOA is given in Fig. 4(f) and 4(g) as a function of the injection current with and without the tunable-laser input at 1320 nm and 20°C, respectively. The spectrum for both cases shows an optical power increase due to the current injection and a red-shift for currents beyond 250 mA. The only peak that appears is the input peak by the tunable laser at 1320 nm which is amplified by the SOA. When there is no input from the tunable laser, the spectrum consists only of the ASE of the SOA without any self-lasing. It is noted that due to the high insertion losses of the grating coupler and in order to capture the ASE spectrum of the SOA, a resolution of 200 pm was used. To capture the input peak and its amplified version, a resolution of 60 pm was used in a 2 nm neighborhood around 1320 nm. Hence, any discrepancy in the optical power of the spectra in Figs. 4(e), 4(f), and 4(g) is attributed to the different resolutions used. Likewise, the small offset of ~18 pm between the SiN reference waveguide and the SOA output peaks

in Fig. 4(e) is considered as an artifact of the separately acquired traces. Specifically, at the 60 pm resolution used, the wavelength registration between OSA sweeps and the re-setting of the tunable laser between the reference and SOA measurements bound the wavelength repeatability. It is noted that no physical mechanism related to the linewidth enhancement factor of the gain region is assumed to contribute to the shift of the input carrier wavelength in the SOA under small-signal input.

C. Interface Back-Reflection

Because parasitic feedback degrades laser coherence and amplifier stability, the back-reflection of the III/V–SiN interface was quantified, using the same cut-back structures employed for the coupling-loss extraction. The results in Fig. 5, reproduced from Supplement 1, Section IV, constitute a key metric of the platform. The Fabry–Perot fringe contrast of structures containing 2 and 10 interfaces was fitted with a scattering-matrix model [42], yielding a mean interface reflectivity of –14.8 dB with a standard deviation of ± 3.04 dB at 1300 nm and below –14.9 dB across the whole O-band, in agreement with propagation simulations that include the fabricated geometric and material deviations listed in Supplement 1, Table S1. This level falls within the –13 dB feedback tolerance reported for comparable quantum dot lasers integrated with silicon photonics [47]. Propagation simulations of a 7° angled interface, subject to the same fabrication variations, predict reflections maintained below –60 dB across the O-band, as shown in Fig. 5(c), providing a route to feedback-insensitive single-mode operation.

3. DISCUSSION

This work establishes a seamless monolithic integration of III/V gain elements within a silicon-photonics platform. By leveraging low-temperature PECVD SiN deposition to create defect-free layers at micrometer scale, it overcomes active-region quality challenges at trench interfaces. Hence, complications such as the III/V waveguide and layers quality, thickness variations and polycrystalline material formation are mitigated. The proposed technique tackles the waveguide coupling bottleneck achieving as low as 1.45 dB loss per junction, easing the total link budget constraints and enabling the use of complex passive elements. Furthermore, the technique introduced in this study ensures passivation and

Table 1. Performance Comparison of Waveguide-Coupled Lasers on a Silicon Substrate^a

Reference	Integration Method	Platform	λ	CL [dB]	BR [dB]	P_{out} [mW]	I_{th} [mA]	J_{th} [A cm ⁻²]	T_{max} [°C]	W × L [μm]	Laser Type	Interface Type
[23]	Monolithic	InAs/GaAs-QDs-on-SOI	O-band	6.7	–	6.36 (212.5 mA, fiber collimator)	65	722	85	3 × 3000	FP CW	Air (wet etch and FIB)
[24]	Monolithic	GaInAsSb-QWs-on-SiN/Si	2.3	10	–	1.15 (400 mA, Int. Sph.)	135	900	–	10 × 1500	FP CW	Air (wet and dry etch)
[28]	Monolithic	InAs-QDs-on-SiN/SOI	O-band	–	–	5 (500 mA, Int. Sph.)	142	1420	–	5 × 2000	FP CW	Air (FIB)
[27]	Monolithic	InAs-QDs-on-SiN/Si	O-band	29.65	–	0.01 and 10 (Fiber and Int. Sph.)	382	2547	–	5 × 3000	FP CW	Air (dry etch)
[25]	Monolithic	InAs-QDs-on-SiN/SOI	O-band	12.77	–	30.19 (1000 mA, Int. Sph.)	183.33	763.88	105	6 × 4000	FP CW	Air (wet and dry etch)
[25]	Monolithic	InAs-QDs-on-SiN/SOI	O-band	5.4	–	4.4 (800 mA, Fiber)	178.33	1112.5	90	4 × 4000	FP CW	BCB (wet and dry etch)
[25]	Monolithic	InAs-QDs-on-SiN/SOI	O-band	5.4	–	0.0084 (500 mA, Fiber)	~500	~3125	–	4 × 4000	DBR CW	BCB (wet and dry etch)
[25]	Monolithic	InAs-QDs-on-SiN/SOI	O-band	5.4	–	0.012 (300 mA, Fiber)	~300	~1875	40	4 × 4000	Rings and DBR CW	BCB (wet and dry etch)
[26]	Monolithic	InAs-QDs-on-SiN/SOI	O-band	9.07	–	10–16 (1000 mA, Int. Sph.)	205	1140	–	6 × 3000	FP CW	Air (wet and dry etch)
[26]	Monolithic	InAs-QDs-on-SiN/SOI	O-band	9.07	–	–	–	–	–	6 × 3000	Ring CW	Air (wet and dry etch)
This work	Monolithic	InAs/GaAs-QDs-on-SiN/Si	O-band	1.45	<–14.8 (normal) <–60 (angled, S)	2.08 (408 mA, fiber)	213 (90)	1015 (428.6)	35	7 × 3000	DBR CW (pulsed)	Si-rich SiN/TEOS

^aThe output powers are quoted at the reference plane reported by each work (integrating sphere, fiber collimator, and fiber). In this work, the output power is measured through a direct waveguide to single-mode fiber coupling and de-embedded from grating coupler and passive waveguide losses with a reference waveguide. CL, coupling loss; BR, back-reflection; P_{out} , output power; I_{th} , threshold current; J_{th} , threshold current density; T_{max} , maximum working temperature; Int. Sph., integrating sphere; FP, Fabry-Pérot; DBR, distributed Bragg reflector; BCB, benzocyclobutene; CW, continuous wave; and S, simulated.

consistent current distribution across the active region, particularly near interfaces, while simultaneously reducing defect formation that could otherwise lead to facet deterioration and increased back-reflections. Table 1 compares our work with the current state-of-the-art monolithic waveguide-integrated III/V lasers on silicon.

To the best of our knowledge, we have reduced the coupling losses by a factor of more than $\times 3.5$ compared to any other demonstrated work and we showed for the first time < -14.8 dB reflections for a normal interface. This back-reflection can be further reduced and maintained below -60 dB by implementing a 7° angled interface, as discussed in Supplement 1, Section IV and Fig. 4(g). We note, that the table contains only works about lasers as monolithically integrated waveguide-coupled optical amplifiers on silicon have not previously been reported.

These low-loss and low-reflectivity interfaces unlock for the first time the monolithic embedding of gain sections into silicon photonic matrices revealing multifold capabilities. Primarily, they can be used as lasers by exploiting high-gain elements combined with external cavity reflectors and minimized parasitic reflections from the interfaces. Without the use of reflectors, the gain sections can act as amplifying boosters in synergy with lasers, by enhancing their output power level and fine-tuning the emission wavelength. Also, they can reduce signal level imbalances in large photonic layouts, facilitating complex routing passive components, while they can be used as the main elements of gain-controlled optical matrices for switching and beam steering.

Furthermore, the substrate-agnostic property of our method and its adaptivity to a plethora of active stack thicknesses unlock a consolidation of multiple photonic systems on silicon operating at different wavelengths. This capability is boosted by the wide transparency window of silicon nitride ($\sim 0.5\text{--}7\text{ }\mu\text{m}$ [44]) which enables its applicability across a wide spectral domain from the visible to the mid-infrared. Moreover, silicon nitride facilitates evanescent coupling to conventional 220 nm SOI waveguides, effectively bridging the two platforms and enabling hybrid operation. This dual-platform extension is complementary to and does not supersede the planar III/V-on-Si configuration demonstrated here, which remains the preferred implementation when SiN serves as the passive routing layer. Where sub-micrometer SOI circuitry is required, the III/V stack would instead be grown within pre-etched SOI trenches, followed by the integration of our SiN interfaces on the smooth III/V facets. These facets are formed through additional wet and dry etching steps, which remove residual amorphous III/V material and define clean, vertical surfaces, respectively. By positioning these facets away from the SOI trench sidewalls and leveraging the adaptability of our SiN interposers to the shaped III/V gain regions, any material inhomogeneity near the facets is mitigated. Consequently, SiN evanescent couplers can be reliably formed on top of the pre-patterned SOI waveguides. This dual-platform approach allows the exploitation of the distinct advantages of each material system, such as compact waveguide bends via SOI and realizing thermally stable (de)multiplexing through SiN. In addition, this coupling strategy unleashes the fabrication yield capabilities of hetero-epitaxy, due to its feasible deployment on a wide variety of substrate sizes ranging from chip-scale to 200 mm diameter wafers, as demonstrated in this work and in Ref. [43]. We believe that the framework outlined in this paper paves the way for a pilot-line process for fully integrated III/V gain sections on silicon substrates, enabling a cost-effective CMOS electronic-photonic integration on a large scale.

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Data availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

Supplemental document. See Supplement 1 for supporting content.

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