

Demonstration of a Split-Gate Power Amplifier using Four Independent Gates

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Abstract—The split-gate technique allows multi-finger RF devices to have electrically reconfigurable peripheries which can be used to actively change output power while maintaining high-efficiency. Previous work has demonstrated the theoretical concepts using the simplest possible test cell, this work expands the concept using four independent gates which allows a more desirable range of achievable output powers.

I. INTRODUCTION

The split-gate was introduced as a method of dynamically varying the device periphery by independently controlling the DC bias of each sub-gate which allows the output power of signals to be controlled simply while maintaining efficiency, this was initially demonstrated using PAs (power amplifiers) with two independent gates [1] with small-signal measurements only.

Further experimentation was used to verify the load restoration theory using an unmatched device in a passive load-pull system; by maintaining essentially the same optimum load, the efficiency does not significantly change between modes, this was demonstrated when the efficiency moved from 54% to 50.9% for a 4.5 dB output power change [2].

The theoretical implications were explored in detail and complemented with with large-signal measurements of a power amplifier which showed a difference in output power, between modes, of 4.8 – 4.9 dB over a range of input powers while maintaining almost identical efficiency [3].

All research on the split-gate concept up to this point has used two equally sized independent gates which is the simplest case. For the first time, a four-gate device has been fabricated which is expected to have a minimum output power $\frac{1}{16}$ of the fully-on condition [3]. For a practical application desiring this output power range and only two power levels, it would theoretically be sufficient to produce an asymmetrical split-gate, however, by providing access to all four gates independently, a greater range of device behaviour can be examined.

II. PRINCIPLE OF OPERATION

The incident RF signal is divided equally into four DC blocking capacitors which serve to mutually separate the DC biases between gates. Each gate is served with a separate DC feed element and, therefore, each can be controlled independently allowing the use of 1, 2, 3 or 4 active gates. The drain

manifold is identical to that of a normal device and hence only requires a single DC feed.

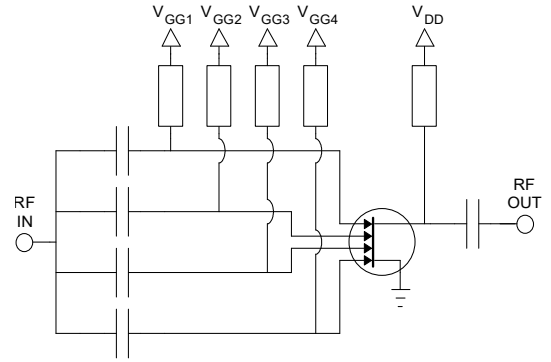


Fig. 1. Conceptual circuit diagram of the four-gate split-gate.

III. IMPLEMENTATION

This paper employs the WIN Semiconductors' NP12-01 GaN-on-SiC technology targeting mm-wave power applications through 50 GHz. This 0.12 μm gate process is manufactured on 50 μm SiC substrates. It uses a source-coupled field plate design to provide the high breakdown voltage required for reliable operation at the drain bias of 28 V, showing a typical saturated output power of 4 W/mm and drain efficiency over 50% at 29 GHz. The NP12-01 platform supports multiple MMIC functions, including optimized switch transistor layouts, two interconnect metal layers, high-reliability MIM capacitors, precision TaN resistors, and through-wafer vias for low inductance grounding.

The conceptual design shown in Fig. 1 was implemented in the NP12 process as shown in Fig. 2.

Observing Fig. 2, the input divider uses a branching configuration which ensures the phases of incident signals are identical at the 5.7 pF DC blocking capacitors. Similarly, the proceeding connections are meandered to preserve phase. The lengths were designed using electromagnetic simulations in Keysight Advanced Design Systems.

It is geometrically impossible to route four gate feeds without overlap hence two air bridges have been used to feed the inner gates. It should be noted that air bridges would not be required in an asymmetrical design (for example connecting three adjacent gates creates a 1:3 split-gate) and are generally

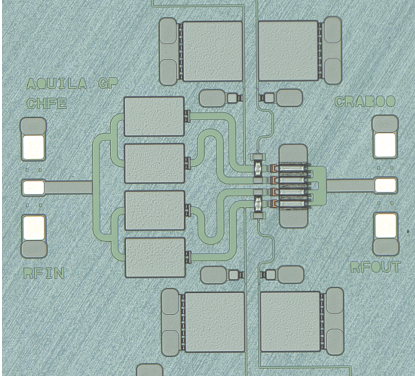


Fig. 2. Photograph of the four-gate split-gate die (size $1.3 \times 1.4 \text{ mm}^2$).

undesirable as they increase the risk of coupling between gate feeds which is a potential cause of instability.

Thin-film resistors of 12.9Ω were placed in series with the gate connections to increase in-band stability.

The out-of-band stability was achieved with 0.1 pF for higher frequencies and larger 8.7 pF capacitors targeted towards lower frequencies.

Off-chip decoupling was achieved with hybrid 100 pF MIM (metal-insulator-metal) capacitors which were connected using wirebonds and $4.7 \mu\text{F}$ electrolytic capacitors which were soldered to the DC launchers.

IV. DCIV TESTING

In the ideal case, all transistor fingers equally contribute to the output power. In practice, scaling deviates and requires complex modelling or simulation [4]. Thermal imaging of RF devices proved uniform device geometries show non-uniform current [5].

Employing a pulsed source in DCIV measurements instead of continuous DC can be used to examine how the device would behave without heating effects [6].

The DCIV characteristics were measured using constant excitation (using a Keysight B1500A) and pulsed excitation (using an Auriga pulsed system). The gate bias was swept from -3.6 V to $+1 \text{ V}$ in 0.2 V increments.

The DCIV characteristic for one active gate is shown in Fig. 3 which shows a 10 mA difference between CW and pulsed.

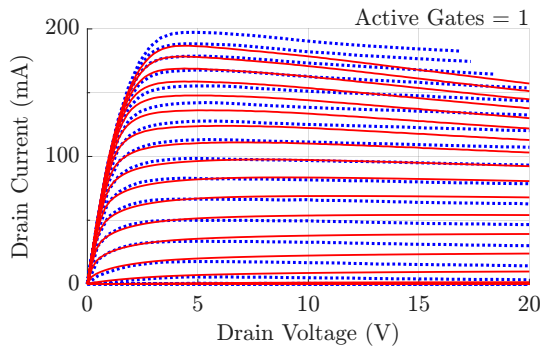


Fig. 3. Continuous DC (solid red) and pulsed (dotted blue) DCIV characteristic of the four-gate split-gate device with one active gate (low power mode).

The two-active gates condition (Fig. 4) shows a difference of approximately 39 mA between the CW and pulsed cases.

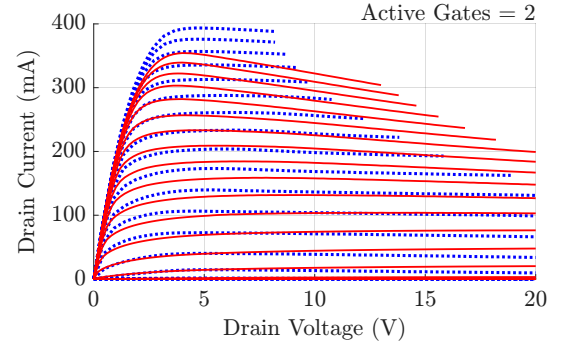


Fig. 4. Continuous DC (solid red) and pulsed (dotted blue) DCIV characteristic of the four-gate split-gate device with two active gates.

The three-active gates condition (Fig. 5) shows a difference of approximately 54 mA between the CW and pulsed cases.

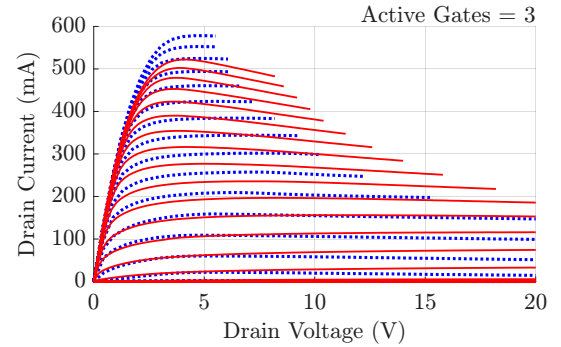


Fig. 5. Continuous DC (solid red) and pulsed (dotted blue) DCIV characteristic of the four-gate split-gate device with three active gates.

The four-active gates condition (Fig. 6) shows a difference of approximately 97 mA between the CW and pulsed cases.

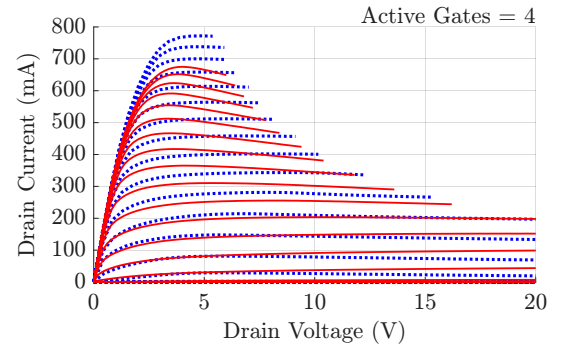


Fig. 6. Continuous DC (solid red) and pulsed (dotted blue) DCIV characteristic of the four-gate split-gate device with four active gates (full power mode).

Evidentially the scaling of the pulsed DCIV characteristics is essentially linear with the number of active gates which matches the ideal case; conversely, as more gates become

active, the continuous DCIV shows a progressively lower peak drain current compared to the ideal case.

As stated above, using ideal current reduction conditions, the power reduction factor [3] is expected to be around 6% (Eq. 1), taking the peak currents under continuous excitation from the measured DCIV characteristics (Figs. 3, 6), the predicted power reduction factor is around 8% (Eq. 2) which equates to an 11 dB reduction.

$$\frac{P_{OUT,MAX,\phi}}{P_{OUT,MAX,F}} = \phi^2 = \left(\frac{1}{4}\right)^2 = 6.25\% \quad (1)$$

$$\frac{P_{OUT,MAX,\phi}}{P_{OUT,MAX,F}} = \phi^2 = \left(\frac{186.8}{675.1}\right)^2 \approx 7.66\% \quad (2)$$

V. LARGE-SIGNAL MEASUREMENTS

The large-signal measurement system used to characterise the split-gate (see Fig. 7) is a source-load-pull, based on a vector network analyzer (67 GHz PNA-X from Keysight). The "Delta" tuners from Focus Microwave are directly connected to the probes, minimizing insertion loss and enabling the measurements at high reflection coefficients ($|\Gamma|$ values up to 0.85). For this measurement, a fundamental-only load-pull was conducted, with harmonics and source impedances terminated at the system impedance (50Ω) by the tuner.

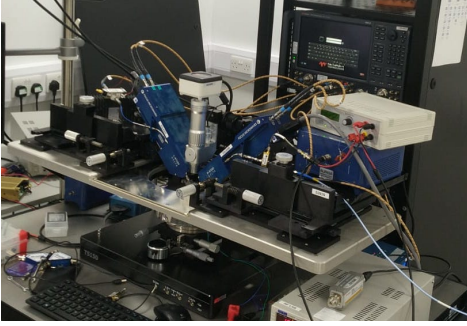


Fig. 7. Photograph of the source-load-pull system.

Loadpull measurements were conducted using a variety of bias conditions and fitted using third-order polynomials, only the optimum loads are shown for brevity.

Switching only the drain bias, (i.e. envelope tracking) results in a trajectory in Fig. 8 which moves over a relatively large area of the Smith chart.

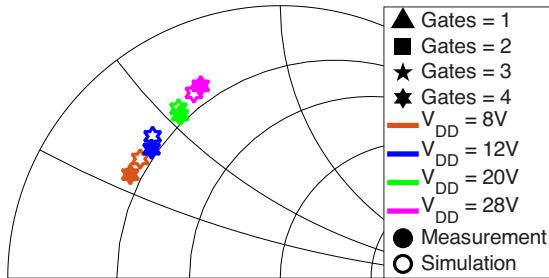


Fig. 8. Optimum load trajectory while only switching drain bias.

Reducing only the number of active gates results in the optimum increasing in magnitude, becoming increasingly reflective which corresponds to the low efficiency loadlines [7].

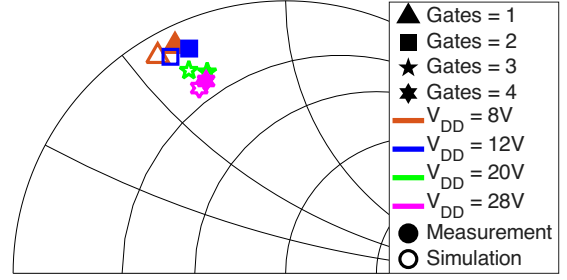


Fig. 9. Optimum load trajectory while only switching the number of active gates.

Finally, switching both the number of active gates and the drain bias results in a trajectory which is less reflective than the case of gates-only and confined to a narrower area than the drain bias-only case.

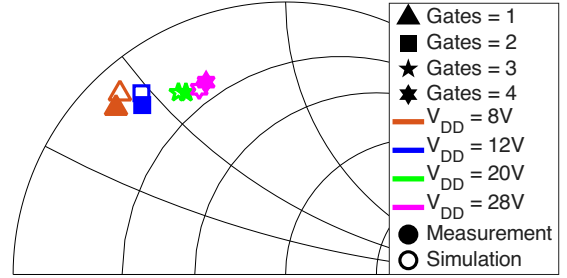


Fig. 10. Optimum load trajectory while switching both the number of active gates and the drain bias.

The 4 active gate 28 V optimum ($10 + j31 \Omega$) was chosen as the impedance for power sweep measurements.

The output power is given in Fig. 11. Interestingly, the difference between the 1 and 2 active gate cases is 4.5 dB, between 2 and 3 active gates it is 4.7 dB and, finally between 3 and 4 active gates it is only 1.8 dB.

The total power switching is therefore 11 dB which matches the predicted power reduction factor given in section IV.

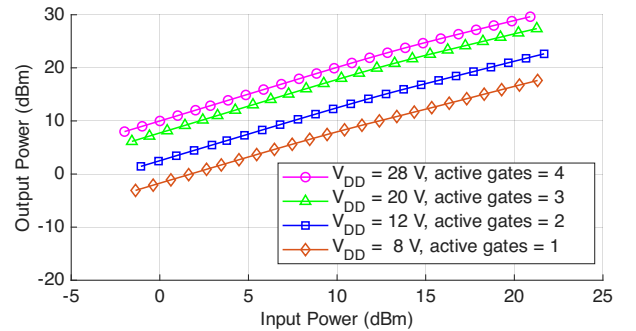


Fig. 11. Output power with respect to input power at $10 + j31 \Omega$.

The drain efficiency is given in Fig. 12; unfortunately the efficiency restoration seen in previous work has not been achieved. The efficiency curves for the 3 and 4 active gate cases are close together and the 1 and 2 active gate cases are spaced further apart which matches the loadpull results in Fig. 10. The disparity between predicted and measured optimum loads would seem to explain the lower efficiency for these conditions.

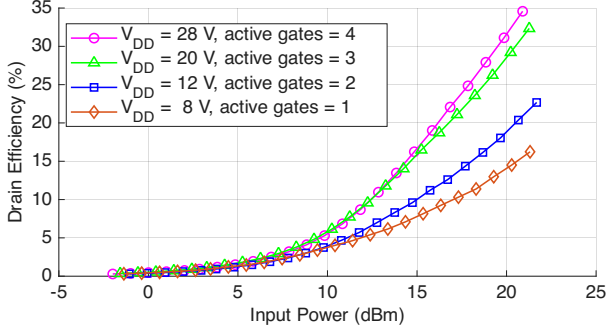


Fig. 12. Drain efficiency with respect to input power at $10 + j31 \Omega$.

Finally the gain is shown in Fig. 13, the 1 active gate case has degenerated into an attenuating mode which would be unacceptable as an output device but may be tolerable as an intermediate gain stage.

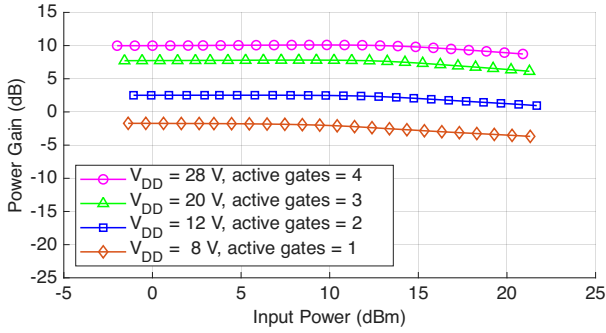


Fig. 13. Power Gain with respect to input power at $10 + j31 \Omega$.

VI. CONCLUSION

The split-gate concept, previously only evaluated using two independent, symmetrical gates has been implemented using four independent, symmetrical gates.

DCIV measurements have been used to predict the power reduction factor of the fabricated device and pulsed measurements have been used for comparison with the ideal case.

Large-signal measurements have been conducted on the new four-gate device using a passive load-pull system which matched the predicted power reduction factor however the expected efficiency was not reached.

Further work is required to measure the devices in heavier compression and to better understand the parasitic effects introduced by the inactive devices which could be used to

derive some form of dynamic compensation for the increasing number of inactive devices.

Using four independent gates provides great flexibility of operation, enabling detailed analysis of the split-gate; for implementation in a practical application such as an adaptive communications system, two power modes would probably be acceptable. Achieving the expected 11 dB output power range in a two-level split-gate device could be performed by merging three of the independent gates together to form an asymmetrical 1:3 split-gate although some form of capacitance compensation is needed to maintain acceptable efficiency.

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