

**DESIGN, CHARACTERIZATION AND REALIZATION
OF THIN FILM PACKAGING FOR BOTH
BROADBAND AND HIGH POWER APPLICATIONS**

A thesis submitted to the University of Wales, Cardiff

In candidature for the degree of

Doctor of Philosophy

By

Zaid Emmanuel Aboush

Division of Electronics

School of Engineering

Cardiff University

United Kingdom

September 2007

UMI Number: U584995

All rights reserved

INFORMATION TO ALL USERS

The quality of this reproduction is dependent upon the quality of the copy submitted.

In the unlikely event that the author did not send a complete manuscript and there are missing pages, these will be noted. Also, if material had to be removed, a note will indicate the deletion.



UMI U584995

Published by ProQuest LLC 2013. Copyright in the Dissertation held by the Author.
Microform Edition © ProQuest LLC.

All rights reserved. This work is protected against
unauthorized copying under Title 17, United States Code.



ProQuest LLC
789 East Eisenhower Parkway
P.O. Box 1346
Ann Arbor, MI 48106-1346

DECLARATION

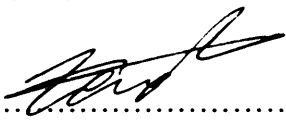
This work has not previously been accepted in substance for any degree and is not concurrently submitted in candidature for any degree.

Signed  (Candidate)

Date 21/9/2007

STATEMENT 1

This thesis is being submitted in partial fulfilment of the requirements for the degree of PhD.

Signed  (Candidate)

Date 21/9/2007

STATEMENT 2

This thesis is the result of my own independent work/investigation, except where otherwise stated. Other sources are acknowledged by explicit references.

Signed  (Candidate)

Date 21/9/2007

STATEMENT 3

I hereby give consent for my thesis, if accepted, to be available for photocopying and for inter-library loan, and for the title and summary to be made available to outside organisations.

Signed  (Candidate)

Date 21/9/2007

To my Parents
Alia and Emmanuel

ABSTRACT

In recent years, high frequency MMICs have witnessed rapid development in terms of miniaturization, higher powers and increasing functionality, whilst the cost per unit has been simultaneously reduced. Cost-wise, modern packages have been unable to follow the same trend as the reduction seen in semiconductor costs and in some cases the package cost has even become a significant part of the overall module cost.

Historically, the diverse range of MMIC applications has always demanded electrically transparent packages to house the on-chip circuits and isolate them from the hostile ambient environment. The other vital role for MMIC packages is to provide good thermal dissipation for the circuits they contain. Thermal issues associated with most packages have led to the invention of different kinds of thermal pastes and strips to help dissipate the excessive heat generated by active devices. However, the thermal design of the package itself remains the basic foundation for a package with good thermal behaviour.

To evaluate the performance of high frequency semiconductor packaging a number of different electrical and thermal measurement setups have been developed. Passive electrical measurements are the most common and easiest measurements to perform as the package is tested without an active device inside. Active measurements involve measuring the package with an active device inside and can become problematic, especially when characterizing high power transistors with low output impedances, such as Si LDMOS transistors with output powers in excess of 30 Watts.

This thesis deals with three main issues central to the problems encountered in modern high frequency MMIC packaging. Firstly, the development of new low-power low cost packages utilising cutting edge materials such as liquid crystal polymer (LCP) to compete with the traditional ceramic substrate packages. Secondly, the development of new high power laminate based packages optimised for electrical and thermal characteristics. Finally, the development of passive and active measurement systems used to characterize the developed packages. The active measurement system is based on the load-pull concept to measure and characterise high power packaged transistors. This system is also capable of measuring the waveforms at the device reference plane, which enables the optimised design of Power Amplifiers (PAs).

ACKNOWLEDGEMENTS

I would like to express my deep and sincere gratitude to my supervisor, Prof. Paul J. Tasker for his continuous and unlimited support throughout my time at Cardiff University, and in particular during my PhD. His seemingly unlimited knowledge has continuously inspired me and has made me believe that there is nothing impossible in science. I would also like to thank my second supervisor Dr. Johannes Benedikt for his support and for keeping me focused and on-track. He always helped me to consider the bigger picture with the richness of his ideas and industrial experience.

I would like to thank Prof. Adrian Porch, who has always been there to advise and guide me in both technical and non-technical related matters, and in particular, for providing the valuable opportunity for me to work with Physics group at Cardiff University.

I would like to thank Labtech Ltd for sponsoring this work and, in particular, Mr. John Priday for his endless support, and Dr. Brian Mazonas for driving the activity. I would also like to thank John Leaf, Gary Morgan, David Gittins and Gil Edwards for their support while I was at Labtech.

During my study at Cardiff University I have been fortunate to meet people whom I now consider very good friends, in particular Dr. Jonathan Lees whose early support and subsequent proof reading of this thesis I particularly appreciate. More recently, Tudor Williams, Peter McGovern, Aamir Sheikh, Hao Qi and Chris Roff (who has also helped in the proof reading of this thesis). Within the Physics department, I have met a number of people who have become friends of mine; Simon Doyle, Dr Philip Mauskof, Giampaolo Pisano, Bruno Maffei and Luca Pietranera have all inspired me with their deep knowledge linking engineering to physics.

I would like to say a **big thanks** to my late mother who looked after me all the way through my PhD study until my last days at Cardiff University. I thank her for her patience, prayer and good wishes; she was always praying and wishing to see me reach this stage which unfortunately has not been able to witness. I would also like to thank my father for his unlimited support and wise advice. Being my father he is also my best friend, whom I always ask for the right advice. I would like to thank my brother for his continuous support and encouragement, and for encouraging me to achieve my goals during difficult times.

LIST OF PUBLICATIONS

Peer Reviewed Publications

1. **Z. Aboush**, J. Benedikt, and P. Tasker, "DC-50 GHz Low Loss Thermally Enhanced Low Cost LCP Package Process Utilizing Micro Via Technology," *IEEE MTT-S International Microwave Symposium Digest*, pp. 961-964, June 2006.
2. **Z. Aboush**, C. Jones, G. Knight, A. Sheikh, H. Lee, J. Lees, J. Benedikt, and P. J. Tasker, "High power active harmonic load-pull system for characterization of high power 100-watt transistors," *European Microwave Conference*, vol. 1, pp. 4-6, October 2005.
3. **Z. Aboush**, J. Lees, J. Benedikt, and P. Tasker, "Active Harmonic Load-pull for Characterizing Highly Mismatched High Power Transistors," *IEEE MTT-S International Microwave Symposium Digest*, pp. 1311-1314, June 2005.

Publications

4. **Z. Aboush**, J. Benedikt, J. Priday, and P. Tasker, "Novel cost-efficient packaging technology for high-power LDMOS devices," *IEEE High Frequency Postgraduate Student Colloquium*, pp. 15 -18, September 2005.
5. **Z. Aboush**, J. Benedikt, and P. Tasker, "High power harmonic active load-pull using broadband impedance transformers," *IEEE High Frequency Postgraduate Student Colloquium*, pp. 145-150, September 2004.

Other Publications

6. **Z. Aboush** and A. Porch, "Compact, Narrow Bandwidth, Lumped Element Bandstop Resonators," *IEEE MICROWAVE AND WIRELESS COMPONENTS LETTERS*, vol. 15, pp. 524-526, August 2005.

PhD Achievements

The work carried out in this thesis resulted in significant published achievements. The first achievement of this work was the design and development of new broadband DC-50GHz low power package using liquid crystal polymer laminate material. The resultant package sustained less than 0.3dB of insertion loss and more than 15dB of return loss across the whole bandwidth, including the package as well as the mounting structure. This was achieved by developing a logical design methodology which enabled via transition and package-to-mounting structure optimisations. The newly designed package offered significant cost reduction compared to its corresponding ceramic packages.

The second achievement was the development of an advanced linear measurement system using multi-tier calibration techniques. This enabled the accurate calibration of the measurement system using traceable standards while shifting the measurement reference plane up to the package plane(s) and consequently a true package model was extracted.

The third achievement was the design and development of new high power package utilising laminate technology. This approach enabled the use of low cost printed circuit board (PCB) manufacturing process to produce these packages. The resultant package offered competitive performance to ceramic packages at much lower cost.

The final achievement was the development of a new and powerful non-linear measurement system capable of characterising high power transistors in excess of 100W CW power. The system was equipped with multi-tier calibration feature which enable accurate measurement system calibration at the coaxial reference plane using traceable standards while shifting the measurement reference plane up to the device under test (DUT) plane using second tier calibration. The system is also capable of measuring waveforms at different reference planes which helps giving deep understanding of the DUT behavior. Also the measurement system imperfection was studied in more details and used to further improve measurement system performance.

Glossary of Terms and Acronyms

<i>Term</i>	<i>Description</i>
ADS	Advanced Design System
BGA	Ball Grid Array
CAD	Computer Aided Design
CPWG	Conductor Backed Coplanar Waveguide
CTE	Coefficient of Thermal Expansion
D.K.	Dielectric Constant
DUT	Device Under Test
EM	Electromagnetic
GSG	Ground Signal Ground
HFSS	High Frequency Structure Simulator
IPD	Integrated Passive Devices
LCP	Liquid Crystal Polymer
LDMOS	Laterally Diffused Metal Oxide Semiconductor
LRL	Line, Reflect and Line
LRM	Line, Reflect and Match
LTCC	Low Temperature Co-fired Ceramic
MMIC	Monolithic Microwave Integrated Circuit
MOSFET	Metal Oxide Silicon Field Effect Transistor
MTA	Microwave Transition Analyser
PA	Power Amplifier
PCB	Printed Circuit Board
PoP	Package on Package
QFN	Quadrature Flat no-Lead
RF	Radio Frequency
RLGC	Resistance, Inductance, Conductance and Capacitance
Rth	Thermal Resistance
Si	Silicon
SiP	System in Package
SMD	Surface Mount Devices
SMT	Surface Mount Technology
SOL	Short, Open and Load
SOLT	Short, Open, Load and Thru
S-Parameters	Scattering Parameters
SP-CSP	Stacked Package Chip-Size Package
SPICE	Simulation Program with Integrated Circuit Emphasis
SWR	Standing Wave Ratio
TMM	Temperature Stable Circuit Board Materials
T-Parameters	Transmission Parameters
TRL	Thru, Reflect and Line
TRM	Thru, Reflect and Match
VNA	Vector Network Analyser
VSWR	Voltage Standing Wave Ratio
WALN	Wireless Local Area Network
WLCSP	Wafer Level Chip Scale Package

TABLE OF CONTENTS

Abstract	iii
Acknowledgement	iv
List of Publications	v
PhD Achievements	vi
Glossary of Terms and Acronyms	vii
Table of Contents	viii
Chapter 1. Introduction	1
1.1 Package Design Objectives and Limitations	4
1.2 Thesis Objectives	5
1.3 Thesis Structure	5
1.4 References	8
Chapter 2. Low-Power Low Cost Packages Characterization and Evaluation	9
2.1 Low Power Package Literature Survey	9
2.2 Packaging Technologies	10
2.3 Package Measurement Techniques Overview	17
2.4 Electrical Measurement System Setup for Passive Package Measurements	19
2.5 Measurement System Calibration Procedures (Multi-tier Cal)	21
2.5.1 SOLT Calibration	23
2.5.2 TRL/TRM Calibration	23
2.5.3 Embedding and De-embedding Techniques	29
2.6 Summary	32
2.7 References	33
Chapter 3. Design, Realization and Measurements of Laminate Based Low-Power Packages	36
3.1 Package Design Basis	36
3.2 Reduced Capacitance Package Design and Measurement	39
3.3 LCP Package Design and Modelling	43

3.4	Package Realization	50
3.5	LCP Package Measurement	51
3.6	LCP Package Design with Launching Structure	54
3.6.1	Mounting Board Design	55
3.6.2	Package Bottom (Buried) Conductor-backed Coplanar Transmission Line Design	56
3.6.3	Transmission Line Impedance Environment Change Interface	57
3.6.4	Package Top Microstrip Transmission Line	59
3.6.5	Package Via Section Design	59
3.7	LCP Mounted Package Measurement	60
3.8	Thermal Analysis for the LCP Mounted Package	63
3.9	Summary	68
3.10	References	69

Chapter 4. High-Power Packages and Their Characterization

	Techniques _____	70
4.1	High-Power Package Technologies	70
4.1.1	High Power Ceramic Packages	70
4.1.2	High Power Plastic Packages	72
4.2	Measurement Techniques for High Power Packages	76
4.3	High-Power Time-Domain Active Harmonic Load-pull Measurement System Overview	80
4.3.1	Load-pull Measurement Systems Limitations	81
4.3.2	Voltage Standing Wave Effect in Load-pull Systems	81
4.3.3	Load-pull Power Levels Associated with the Active Load-pull Measurement Systems	84
4.4	New Measurement System Description	87
4.5	Impedance Transformation Solution	88
4.5.1	Narrowband vs Broadband Impedance Transformers	92
4.5.2	Optimum Impedance Transformer Design	93
4.6	System Mismatch Issue	94
4.7	Hybrid Load-pull Measurement System	96
4.8	Measurement System Calibration	98

4.9 Measurement System Verification	102
4.10 Summary	106
4.11 References	107
Chapter 5. High-Power Package Design and Measurements _____	109
5.1 High Power Package Description	109
5.2 Package Design	110
5.2.1 Electrical Design	110
5.2.2 Thermal Analysis	112
5.3 Package Realization and Measurement	114
5.4 Summary	119
5.5 References	120
Chapter 6. Conclusion and Future Work _____	121
6.1 Conclusion	121
6.2 Future Work	123
Appendices _____	125
Appendix A. Two-port Calibration Using Thu, Reflect and Line (TRL)	126
Appendix B. Lossless Reciprocal Network Analysis	136
Appendix C. Standing Wave Analysis in Load-pull Measurement Systems	139
Appendix D. Load-pull Power Analysis for non 50 Ohm Measurement Systems	143
Appendix E. Klopfenstein Taper Design	145
Appendix F. Impedance Transformer Characteristic Impedance Measurements	149
Appendix G. Publications	157

CHAPTER 1

INTRODUCTION

Semiconductor technologies have undergone rapid development over recent decades, and the electronic packaging industry in particular has faced many challenges due to ever increasing device performance, levels of device integration and reductions in physical size. The problems lay in the fact that while semiconductor devices are getting smaller, their functionality is increasing significantly. Operational speed is also increasing rapidly due to the ever-increasing demand for bandwidth, resulting in ever-increasing electrical performance requirements which implied higher levels of power consumption. From the packaging perspective, the smaller the package; the less heat it can dissipate. Also the smaller size of for example signal tracks, results in increased losses which scale with increasing frequency. Stacked-dies in system-in-package (SiP) modules and stacked package-on-package (PoP) technologies are also placing an additional burden on the overall package performance due to the need for vertical expansion which requires a significant amount of routing and interconnect optimisation. As a result, good quality RF substrate materials and small and efficient interconnect geometries are under continuous demand to fulfil current and future semiconductor packaging requirements. The improvement in semiconductor device performance and cost has been a facilitating factor in a huge range of technological advances. Numerous applications have been made possible largely due to the availability of cheap, reliable and high performance electronic circuits. Perhaps the most important of these applications has been radio frequency communication.

In a typical RF device package, multiple dies can be used in order to realise a complete solution (module). These packages must fulfil the requirements for small size, high power, multi-functional, broadband, and most importantly low cost RF devices and modules.

Although the semiconductor dies can be placed directly into the PCB board for example in mobile phone, this option is very limited for a number of reasons. The first reason is that high-technology vendors cannot make much profit from unpackaged devices. The other important factors are manufacturability and reliability. On the manufacturing side, high-end applications companies (e.g. mobile phone

manufacturers) do not normally prefer to bring all the manufacturing processes in-house since it makes mass-production very expensive and the manufacturing lead times can become significant.

From a reliability point of view, the PCB board, by nature is a good moisture absorber and is also easily bent. Therefore, if the PCB board is dropped or is exposed to frequent mechanical shock, this can cause the die to detach from the board.

The other factor is that mounting the die directly will limit its suitability to different vendors who deal with end applications due to the inability to perform routing for different customer PCB boards. In reality, PCB boards are multilayer and, for complex circuits like Bluetooth and WLAN modules where the simplest die has around 80 to 90 Input / Output (I/O) pins, these pins have to be routed to make contact with different layers, which can only be done using packages.

The basic requirements for any package are to physically protect and provide a near electrically transparent housing for the MMIC inside. The ideal package should pass the electrical signal with minimum degradation while perfectly dissipating any heat generated by the semiconductor; all this to be achieved at a fraction of the cost of the MMIC inside. Therefore, much research has gone into creating packaging solutions that fulfil stringent demands on electrical, thermal, protective and financial performances.

Unfortunately, the financial cost of the best performing ceramic RF package technology is prohibitive for many commercial applications. While ceramic based packages have been shown to offer the best performance [1, 2] for RF and millimetre wave MMIC packaging, the cost of these packages is becoming a significant part of the overall RF module cost, and in some cases even exceeding the price of the MMIC itself. Therefore, many solutions have been introduced in the past which sacrifice performance in order to cut the package cost. An example of this trend has been the popularity of molded plastic packages.

More advanced technologies such as Ball Grid Array (BGA) and the Wafer Level Chip Scale packaging (WLCSP) can provide a compact environment for the MMIC while achieving good electrical performance. Unfortunately, these kinds of packages are more prone to thermal issues.

Other technologies introduced in recent years include the laminate based surface mount packages. Laminates (Fig. 1) usually have copper on both sides, providing flexibility in manufacturing since patterns can be created on both sides at once which

also make it suitable for multilayer package substrate as well as different package sizes can be realized. Laminate packages are fabricated using standard, well established PCB manufacturing technologies. These processes have been optimised for cost which means that manufacturing costs of such packages is very low. In addition, the laminate itself is relatively low-cost.

These laminate based surface mount packages require wire bonding to connect to the MMIC and are also slightly bigger than the BGA and WLCSP equivalents. Their advantages lie in competitive electrical performance compared to ceramic solutions, and their significantly lower cost. This technology holds great promise to replace the high performance ceramic packages, especially with the emergence of the new crystalline filled polymers or so called Liquid Crystal Polymer or LCP (Fig. 1.b) which have dual properties of low electrical loss and associated cost that is significantly less than ceramic. Indeed, with the existence of different laminate materials to suite different power levels, the laminate based packaging technology has recently been extended to include high-power (>30W) RF transistors [3].

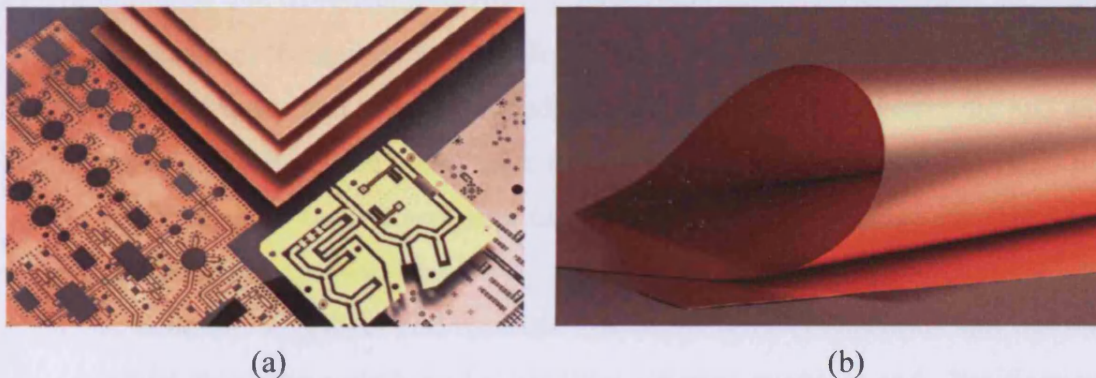


Fig. 1 Laminate substrates - a) Standard high frequency laminate and b) Liquid crystal polymer (LCP) laminate.

Another interesting feature associated with laminate is the ability to embed passive circuits on the same package substrate (laminate) which can replace some of the external passive components attached to the packaged device. This technology is known as Integrated (embedded) Passive Devices (IPD) and can offer cost reduction and module size reduction through the elimination of the external passive components.

One challenging future packaging technology that is yet to emerge is stacked wafer chip scale package (CSP) packages which includes massive routing on each silicon layer. The in-silicon via is probably one of the most critical passive components for

future packaging and routing technologies (the smaller and more numerous the vias, the more useful the package; this comes at a cost of increased loss and cost however). This new technology will increase the challenge faced by RF package engineers in maintaining a clean, transparent path for RF and high-speed digital signals alike. When the die pads become high in number, the on-die routing can become extremely difficult, therefore a routing PCB layer (package substrate) can become necessary which represents the package itself. This kind of architecture will possibly to be used and expanded in the foreseeable future where one package is mounted onto another, with the routing being performed on the package level as well as the silicon level.

1.1 Package Design Objectives and Limitations

The packaging objective is not only to protect the die from the external environment, but also to provide an electrical connection to the external world and a thermal path to dissipate the heat introduced by the device. In fact, packaging can be a critical factor in achieving high performance whilst meeting the cost objectives in many microelectronics and computer systems [4]. Essentially, an RF package must provide:

1. Connections to the mounted dies for power (DC) and signal (RF) lines.
2. An electrically and thermally conductive base to attach the active die and any associated components. However in technologies such as flip-chip, where the die is ‘flipped’ over, a heat sink can be attached to the package top surface to dissipate the excessive heat.
3. A structure to protect and maintain the integrity of connections and the die, whilst providing a platform for handling, external markings and identification; this is basically the package cap or lid.

For the first point the ultimate goal is to design a package with an all-pass filter with a frequency response similar to that of a transmission line. This is a challenging task since the package normally contains components other than transmission lines, such as vias and launching points, where changes in impedance environments exist, requiring careful matching design. The bonding wires themselves will also affect the RF signal and therefore wire bonding compensation circuitry becomes necessary.

For the second point, the package base serves two functions: the first is to provide a good electrical contact to ground with minimum ground inductance (which adds to the transistor’s source inductance), and secondly to provide a good thermal path to dissipate the heat associated with the device. Combining these two objectives into one

is quite difficult. However, with the emergence of special electrically and thermally conductive pastes, and by using bare copper as a package base, this objective can be met to some extent.

The third and final point is the package cap which can be realised either by using a metal lid or plastic lid. The metal lid can cause significant side effects since it can trigger cavity resonance effects leading to device oscillation and instability. However, both metal and plastic lids can change the package RF performance since they provide an RF path for interactions between the package components. As a result, the package lid has to be taken into account during the design process.

1.2 Thesis Objectives

The objectives of this work were to investigate the use of low cost laminates that exhibit very low electrical losses and excellent thermal properties in the design and realisation of two kinds of package. The first objective is to design a DC to 50 GHz broadband low power surface mount package utilising liquid crystal polymer (LCP) laminate as an alternative cost effective technology, with properties similar to those of ceramic equivalents. For this design, micro-via technology will be used as a form of transition between metallization layers. Micro-vias are attractive due to their small physical size and the flexibility in controlling their geometries. This kind of via helps with package miniaturisation as well as allowing hermeticity

The second objective is to design a laminate based, high-power package suitable for high-power transistors, especially the popular LDMOS devices with power rating exceeding 30 Watts of CW power. In this application, the laminate based package process provides a significant cost reduction compared to corresponding ceramic based packages.

In order to develop these high-power packages, it was necessary to conceive and develop a new measurement system capable of characterising high-power devices (>30 Watt CW).

1.3 Thesis Structure

This thesis is divided into two main parts; low-power package design and characterization (Chapters 2 and 3), and the high-power package design and characterization (Chapters 4 and 5).

Chapter 2 presents a thorough literature survey, summarising the available low power packaging technologies, their applications and their measurement techniques. The measurement system used to characterise the packages presented in this thesis, including low power packages is discussed in detail. Different measurement setups are explained along with their associated calibration procedures, including multi-tier calibration approaches.

Moving forward to Chapter 3, the package design evolution is presented, starting with a basic package used at the beginning of this work, provided by Labtech Ltd, and then going through multiple iterations of analysis and package optimisation in order to achieve a logical and coherent method for designing broadband, high frequency, low-loss packages. Package modelling has been tackled and is used as a design aid to design new LCP packages with the ultimate package being mounted onto a PCB board. All packages presented in this chapter are measured using the measurement system discussed in Chapter 2.

Thermal analysis is also presented for the ultimate mounted LCP package in order to determine the maximum device power rating that can be accommodated inside these packages.

Chapter 4 deals with the high-power packages and their characterization techniques. Here, a literature search on high-power packages is presented which includes the ceramic and over-molded plastic packages. Also a review of the available measurement techniques, specifically passive and active load-pull measurement systems and their suitability for characterising high-power packages is presented. High-power, time-domain active harmonic load-pull measurement systems, their limitations and the problems associated with measuring high-power, low-impedance devices are discussed. Specifically, the need for increased load-pull power levels and the problems of very-high VSWR associated with increased load-pull power are presented in great detail.

In this chapter, a new time domain, active harmonic load-pull measurement system is described. The new system utilises broadband impedance transformers to solve the problems associated with active load-pull measurement systems when characterising packaged high-power, low impedance devices.

Also in this chapter, the system characteristic impedance mismatch associated with the high-power active load-pull measurement systems is studied and analysed. This impedance mismatch problem exploited in order to design a new, powerful hybrid

load-pull measurement system which is capable of characterising high-power, low impedance devices with a minimum amount of load-pull power.

The measurement system calibration techniques are also described in detail and the measurement system has been verified by measuring a 100 Watt LDMOS device which confirmed the validity of the analysis presented in this chapter.

In Chapter 5, a high-power package suitable for high power devices (e.g. 30 Watt LDMOS device) has been designed, the electrical and thermal design analysis are presented in full. The package was manufactured and verified with a 30 Watt Philips LDMOS device. The packaged device was then characterised using the newly developed measurement system described in Chapter 4 of this thesis and compared to similar device in a standard commercially available package.

Finally, conclusions and future work are presented in Chapter 7.

1.4 References:

- [1] K. Yoshida, T. Shirasaki, S. Matsuzono, and C. Makihara, "50 GHz Broadband SMT package for microwave applications," *Electronic Components and Technology Conference Proceedings, 51st*, pp. 744 - 749, 2001.
- [2] H. C. Huang, A. Ezzeddine, A. Darwish, B. Hsu, J. Williams, and S. Peak, "Ku-Band MMIC in low-cost, SMT compatible packages," *IEEE MTT-S International Microwave Symposium Digest, 2002*, vol. 1, pp. 27 - 30, June 2002.
- [3] Z. Aboush, J. Benedikt, J. Priday, and P. Tasker, "Novel cost-efficient packaging technology for high-power LDMOS devices," *IEEE High Frequency Postgraduate Student Colloquium*, pp. 15 -18, September 2005.
- [4] D. Boulin and H. Safar, "Plastic Packages Take On High-Power Devices," *Microwave and RF Online Journal*, pp. 1-2, February 2004.

CHAPTER 2

LOW-POWER LOW COST PACKAGES CHARACTERIZATION AND EVALUATION

In this chapter, a thorough literature survey summarising the available low power packaging technologies, future trends and measurement techniques will be presented. Additionally, detailed discussions are presented for a passive measurement system used to measure the low power packages introduced in this thesis along with the calibration procedures to allow parameters to be measured at the package plane for the various package structures.

2.1 Low-Power Package Literature Survey

Low power packages have gone through a long development process and although it has been slow compared to semiconductor research, the advances have been significant and the costs have been significantly reduced. The basic requirements for any package are to physically protect and provide a near electrically transparent housing for the MMIC inside. The ideal package should pass the electrical signal with minimum degradation while perfectly dissipating any heat generated by the semiconductor. However this ideal is not the case for the current packaging technologies, where the package usually degrades the electrical signal to some extent and the package is usually unable to fully dissipate the heat associated with the MMIC inside. This causes the package temperature to increase which in turn leads to mechanical problems; namely package expansion when hot and contraction when cold. The hot-cold cycle will gradually degrade the package mechanical stability and reliability. Choosing proper package materials with comparable thermal coefficients will minimize this effect, although it is not practicably feasible, because there is no such dielectric with a similar coefficient of thermal expansion (CTE) to Silicon and Copper. Ultimately the package has to be optimized for heat dissipation design which can also minimize the above effects while maintaining low manufacturing cost rather than using expensive materials.

Combining a high performance dielectric with a good thermal design will give the opportunity to come up with a high performance package at a fairly reduced cost.

In this work liquid crystal polymer (LCP) material, which represents the cutting edge technology in high frequency dielectric materials, has been used as the material of choice in which to design and fabricate high performance low power packages delivering low cost solutions. Good thermal management in the designed package may insure optimum electrical and thermal performance at reduced substrate and manufacturing cost.

2.2 Packaging Technologies

Due to the diversity of semiconductor applications, a wide range of packages have been developed to accommodate different MMICs. Irrespective of the package shape, there are recognisable packaging architectures and topologies which can be summarised into the following main categories:

Plastic RFIC Packages: Plastic package technology (Fig. 2.1) has been the workhorse of the integrated circuit industry for many years, and this will continue for the foreseeable future [1]. The major advantages of these kinds of packages are the cost, since they are extremely cheap with relatively high performance. Two major kinds of plastic package are available; these are the Lead-frame packages (Fig. 2.1.a) and Quad Flat no-Lead packages (Fig. 2.1.b).

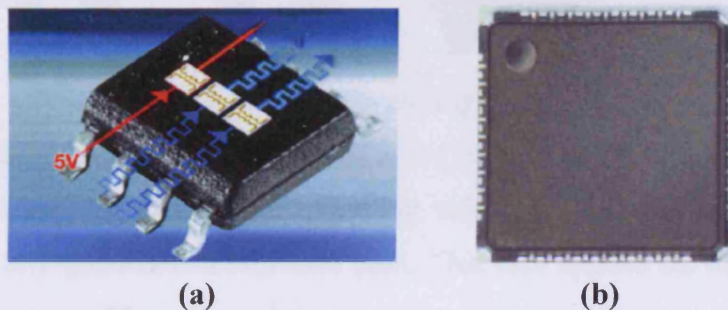


Fig. 2.1 Plastic packages (a) Lead frame, (b) Quad Flat no-Lead (QFN) packages

The main disadvantage with the Lead-frame packages is that they have limited number of pin counts in addition their RF frequency handling is limited to few GHz, which is mainly due to the inductance rise associated with the lead frame at increasing frequencies. One of the solutions aimed at increasing the bandwidth of this kind of package up to 10 GHz, is to modify the lead frame to maintain 50 Ohm impedance environment[2]. This approach holds great promise for increasing the performance of such RF packages at higher microwave frequencies.

However, quadrature flat-no-lead (QFN) packages are even cheaper and their pin counts[3] are higher than the lead-frame packages although it is still low compared to

flip-chip or BGA packages discussed below. Again, the RF performance of these packages is quite limited.

Flip-Chip Technology: In this technology the die pads are bumped with solder balls and the whole die is flipped over a double sided (multi-layer) substrate usually made of FR4 or similar cheap material (Fig. 2.2). The routing can be made on both substrate metallization layers with the solder bumps being attached to the substrate bottom side. The key advantage of flip chip technology is size, flip chip packages do not require peripheral space for the wire bonds thus, they can be made smaller than wire bond packages with a similar I/O count. For dies with a high I/O count, flip chip technology offers large space savings since the I/O can be arranged in an array on both the die and the substrate. At the substrate level, routings can be directed through multiple internal layers [4]. The short signal paths associated with the flip chip technology provide low inductance, resistance and capacitance, resulting in faster signal propagation and better high frequency performance.

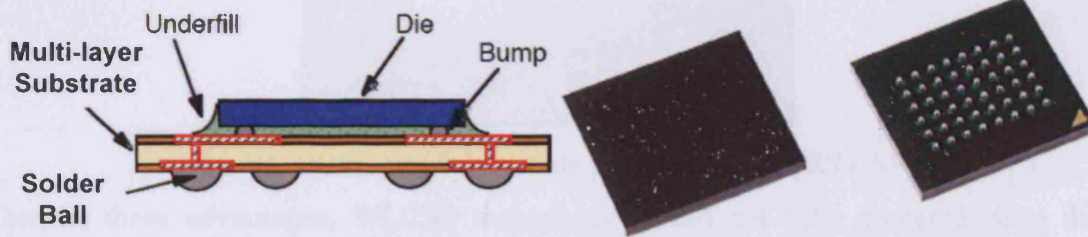


Fig. 2.2 Flip chip package example

The major disadvantage of this technology is the poor heat dissipation. Since the die is flipped over when attached to the mounting substrate, the back of the die is left unattached to any good heat dissipation path. This also applies on the coefficient of thermal expansion (CTE) mismatch between the silicon and organic PCB leading to cracking of the solder bumps.

Different thermal dissipation techniques have been introduced to enhance this kind of package's thermal properties, [5] including leaving an air cavity between the die and the lid (instead of direct lid-die contact) to aid heat dissipation as well as introducing a special metal heat spreader onto the top of the package. Determining an optimum metal thickness for the heat spreader can improve the thermal management at the package level; hence the die junction temperature can be maintained at a minimum level. An added attraction is that the heat spreader also acts as an environmental protection to the die [5].

The other limiting factor associated with this technology is the cost, which is roughly 2-3 times that of an equivalent wire bond attachment on a per-pin basis [1].

Wafer Level Chip Scale Packages (WLCSP): This package (Fig. 2.3) is an extension of the flip chip technology [6, 7] in the essence that the routing being performed on the die itself (no substrate is required) with the advantages of real die size packaging, high electrical performance and low manufacturing cost.

This kind of package architecture supports a high level of integration and multi-layer capability using a technology called stacked package-chip size package (SP-CSP) [8], where multiple dies are routed and stacked on top of each other to form a multilayer die structure.

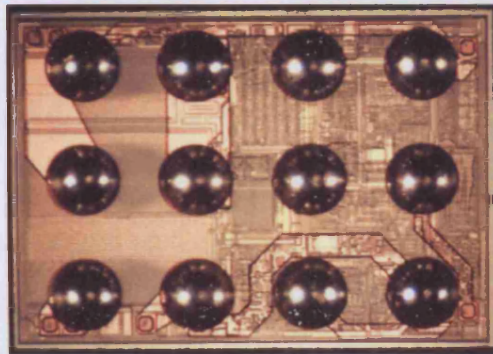


Fig. 2.3 Wafer level chip scale package layout (WLCSP)

Despite these advantages, WLCSP technology is still not fully accepted since the mechanical reliability of a large die cannot be guaranteed. The main drawback of this technology is that it doesn't scale well with increasing die power and increasing temperature due to the mismatch in the thermal expansion coefficients between the silicon chip and the metallization and associated solder bumps (made of 95% tin) which reduce the package reliability. From the electrical point of view, an RF die should contain some RF circuitry and on-chip passive component(s) (e.g. inductors and de-coupling capacitors). Unfortunately since the routing in this technology is done on the silicon die after applying a thin layer of polymer on top of it therefore no routing is preferred on top of the critical RF chip components which will limit the routing area and the total number of balls.

With the mechanical issue, several researchers [9-11] have dealt with the issue of optimizing the solder bump shape and height (profile) to increase the package reliability against temperature cycles, including the incorporation of an underfill material to enhance the package's mechanical stability.

Ball Grid Array (BGA): This technology is similar to the Flip-chip technology in the essence that the die is mounted onto a substrate but here the die isn't flipped but mounted on its back onto the package substrate, the die pads are then connected to the package substrate through bonding wires from which the traces can be routed on the substrate top and bottom metallization layers and connected to the balls on the substrate bottom layer; BGA package examples are shown in Fig. 2.4.a below,

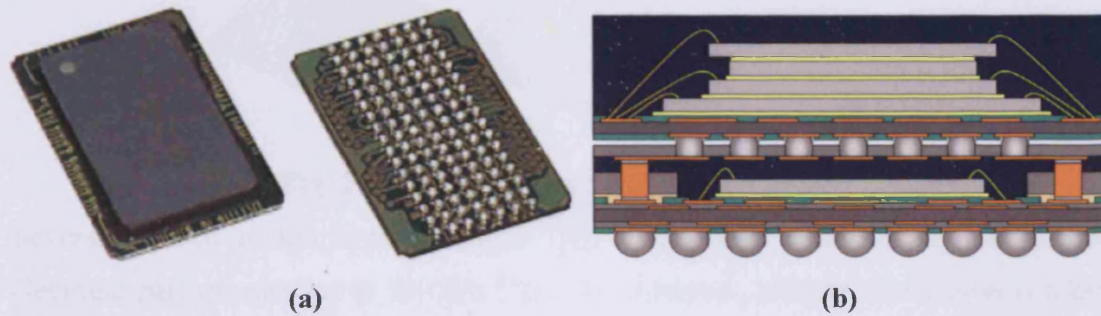


Fig. 2.4 BGA package (a) finished package, (b) Stacked chips in stacked package-on-package (PoP) [12]

This technology allows multiple packages with multiple dies to be stacked on top of each other and bonded to the package substrate as shown in Fig. 2.4.b. In this example two BGA packages are stacked on top of each other in a technology called Package-on-Package (PoP). However there is a limit on the number of dies and packages which can be stacked on top of each other, this is because every time a die is attached the whole package has to be baked. Therefore there is maximum number of times the silicon can be exposed to heat (baked) without damaging its circuitry (usually this is specified by the silicon manufacturer).

The major disadvantage associated with this technology is the package poor ability to dissipate heat therefore thermal vias and centre thermal balls have to be used to provide sufficient thermal escape path. The manufacturing cost of BGA package is more than WLCSP and the plastic packages. However the assembly cost of BGA package is much less than the WLCSP which bring the cost of BGA solution well below the WLCSP solution.

Low Temperature Co-fired Ceramic (LTCC) Packages: This technology was originally developed for military applications where high performance and reliability are of the uppermost importance. The technology has subsequently established itself in a variety of commercial applications. LTCC layers are built up on individual layers of flexible ceramic tape which are pressed together and fired at 900°C, resulting in a

multi-layered ceramic structure which exhibits relatively low loss and shrinkage [1]. The other ceramic substrate types are made of Alumina which, thanks to its crystalline structure, can also provide a very low loss substrate suitable for use in RF and millimeter wave applications.

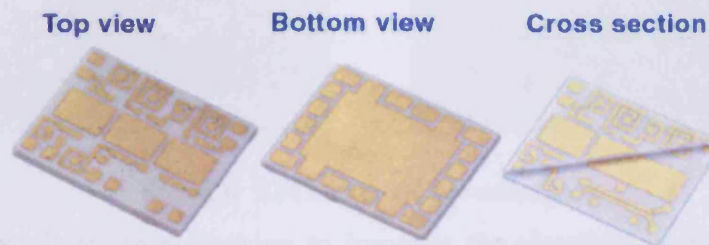


Fig. 2.5 Alumina ceramic package example

Several surface mount type packages (Fig. 2.5) have demonstrated very good electrical performance up to 50 GHz [13, 14]. However, thermal dissipation is a key challenge facing this kind of package which has always attempted to treat the problem at the package design level rather than optimizing the materials themselves [13]. Unfortunately, the cost for these packages is rather expensive due to the fact that the ceramic material and its manufacturing process is expensive and also the package tooling can be expensive since these substrates are brittle and therefore it is difficult to shape and saw. However when the package performance cannot be compromised, then this package is currently the best solution.

Laminate Based SMT/D Packages: Laminate based surface mount technology (SMT) packages (Fig. 2.6), or sometimes so called surface mount devices (SMD), is a new technology which targets the package cost issue by replacing the costly ceramic substrate with normal high frequency substrates (e.g. glass reinforced ceramic laminate).

Due to its flexibility when integrating it with other electronic components this kind of package has found its way into a number of current applications, such as mixers [15], millimeter-wave transceiver module [16], low noise amplifiers [17] and other MMIC applications [18, 19].

Although the cost of these packages is low compared to a corresponding ceramic packages and its frequency range can go up to 40 GHz, the electrical performance of these packages represents a challenge for package designers.

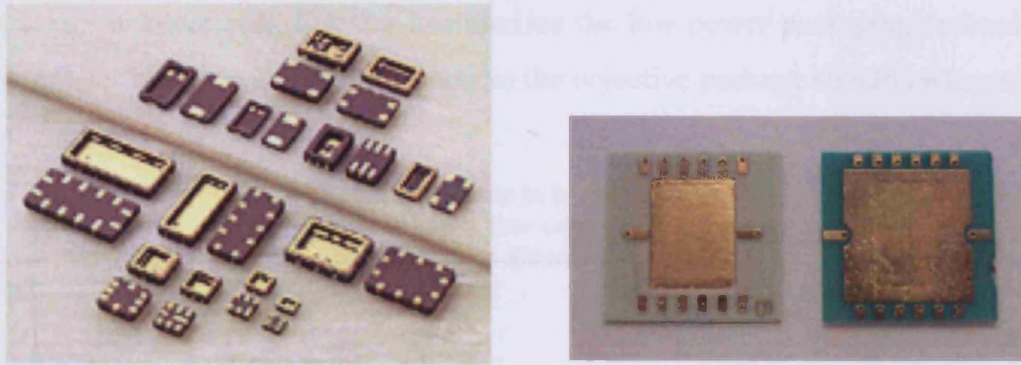


Fig. 2.6 SMT/D package examples

Many researches have been working to improve the electrical performance of these packages, including optimization of the transitions inside the package and the launching to the package from the PCB [13, 20-22]. Indeed, some researchers have started investigation into replacing the traditional laminates (e.g glass reinforced ceramic laminate) with high performance laminate materials such as liquid crystal polymers (LCP) [23-25]. These materials represent the cutting edge of MMIC packaging technology, and have shown that they are broadband and capable of competing with the expensive traditional ceramic substrates [25], a 50 Ohm, 1 cm LCP coplanar transmission line can have the frequency response shown in Fig. 2.7.

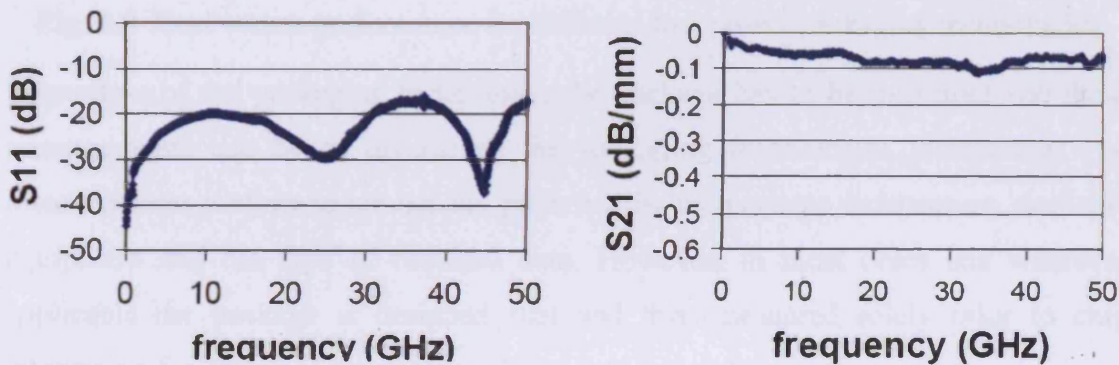


Fig. 2.7 Measured return and insertion loss of a CPW line on a 125 μm thick LCP substrate (width=235.5 μm , gap=50 μm) [25]

This material holds a great promise to significantly impact the packaging market, with the only problem associated with it being its high z-axis expansion. Novel DC-60GHz packages made of LCP substrate have been reported [26] with 0.5dB of insertion loss and more than 10 dB of return loss. The design of such packages relies on normal through vias coupled with complex in-package matching techniques.

The objective of this work on low power packages is to develop a high performance low power package with similar performance to the best performing ceramic packages

but at much lower cost. Fig. 2.8 summarises the low power packaging technologies cost and performance and identifies where the objective package should be located.

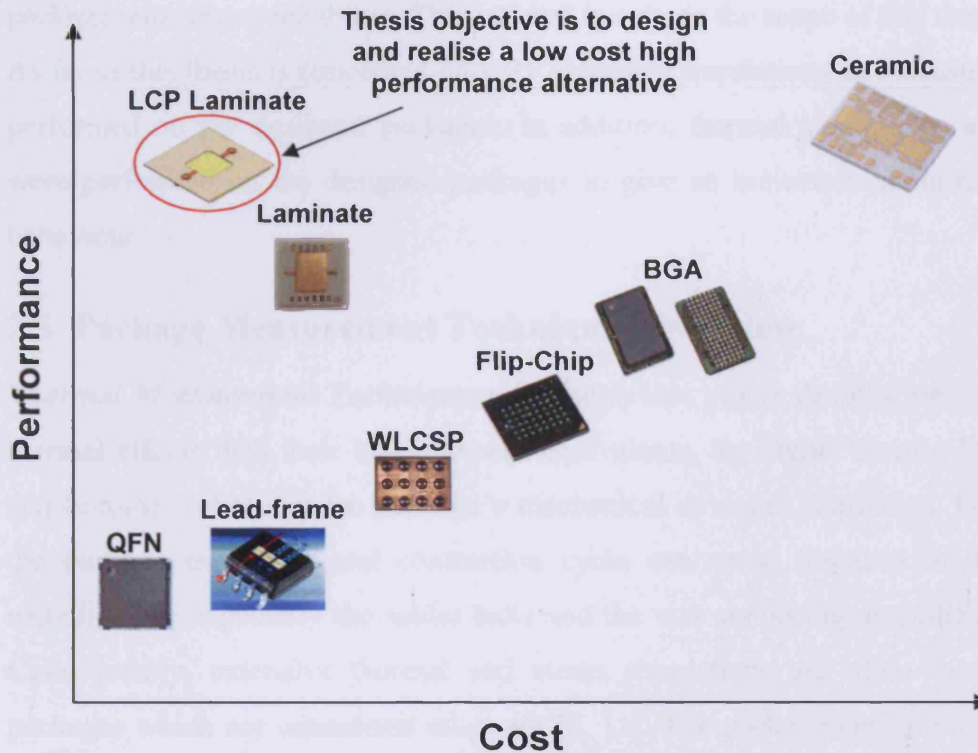


Fig. 2.8 Cost versus performance for different low power packaging technologies

Regardless of the packaging technology, the package has to be measured and these measurements can be as diverse as the packaging technologies themselves. The measurements performed are usually governed by the package architecture, available equipment and the type of required data. However, in most cases and wherever applicable the package is designed first and then measured solely prior to chip integration for different parameters. These pre-integration measurements can give a clear indication about the package overall performance and reliability when it will be under operation. Among these measurements are the electrical measurements where the package is tested for its RF (analogue) and/or signal integrity (digital) performance (e.g. insertion loss, return loss, cross talk, cavity resonance, leakage current, RLGC model,...etc) to make sure that the RF and digital paths are well designed and therefore optimised. Other measurements involve measuring the package thermal performance which also describes the package's mechanical stability under thermal cycle tests (i.e. to make sure no cracks will develop when the package is exposed to thermal cycles). Other industry standard tests include a drop-test, which

involves the package being attached to a PCB board and then the whole board is dropped in test chamber at specific speed and acceleration to emulate the physical drop effect; this test is very useful to check the package to PCB connection and die to package attachment reliability. This last test is outside the scope of this thesis.

As far as this thesis is concerned only RF electrical simulations and measurements are performed on the designed packages. In addition, thermal simulations and analysis were performed on the designed packages to give an indication about their thermal behaviour.

2.3 Package Measurement Techniques Overview

Thermal Measurement Techniques: Although low power devices are less prone to thermal effects than their higher power equivalents, the higher density MMIC chips can become so hot that the package's mechanical structure is affected. For example, the package expansion and contraction cycle can cause fractures in the package metallization, especially the solder balls and the vias connecting metallization layers. Consequently, extensive thermal and stress simulations are often carried out on packages which are considered adequate [9, 11]. The package design process can go through many electrical/thermal design optimisation cycles before passing them to production.

Novel algorithms have been reported, which optimise the height and shape of the solder balls for BGA and WLCSP packages, [9, 10]. Other researchers went as far as to measure the package degradation after a number of temperature cycles (1000-2000 cycles) [5]. The published results from these tests show that the package degradation due to thermal expansion and contraction could be significant if not properly taken into account in the design process.

Electrical Measurement Techniques: A variety of different measurement setups have been utilised by researchers in the past in order to measure the various packaging architectures. For this work, only measurement techniques suitable for the laminate based SMT packages are discussed.

In the generic case, the packages are mounted on a PCB board which provides the launching terminal to the package as shown in Fig. 2.9 [26]. The package ground is presented through the use of multiple vias underneath the die to ensure low ground resistance and inductance while providing thermal escape path. Depending on the

transmission line environment employed in the package design (normally coplanar or conductor backed coplanar structures) the easiest test is to use on wafer probes to measure directly a package shorted with a thru line, this measurement will give a very basic (crude) knowledge about the package itself (no launching effect is taken into account). Another method involves placing the package on a test board and probing the package from one side (on the package top surface) while probing the test board (which is connected to the package bottom surface) from the other side [14]. This method can work provided that the package top surface transmission line configuration is suitable for probe measurement (e.g. Coplanar or conductor backed coplanar structures).

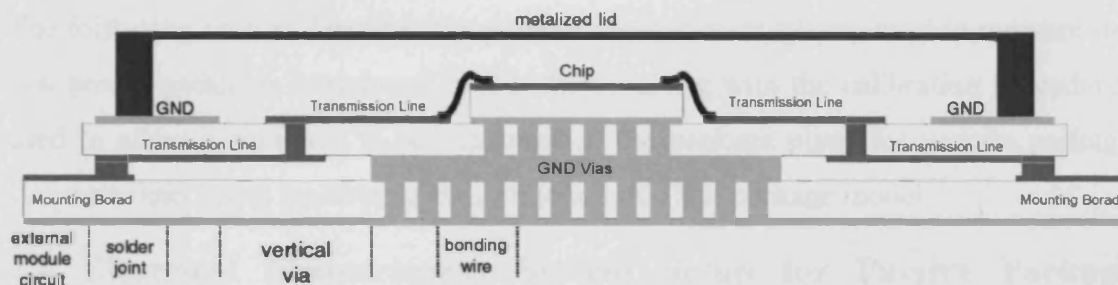


Fig. 2.9 Package mounted on mounting board and the die is placed inside the package and bonded[26]

Another method which tests the package quality is to bond up a precision load inside the package and by observing the package return loss, the package quality can be estimated [27]. Other tests involve placing a piece of transmission line in the package cavity and bonding it to the package using one or two (V-shape) bonding wires [28]. This test will give a rough estimation of the package's behaviour and will verify that no resonances occur at the frequency of interest.

More advanced techniques are available which involve mounting on wafer calibration standards in the place where the device is mounted and bonding them to the package. This approach is capable of giving a complete model for the package, including the launching transition and any via transition in the package transmission path [26]. However there is an increased level of measurement uncertainty associated with this technique due to the bonding wire discontinuity which might resonate at different frequencies depending on the standards attached to them and the wire bond length and profile. Add to that each calibration standard requires a separate package.

The ultimate package measurement requires the placement of an active device (MMIC) with complete bonding and a lid placed on top. The measured device

characteristics for this structure can then be compared to a reference dataset, for example an on-wafer measurement or a well known high quality packaged device of the same type [16-19].

From the above overview it is clear that placing simple Thru transmission line inside the package isn't adequate to reveal the package performance accurately. In order to generate an accurate model for the package to be used in a CAD environment (e.g. s-parameters model) a more complex measurement has to be performed. This implies the development of an accurate and robust measurement system calibrated using traceable standards and utilising multi-tier calibration techniques to shift the measurement reference plane up to the package plane.

The following section describes the passive measurement system used to measure the low power packages introduced in this thesis, along with the calibration procedures used to allow parameters to be measured at the package plane for various package structures and hence facilitating the extraction of a full package model.

2.4 Electrical Measurement System Setup for Passive Package Measurements

A test bench has been set up to enable the measurement and characterisation of the packages presented in chapter 3 of this thesis. This measurement setup is versatile enough to passively characterise the majority of packages.

Since the packages are normally mounted onto a test board with small feature sizes and were to be measured up to 50 GHz, on-wafer probing was considered the most suitable method to connect the packages and/or any associated mounting board to the measurement system.

The measurement system was configured as shown in Fig. 2.10.a; in this measurement setup a Vector Network Analyser (VNA) was used as only linear measurements were required and no active devices were involved. High quality phase-stable, low-loss cables have been used to attach the VNA to a pair of DC-50 GHz GSG probes with 400 um pitch.

Thus, by probing onto a mounting board which is suitable for the probe pitch, and by applying a suitable calibration procedure(s), the measurement reference plane can be shifted to the package plane (Fig. 2.10.b,c).

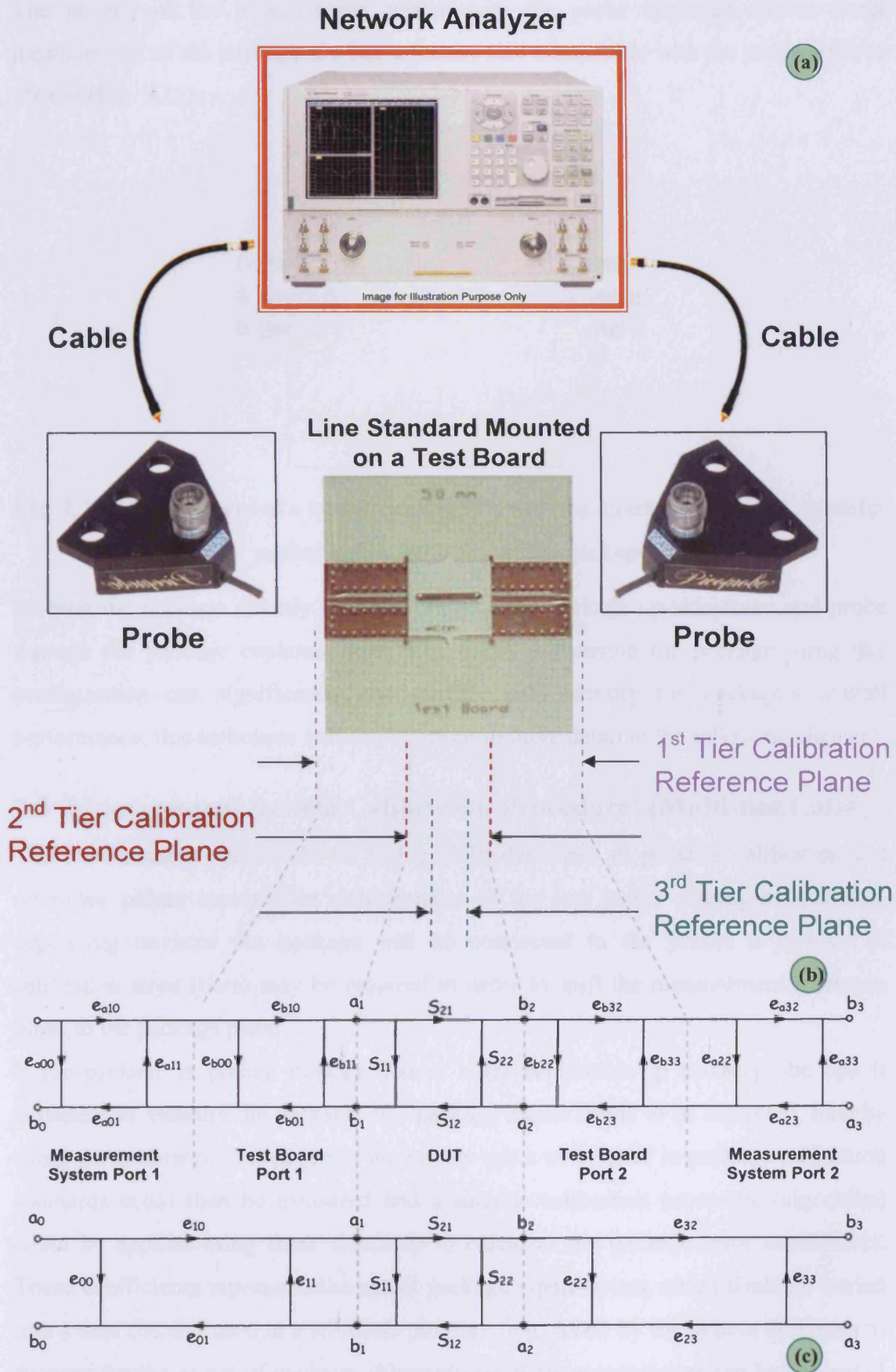


Fig. 2.10 Measurement system setup to perform passive package measurements and the system equivalent error flow graphs

The novelty of the measurement system with the probe approach allows direct measurement of the package if it has a feature size compatible with the probe pitch of 400 μ m (Fig. 2.11).

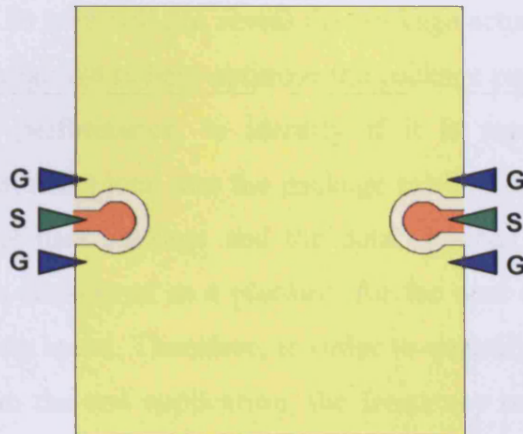


Fig. 2.11 Measurement of a typical package through the direct placement of on-wafer probes on the back side of the package

Probing the package directly involves flipping the package up-side-down and probe through the package coplanar lines (Fig. 2.11). Measuring the package using this configuration can significantly and quickly help identify the package's overall performance; this technique will be discussed in more detail in the following chapter.

2.5 Measurement System Calibration Procedures (Multi-tier Cal)

The measurement system shown in Fig. 2.10 describes all possible calibration and reference planes involved in measurement of the low power packages. However, depending on how the package will be connected to the probes a number of calibration steps (tiers) may be required in order to shift the measurement reference plane to the package plane.

If the package is probed directly then a 1-tier calibration up to the probe tips is sufficient to measure the package. If a package model needs to be extracted, then by using the calibrated probes (up to the probes tip) a new set of in-package calibration standards could then be measured and a suitable calibration procedure (algorithm) could be applied using these standards to calculate the package error coefficients. These coefficients represents the actual package s-parameters which could be buried into a data file and used in a RF CAD program (e.g. ADS) by the system designers to account for the effect of package. Alternatively these s-parameters can be converted

into RLGC model or SPICE model which then can be used by both the analogue and digital designers to include in their designs.

Since packages are normally attached to a mounting board therefore measuring an unmounted package on its own will not reveal the package actual performance although it can be used as a design aid to help optimise the package performance (e.g. to check the overall package performance, to identify if it is resonating at any specific frequency and determine the total loss the package exhibits before mounting it to any mounting board). The bare package and the data obtained from the bare package measurements can be considered as a platform for the next design step which is the package with mounting board. Therefore, in order to quantify the performance of the package to be used in the end application, the frequency response of the mounting board must also be included in the measurements. In order to achieve the necessary measurements at the package reference plane there are various kinds of calibration setups which can be adopted.

Setup 1 - Is to calibrate the measurement system up to the probe tips (referred to as 1st-tier calibration) then perform another calibration using mounting board calibration standards to shift the measurement reference plane up to the package plane this is referred to as 2nd-tier calibration. A 3rd-tier calibration can also be implemented by measuring in-package standards. This calibration can reveal the actual package s-parameters from which a package model can be extracted.

Setup 2 - The measurement system can be calibrated at once up to the package plane using a number of mounting board calibration standards (these can be made by fabricating different standards attached to the mounting board similar to the one which will be used to mount the package onto) which in this case represents the 1st-tier calibration. Again in order to generate a package model a 2nd-tier calibration is required where a range of in-package calibration standards are measured and the responses are used in a suitable calibration algorithm to calculate the package error coefficients and hence the actual response of the package (s-parameters).

Regardless of the package launching topology, the measurement system has to be calibrated up to a certain reference plane. This is done by measuring known calibration standards (e.g. Line, Thru, Open, Offset Open, Short, Offset Short, load, etc...) as part of a calibration procedure, such as SOLT, TRL, TRM, LRL, LRM,

etc... calibration procedures. The most popular standard calibration procedures are described briefly below:

2.5.1 SOLT Calibration: SOLT calibration stands for Short-Open-Load-Thru and in this kind of calibration a SOL calibration is performed on each port to fully calibrate out each port individually. The remaining Thru standard is then used to relate (link) the transmission error coefficients of both ports in a coherent way and also to compensate for any switching effect. The accuracy of this calibration is heavily dependant on the calibration standards definition, in other words the calibration uncertainty depends on how accurate the standards can be defined. The calibration standard manufacturer characterises each standard and generates a model which is converted into polynomial coefficients that are normally entered into the VNA. Unfortunately, when the on-wafer calibration standards are measured and re-measured numerous times (over the course of a number of different calibrations) they experience a change in their characteristics and consequently the coefficients stored in the VNA will not be as accurate. Ideally at this point these coefficients should be adjusted within the VNA definition. This requires a re-characterisation of the calibration substrate to generate the new polynomial coefficients which is difficult to achieve with a high degree of accuracy.

2.5.2 TRL/TRM Calibration: TRL calibration and TRM calibration (which is a specific example of a TRL calibration) are the most popular calibration procedures for on wafer calibration because they can give a very good [29, 30] calibration accuracy over a wide bandwidth. They achieve this because they rely on the accuracy of the Line (or Match for TRM) and Thru standard impedances which are normally set to 50 Ohm. These two calibration methods are described briefly below,

TRL/LRL Calibration: TRL calibration (Fig. 2.12) stands for Thru-Reflect-Line where the Thru standard is a line with 0 mm length, the Reflect standard can take different kinds (e.g. Open, Offset Open, Short, Offset Short), and the Line standard is a line similar to the Thru standard but of a different length.

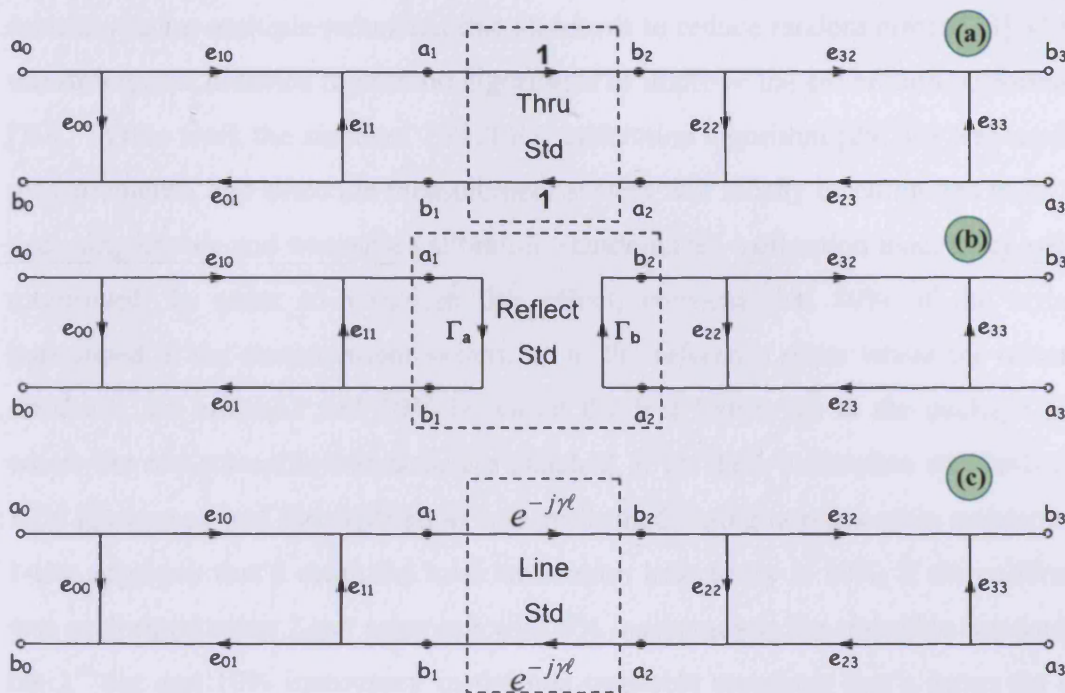


Fig. 2.12 TRL calibration error flow graphs when calibration standards are attached

LRL stands for Line-Reflect-Line where the first Line standard represents a non zero length Thru standard, the Reflect standard is similar to TRL reflect and finally the second Line standard should be longer than the first Line (non zero length Thru) standard.

However in both TRL/LRL methods the Reflect standard has to be the same on both calibration ports and the reflect type should be known in order to solve for the calibration phase ambiguity.

Generally speaking TRL/LRL calibration is one of the most accurate calibration procedures since it relies solely on the impedance of the calibration lines and no standard definitions are required. Clearly, good quality and symmetrical lines with different lengths are essential to obtain a good calibration; it is therefore important that the line impedance is known prior to calibration. A great deal of research work has dealt with impedance measurement techniques [31, 32] where the impedance is calculated based on the measurement of the transmission line propagation constant. As far as this work is concerned, the calibration line impedance is determined from the direct measurement of the calibration lines after calibrating the measurement system up to the probe tips.

There has been a range of publications exploring the quality of TRL/LRL calibration techniques. Many publications have dealt with the issue of increasing the calibration

accuracy using multiple redundant line standards to reduce random errors [33]. Others use orthogonal distance regression algorithms to improve the calibration performance [30]. In this work the standard TRL/LRL calibration algorithm [29, 34] was used for measurements, and since the measurement system will mostly be calibrated in its first tier using known and traceable calibration standards the calibration inaccuracy will be minimised. In order to visualize this effect, consider that 80% of the error is introduced in the measurement system up to the reference plane where the traceable standards are attached and 20% is within the test fixture up to the package plane where the non-traceable standards are attached, if the TRL calibration standards have 10% inaccuracy and the calibration was performed (using non-traceable standards) in 1-tier approach that's mean the total calibration inaccuracy is 10%. If the calibration was performed using 2-tier approach with 0% inaccuracy in the traceable standard for the 1st tier and 10% inaccuracy in the non-traceable standards that's mean the total calibration inaccuracy is reduced to 2% only. The standard TRL calibration algorithm is described in details in appendix A of this thesis [34].

The other important issue associated with TRL/LRL calibration is the determination of the calibration line lengths. Several publications have dealt with this issue [35, 36] and a summery of the line length calculations is given below.

Assuming a transmission media which supports a linear phase, the following expressions can be used to select a Line with $\frac{1}{4}$ wavelength length at the desired centre frequency.

$$\text{Electrical Length} = V_f * \text{Free Space Length} * \text{Line Wavelength} \quad (2.1)$$

Where

$$V_f (\text{Velocity factor \%}) = \frac{1}{\sqrt{\epsilon_e}}$$

$$\text{Line Wave Length} = \frac{1}{4}, \frac{1}{2} \text{ etc.}$$

$$\text{Free Space Electrical Length} = \frac{C}{f}$$

$$C (\text{Speed of light}) = 2.997925 * 10^8 \text{ m/s} \quad \text{and} \quad f (\text{Frequency}) \text{ in GHz}$$

For a Line wavelength of $\frac{1}{4}$, substituting into equation (2.1):

$$\text{Electrical Length} = V_f * \frac{C}{f} * \frac{1}{4} \quad (2.2)$$

In order to cover the whole desired frequency range (f_1 to f_2), f should be the centre frequency of the range, Therefore equation (2.2) can be written as:

$$\text{Electrical Length } (l) = V_f * \frac{2.997925 * 10^8}{\frac{f_1 + f_2}{2}} * \frac{1}{4} \quad [\text{m}]$$

$$\text{Electrical Length } (l) = V_f * \frac{14.989625}{f_1 (\text{GHz}) + f_2 (\text{GHz})} \quad [\text{cm}] \quad (2.3)$$

To determine whether the Line meets the conditions of the acceptable insertion phase (an 8:1 frequency span, harmonic frequencies bandwidth) the following equation is used to check the boundary frequencies (i.e. f_1 and f_2).

$$\text{Phase (degrees)} = 360 * f * l * \sqrt{\epsilon_e} / C \quad (2.4)$$

Note that a phase difference between 18° and 162° has proven to be adequate in some cases. However the National Institute of Standards Technology (NIST) and Hewlett-Packard (HP) both recommend that the phase difference should remain between 30° and 150° . In order to cover greater than an 8:1 frequency span, multiple lines might be used. To do that, the desired frequency span must be divided, allowing $\frac{1}{4}$ wavelength LINE to be used over the lower portion of the frequency span and another one to be used for the upper band. The optimal break frequency is the geometric mean frequency ($\sqrt{f_1 * f_2}$).

TRM/LRM Calibration: TRM/LRM calibration has the same definition as TRL/LRL calibration except that the Line standard is replaced by a Match (Load) standard.

This kind of calibration is much easier to implement compared to the TRL calibration. The accuracy of this calibration procedure depends on the Thru standard impedance and the Match standard quality. Again in order for the algorithm to work it is essential to have symmetrical reflects on both measurement system ports.

The TRM algorithm could be easily formalised by depicting the error flow graph of Fig. 2.10.c while replacing the DUT with the calibration standards, this is shown in Fig. 2.13 below,

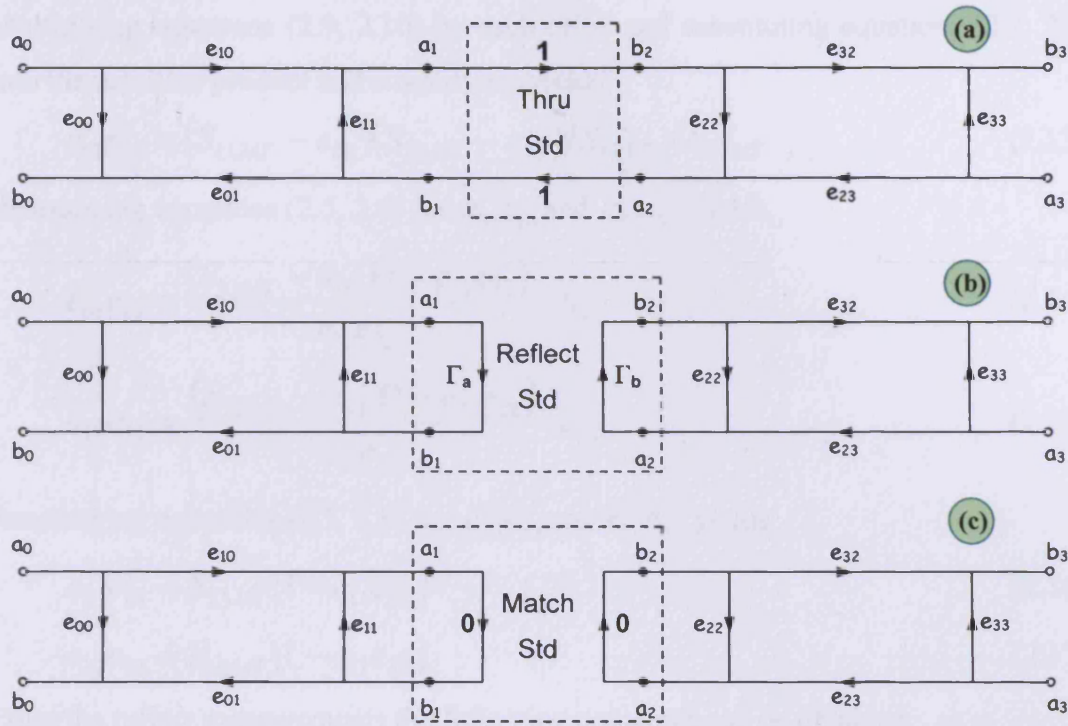


Fig. 2.13 TRM calibration error flow graph for different calibration standards

From the Thru standard measurement the following four equations can be written,

$$S_{11MT} = e_{00} + \frac{e_{01}e_{10} \cdot e_{22}}{1 - e_{11}e_{22}} \quad (2.5)$$

$$S_{22MT} = e_{33} + \frac{e_{23}e_{32} \cdot e_{11}}{1 - e_{11}e_{22}} \quad (2.6)$$

$$S_{21MT} = \frac{e_{23}e_{10}}{1 - e_{11}e_{22}} \quad (2.7)$$

$$S_{12MT} = \frac{e_{32}e_{01}}{1 - e_{11}e_{22}} \quad (2.8)$$

Rearranging (2.5 and 2.6) yields

$$S_{11MT} - e_{00} = \frac{e_{01}e_{10} \cdot e_{22}}{1 - e_{11}e_{22}} \quad (2.9)$$

$$S_{22MT} - e_{33} = \frac{e_{23}e_{32} \cdot e_{11}}{1 - e_{11}e_{22}} \quad (2.10)$$

From the match measurements the following can be obtained

$$S_{11MM} = e_{00} \quad (2.11)$$

$$S_{22MM} = e_{33} \quad (2.12)$$

Multiplying equations (2.9, 2.10) by each other and substituting equations (2.7, 2.8) into the resultant product and simplifying yields,

$$e_{11}e_{22} = (S_{11MT} - e_{00})(S_{22MT} - e_{33})/S_{12MT} \cdot S_{21MT} \quad (2.13)$$

Rearranging equations (2.5, 2.6) for $e_{01}e_{10}$ and $e_{23}e_{32}$ yields,

$$e_{01}e_{10} = \frac{(S_{11MT} - e_{00})(1 - e_{11}e_{22})}{e_{11}e_{22}} \cdot e_{11} \quad (2.14)$$

$$e_{23}e_{32} = \frac{(S_{22MT} - e_{33})(1 - e_{11}e_{22})}{e_{11}e_{22}} \cdot e_{22} \quad (2.15)$$

Rearranging equations (2.7, 2.8) for $e_{23}e_{10}$ and $e_{32}e_{01}$ yields

$$e_{23}e_{10} = S_{21MT}(1 - e_{11}e_{22}) \quad (2.16)$$

$$e_{32}e_{01} = S_{12MT}(1 - e_{11}e_{22}) \quad (2.17)$$

From the reflect measurements the following equations can be obtained,

$$S_{11MG} = e_{00} + \frac{e_{01}e_{10} \cdot \Gamma_a}{1 - e_{11} \cdot \Gamma_a} \quad (2.18)$$

$$S_{22MG} = e_{33} + \frac{e_{23}e_{32} \cdot \Gamma_b}{1 - e_{22} \cdot \Gamma_b} \quad (2.19)$$

Solving equations (2.18, 2.19) for Γ_a and Γ_b yields,

$$\Gamma_a = \frac{S_{11MG} - e_{00}}{e_{11} \left(\frac{e_{01}e_{10}}{e_{11}} - e_{00} + S_{11MG} \right)} \quad (2.20)$$

$$\Gamma_b = \frac{S_{22MG} - e_{33}}{e_{22} \left(\frac{e_{23}e_{32}}{e_{22}} - e_{33} + S_{22MG} \right)} \quad (2.21)$$

Assuming that the reflect standards on both ports are similar to each other, therefore equating equations (2.20, 2.21) and solving for e_{11} yields,

$$e_{11} = e_{22} \frac{\left(\frac{e_{23}e_{32}}{e_{22}} - e_{33} + S_{22MG} \right) \cdot (S_{11MG} - e_{00})}{\left(\frac{e_{01}e_{10}}{e_{11}} - e_{00} + S_{11MG} \right) \cdot (S_{22MG} - e_{33})} \quad (2.22)$$

Substituting equation (2.13) into (2.22) and solving for e_{11} yields,

$$e_{11}^2 = \frac{\left(\frac{e_{23}e_{32}}{e_{22}} - e_{33} + S_{22MG} \right) \cdot (S_{11MG} - e_{00})}{\left(\frac{e_{01}e_{10}}{e_{11}} - e_{00} + S_{11MG} \right) \cdot (S_{221MG} - e_{33})} \cdot \frac{(S_{11MT} - e_{00})(S_{22MT} - e_{33})}{S_{12MT} \cdot S_{21MT}} \quad (2.23)$$

In order to solve equation (2.23) for e_{11} the magnitude of e_{11} can be revealed by taking its square root. The phase ambiguity can be solved by substituting e_{11} into equation (2.20) provided that the reflect type is specified prior to calibration. Having solved for e_{11} all error coefficients can be revealed.

2.5.3 Embedding and De-embedding Techniques

Embedding Techniques: If the calibration procedures are done in two tier steps (Fig. 2.10.a) then the equivalent error flow graph (Fig. 2.10.b) can be combined to form a single flow graph which includes the error coefficients from the two tier calibration (Fig. 2.10.c). Using flow graph analysis [37], the error flow graph model of Fig. 2.10.b can be converted into the error model of Fig. 2.10.c using the following set of equations,

Port 1:

$$e_{00} = e_{a00} + \frac{e_{a01}e_{a10}e_{b00}}{1 - e_{a11}e_{b00}}$$

$$e_{11} = e_{b11} + \frac{e_{b01}e_{b10}e_{a11}}{1 - e_{a11}e_{b00}}$$

$$e_{21} = \frac{e_{b10}e_{a10}}{1 - e_{a11}e_{b00}}$$

$$e_{12} = \frac{e_{a01}e_{b01}}{1 - e_{a11}e_{b00}}$$

Port 2:

$$e_{22} = e_{b22} + \frac{e_{b32}e_{b23}e_{a22}}{1 - e_{b33}e_{a22}}$$

$$e_{33} = e_{a33} + \frac{e_{a32}e_{a23}e_{b33}}{1 - e_{b33}e_{a22}}$$

$$e_{32} = \frac{e_{b32}e_{a32}}{1 - e_{b33}e_{a22}}$$

$$e_{23} = \frac{e_{b23}e_{a23}}{1 - e_{b33}e_{a22}}$$

Any combination of the above variables can be formed and used directly in the calibration procedure. This operation is called an embedding technique since one error model is embedded into another one to form a new error model.

De-embedding Techniques: De-embedding in this document is referred to as extracting the DUT actual s-parameters by de-embedding the calibration error coefficients from the DUT measured raw data. This technique is explained in detail in [34] and will be summarised here for completeness.

In any measurement system like the one shown in Fig. 2.10.a and in order to measure the four s-parameters, two measurement configurations are normally applied. First the energy is injected into port-1 of the system while terminating port-2 into a 50 Ohm load. This will reduce the measurement system error flow graph of Fig. 2.10.c to the error flow graph shown in Fig. 2.14 below; note that the leakage or isolation error term is included in this model for completeness.

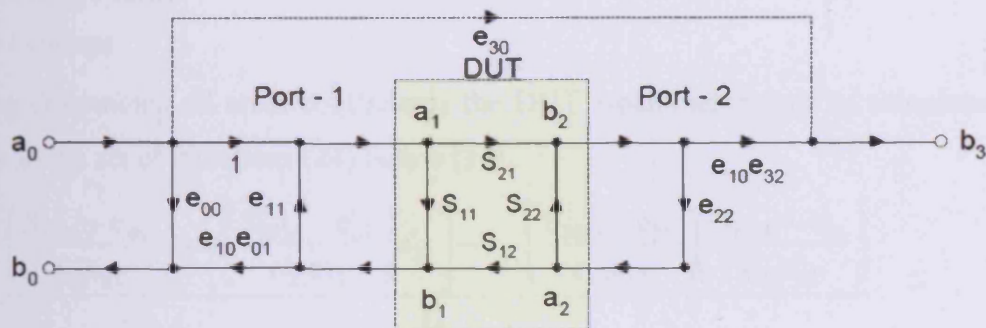


Fig. 2.14 Measurement system forward error flow graph

Where,

e_{00} = Directivity

e_{11} = Port-1 Match

$(e_{10}e_{01})$ = Reflection Tracking

$(e_{10}e_{32})$ = Transmission Tracking

e_{22} = Port-2 Match

e_{30} = Leakage

This measurement will reveal two DUT s-parameters namely S_{11M} and S_{21M} . In order to measure the other two s-parameters, namely S_{22M} and S_{12M} , the energy has to be injected into port 2 of the measurement system while terminating port-1 into a 50 Ohm load. This will reduce the measurement system error flow graph of Fig. 2.10.c

into the error flow graph shown in Fig. 2.15 below; note that the leakage or isolation error term is included in this model for completeness. The error terms in Fig. 2.15 are given slightly different notation to distinguish them from the forward error model terms.

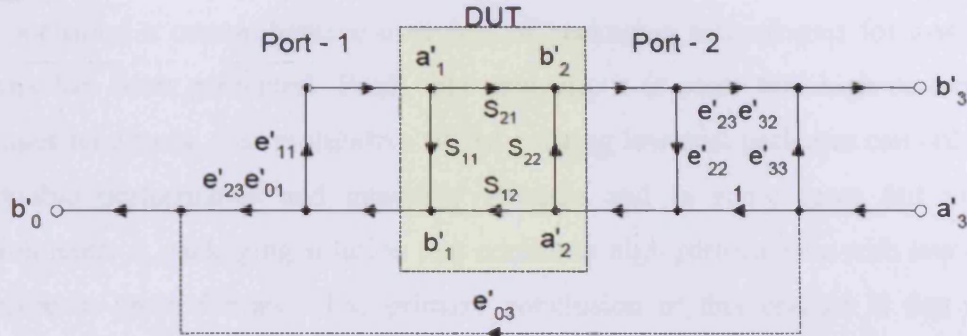


Fig. 2.15 Measurement system reverse error flow graph

Where,

e'_{33} = Directivity

e'_{11} = Port-1 Match

$(e'_{23}e'_{32})$ = Reflection Tracking

$(e'_{23}e'_{01})$ = Transmission Tracking

e'_{22} = Port-2 Match

e'_{03} = Leakage

Having determined all error coefficients the DUT s-parameters can be calculated as shown in the set of equations (24) below [34].,

$$S_{11} = \frac{\left(\frac{S_{11M} - e_{00}}{e_{10}e_{01}} \right) \left[1 + \left(\frac{S_{22M} - e'_{33}}{e'_{23}e'_{32}} \right) e'_{22} \right] - e_{22} \left(\frac{S_{21M} - e_{30}}{e_{10}e_{32}} \right) \left(\frac{S_{12M} - e'_{03}}{e'_{23}e'_{01}} \right)}{D}$$

$$S_{21} = \frac{\left(\frac{S_{21M} - e_{30}}{e_{10}e_{32}} \right) \left[1 + \left(\frac{S_{22M} - e'_{33}}{e'_{23}e'_{32}} \right) (e'_{22} - e_{22}) \right]}{D}$$

$$S_{22} = \frac{\left(\frac{S_{22M} - e'_{33}}{e'_{23}e'_{32}} \right) \left[1 + \left(\frac{S_{11M} - e_{00}}{e_{10}e_{01}} \right) e_{11} \right] - e'_{11} \left(\frac{S_{21M} - e_{30}}{e_{10}e_{32}} \right) \left(\frac{S_{12M} - e'_{03}}{e'_{23}e'_{01}} \right)}{D}$$

$$S_{12} = \frac{\left(\frac{S_{12M} - e'_{03}}{e'_{23}e'_{01}} \right) \left[1 + \left(\frac{S_{11M} - e_{00}}{e_{10}e_{01}} \right) (e_{11} - e'_{11}) \right]}{D}$$

$$D = \left[1 + \left(\frac{S_{11M} - e_{00}}{e_{10}e_{01}} \right) e_{11} \right] \left[1 + \left(\frac{S_{22M} - e'_{33}}{e'_{23}e'_{32}} \right) e'_{22} \right] - \left(\frac{S_{21M} - e_{30}}{e_{10}e_{32}} \right) \left(\frac{S_{12M} - e'_{03}}{e'_{23}e'_{01}} \right) e_{22}e'_{11} \quad (24)$$

The set of equations shown above will reveal the actual DUT four s-parameters after removing the system errors up to the calibration reference plane.

2.6 Summary

In this chapter a comprehensive overview of packaging technologies for low power devices has been presented. From this analysis, it is clear that high-performance packages tend to be cost prohibitive whilst existing low-cost packages can only offer reasonable performance and generally struggle and in some cases fail to meet requirements. A packaging solution that combines high performance with low cost is therefore in great demand. The primary conclusion of this chapter is that a new material; Liquid Crystal Polymer (LCP) laminate possesses excellent properties that make it suitable for the development of broadband, low-cost packages that are suitable for low power devices, hence it will be the focus of this thesis.

In order to properly characterise the developed low-power packages, it was necessary to develop an accurate and robust measurement system and multi-tier calibration characterization framework. The measurement system's flexibility enables it to measure the s-parameters of any device at any reference plane. This was achieved by performing a reference small-signal calibration using traceable calibration standards, followed by a sequence of further calibration stages (multi-tier), where the measurement reference plane is shifted to the desired reference plane.

2.7 References:

- [1] L. Larson and D. Jessie, "Advances in RF packaging technologies for next-generation wireless communications applications," *IEEE proceedings Custom Integrated Circuits Conference*, pp. 323 – 330, Sept. 2003.
- [2] D. Jassie and L. Larson, "An X-Band small outline leaded plastic package for MMIC applications," *IEEE Transactions on Advanced Packaging*, vol. 25, pp. 439-447, August 2002.
- [3] D. V. Retuta, B. K. Lim, and H. B. Tan, "Design and process optimization for dual row QFN," *Electronic Components and Technology Conference Proceedings, 56st*, pp. 1827-1835, 2006.
- [4] G. Pascariu, P. Cronin, and D. Crowley, "Next Generation Electronics Packaging Utilizing Flip Chip Technology," *IEEE/CPMT/SEMI 28th International Electronics Manufacturing Technology Symposium.*, pp. 423 - 426, July 2003.
- [5] S. Krishnamoorthi, D. Y. R. Chong, and A. Y. S. Sun, "Thermal Management and Characterization of Flip Chip BGA Packages," *Proceedings of Electronics Packaging Technology Conference.*, pp. 53 - 59, 2004.
- [6] W. Blood and A. Lai, "Early Analysis of Chip Scale Package Design Trade-offs," *IEEE Symposium on IC/Package Design Integration Proceedings*, pp. 64-69, 1998.
- [7] S. Chang, C. Cheng, L. Shen, K. Chiang, Y. Hwang, Y. Chen, J. Ko, H. Hu, K. Chen, and C. Chang, "A novel WLCSP technology with high reliability, low cost and ease of fabrication," *IEEE Electronic Packaging Technology Conference*, pp. 7-12, 2004.
- [8] T. Kamgaing, K. Ichikawa, X. Zeng, K. Hwang, Y. Min, and J. Kubota, "Future package technologies for wireless communication systems," *Intel Technology Journal*, vol. 9, 2005.
- [9] S. Chaparala, B. D. Rogermann, J. M. Pitarresi, and B. G. Sammakia, "Effects of geometry and temperature cycle on the reliability of WLCSP solder joints," *IEEE Transactions on Components and Packaging Technologies*, vol. 28, pp. 441 - 448, September 2005.
- [10] C. Liu, C. Lee, and K. Chiang, "Solder joints layout design and reliability enhancement of wafer level packaging," *Proceedings of the 6th International Conference on Thermal, Mechanical and Multi-Physics Simulation and Experiments in Micro-Electronics and Micro-Systems, 2005*, pp. 234 - 241, April 2005.
- [11] C. Yuan, C. Han, M. Yew, C. Chou, and K. Chiang, "Design, analysis, and development of novel three-dimensional stacking WLCSP," *IEEE Transactions on Advanced Packaging*, vol. 28, pp. 387-396, August 2005.
- [12] T. Kamgaing, K. Ichikawa, X. Y. Zeng, K.-P. Hwang, Y. Min, and J. Kubota, "Stacked Package-on-Package Technology for Improved 3D Integration," *Intel Technology Journal*, vol. 9, November 2005.
- [13] H. C. Huang, A. Ezzeddine, A. Darwish, B. Hsu, J. Williams, and S. Peak, "Ku-Band MMIC in low-cost, SMT compatible packages," *IEEE MTT-S International Microwave Symposium Digest, 2002*, vol. 1, pp. 27 - 30, June 2002.
- [14] K. Yoshida, T. Shirasaki, S. Matsuzono, and C. Makihara, "50 GHz Broadband SMT package for microwave applications," *Electronic Components and Technology Conference Proceedings, 51st*, pp. 744 - 749, 2001.

- [15] K. Fuji and H. Morkner, "A 6-30 GHz image-rejection distributed resistive MMIC mixer in a low cost surface mount package," *IEEE MTT-S International Microwave Symposium Digest*, pp. 4, June 2005.
- [16] M. Heijningen and G. Gauthier, "Low-cost millimetre-wave transceiver module using SMD packaged MMICs," *34th European Microwave Conference, 2004.*, vol. 3, pp. 1269 - 1272, October 2004.
- [17] K. Phan and H. Morkner, "A high performance yet easy to use low noise amplifier in SMT package for 6 to 20 GHz low cost applications," *34th European Microwave Conference*, vol. 1, pp. 365 - 368, October 2004.
- [18] A. Bessemoulin, M. Parisot, P. Quentin, C. Saboureau, M. Heijningen, and J. Priday, "A 1-Watt Ku-band power amplifier MMIC using cost effective SMD package," *34th European Microwave Conference*, vol. 1, pp. 349 - 352, October 2004.
- [19] M. Heijningen and J. Priday, "Novel Organic SMD package for high-power millimetre wave MMIC," *34th European Microwave Conference*, vol. 1, pp. 357 - 360, October 2004.
- [20] D. R. Decker, H. M. Olson, R. Tatikola, R. Gutierrez, and N. R. Mysoor, "Multichip MMIC package for X and Ka bands," *IEEE Transactions on components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging*, vol. 20, pp. 27-33, 1997.
- [21] L. Hyvonen and A. Hujanen, "A compact MMIC-compatible microstrip to waveguide transition," *IEEE MTT-S International Microwave Symposium Digest*, vol. 2, pp. 875-878, June 1996.
- [22] W. Simon, R. Kulke, A. Wien, M. Rittweger, I. Wolff, A. Girard, and J. P. Bertinet, "Interconnect and transitions in multilayer LTCC multichip modules for 24 GHz ISM-Band applications," *IEEE MTT-S International Microwave Symposium Digest*, vol. 2, pp. 1047 - 1050, June 2000.
- [23] D. Thompson, N. Kingsley, G. Wang, J. Paapolymerou, and M. M. Tentzeris, "RF characteristics of thin film liquid crystal polymer (LCP) packages for RF MEMS and MMIC integration," *IEEE MTT-S International Microwave Symposium Digest*, pp. 4, June 2005.
- [24] D. C. Thompson, O. Tantot, H. Jallageas, G. E. Ponchsk, M. M. Tentzeris, and J. Papapolymerou, "Characterization of liquid crystal polymer (LCP) material and transmission lines on LCP substrates from 30 to 110 GHz," *IEEE Transactions on Microwave Theory and Techniques*, vol. 52, pp. 1343 - 1352, April 2004.
- [25] Z. Wei and A. Pham, "Liquid crystal polymer (LCP) for microwave/millimetre wave multilayer packaging," *IEEE MTT-S International Microwave Symposium Digest*, vol. 3, pp. 2273 - 2276, June 2003.
- [26] H. Kanno, H. Ogura, and K. Takahashi, "Surface mountable liquid crystal polymer package with vertical via transition compensating wire inductance up to V-band," *IEEE MTT-S International Microwave Symposium Digest, 2003*, vol. 2, pp. 1159 - 1162, June 2003.
- [27] D. Nicholson, "Low return loss DC to 60 GHz SMT package with performance verification by precision 50 Ohm load," *European Microwave Conference*, vol. 1, pp. 157-160, October 2005.
- [28] J.-G. Yook, L. Katehi, R. N. Simons, and K. A. Shalkhauser, "Experimental and theoretical study of parasitic leakage/resonance in a K/Ka-band MMIC package."

- [29] G. F. Engen and C. A. Hoer, "“Thru-Reflect-Line:” An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer," *IEEE Transactions on Microwave Theory and Techniques*, vol. 27, pp. 987-993, December 1979.
- [30] D. Williams, C. M. Wang, and U. Arz, "An optimal multiline TRL calibration algorithm," *IEEE MTT-S International Microwave Symposium Digest, 2003*, vol. 3, pp. 1819 - 1822, June 2003.
- [31] R. B. Mark and D. Williams, "Characteristic impedance determination using propagation constant measurement," *IEEE Microwave and Guided Letters.*, vol. 1, pp. 141-143, June 1991.
- [32] D. Williams and R. B. Mark, "Transmission Line Capacitance Measurement," *IEEE Microwave and Guided Letters.*, vol. 1, pp. 243-245, September 1991.
- [33] R. B. Mark, "A Multiline Method of Network Analyzer Calibration," *IEEE Transactions on Microwave Theory and Techniques.*, vol. 39, pp. 1205-1215, July 1991.
- [34] D. Rytting, "Appendix to an analysis of vector measurement accuracy enhancement techniques," *Hewlett-Packard RF Microwave Symposium Digest*, pp. 1-42, March 1982.
- [35] Hewlett-Packard, "Agilent Network Analysis Applying the 8510 TRL Calibration for Non-Coaxial Measurements," *Product Notes 8510-8A*.
- [36] C. A. Hoer, "Choosing line lengths for calibrating network analyzers," *IEEE Transactions on Microwave Theory and Techniques*, vol. 83, pp. 76 - 78, January 1983.
- [37] D. M. Pozar, *Microwave Engineering*: John Wiley, ISBN 0-471-17096-8.

CHAPTER 3

DESIGN, REALIZATION AND MEASUREMENTS OF LAMINATE BASED LOW-POWER PACKAGES

This chapter addresses the design of low-power packages and their electrical performance. The designed packages are based on different laminate substrate materials with different via technologies. For completeness the package manufacturing process is also presented. Using the developed measurement system discussed in Chapter 2 of this thesis the packages were measured and package models have been extracted. Finally a thermal analysis of the optimized package was performed and presented.

3.1 Package Design Basis

The packages presented in this chapter originated from the unoptimized laminate based packages provided by Labtech at the project start. One of the measured packages is shown in Fig. 3.1, this prototype package consists of two 45 μm metallization layers (gold plated copper) separated by a 250 μm of RO4350 laminate (dielectric). Since the package is normally placed onto a mounting board there should be a way to transfer the ground energy to the package, hence a coplanar line structure is presented on the package bottom metallization layer. However a simple microstrip line referenced to the package ground plane is used to transfer the energy from the mounting board to the MMIC using normal through via technology. The MMICs normally sit in the package cavity and are bonded to the package signal lines. The MMIC ground is normally fed through straight bonding to the package solid gold plated copper cavity. Both package metallization layers are connected to each other using straight through hole vias.

The package transmission line configuration described above will stay almost the same throughout the low power package design and development process since it represents a standard which has to be implemented while varying other parameters to improve the package performance.

Note that three DC bias feeds were provided on each package sides and isolated from the RF path by a ground ring.

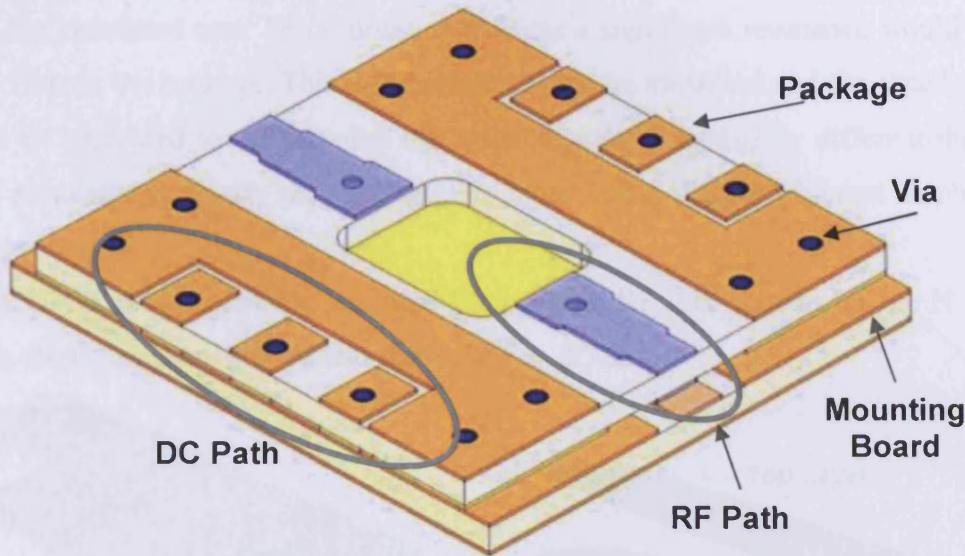


Fig. 3.1 Labtech package prototype HFSS representation

Measurements were performed on the open port package shown in Fig. 3.1 with the package mounted onto a mounting board. The mounting board was calibrated up to the package plane using a TRL calibration procedure, thus the 8510 Vector Network Analyzer (VNA) measures the package open (reflect) response. For that measurement the Anritsu test fixture (Fig. F.2 in Appendix F), which can go up to 40GHz (max) was used to launch to the mounting board structures. The package and the mounting board underneath were simulated using Ansoft HFSS and the simulation results are compared to the measured response as shown in Fig. 3.2 below.

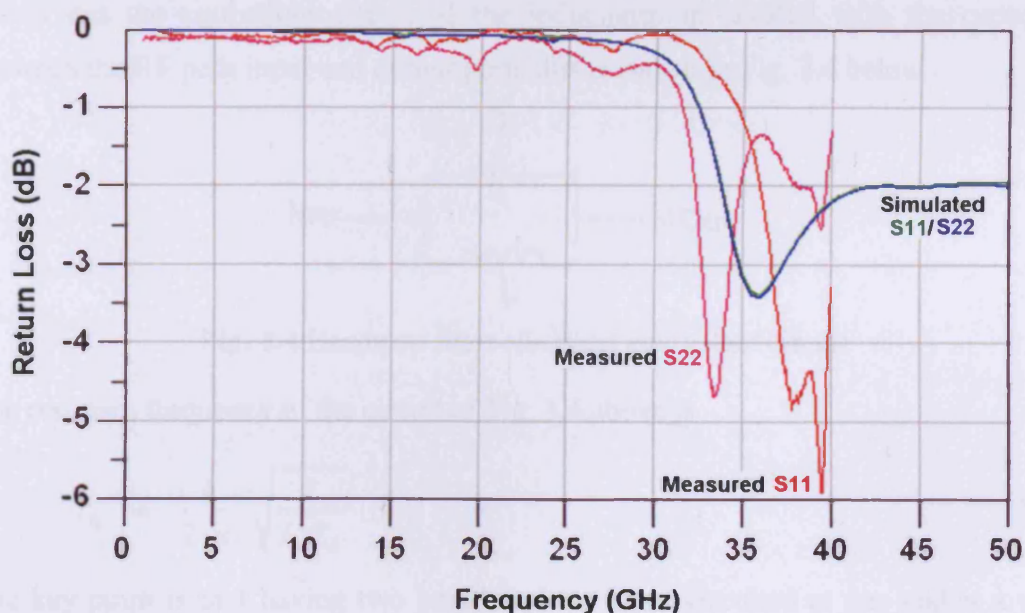


Fig. 3.2 Simulated and measured response of Labtech package of Fig. 3.1

The measured results shown in Fig. 3.2 above clearly confirm that the package has resonances that could be seen in the measured S_{11} and S_{22} but shifted in frequency from the simulated one. The simulation predicts a significant resonance would occur at 35 GHz in the package. This difference between the measured and simulated results could be attributed to the fact that the realised package is slightly different than the ideal simulated one with the package two sides being slightly different in physical dimensions.

Using HFSS it is possible to examine the package RF feed section for the H and E fields, these fields are plotted and shown in Fig. 3.3 below.

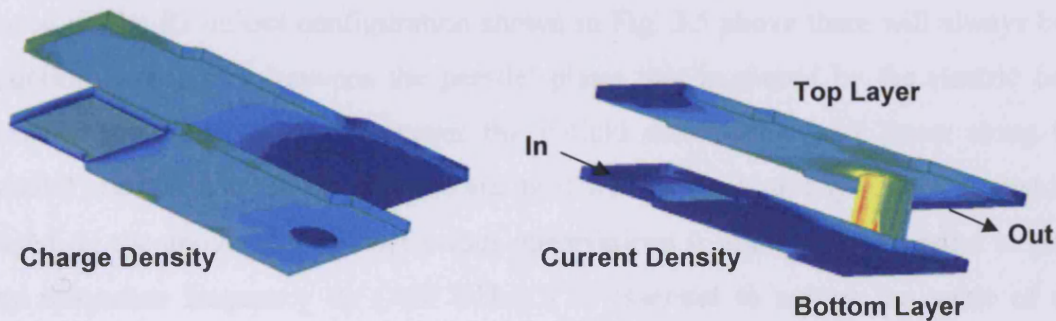


Fig. 3.3 Charge and Current densities for Labtech package RF feed lines

It is clear from the charge and current densities shown above that the package top and bottom feed lines are strongly coupled (E-field) which emulate the capacitance effect, on the other hand the via itself has large current density which can act as an inductance.

This configuration suggests that the RF feed section is acting as a bandstop resonator which has the equivalent circuit of the inductance in parallel with the capacitor between the RF path input and output ports this is shown in Fig. 3.4 below.

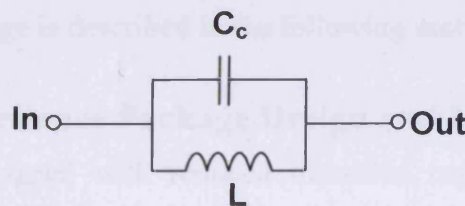


Fig. 3.4 Bandstop filter electrical equivalent circuit

The resonant frequency of the circuit of Fig. 3.4 above is

$$f_o = \frac{1}{2\pi} \sqrt{\frac{1}{LC_c}} \quad (3.1)$$

The key point is that having two parallel plates short circuited at one end is a very complicated structure in terms of analyzing any capacitance and/or inductance

associated with it. In order to understand the problem further consider the structure shown in Fig. 3.5 below, where two parallel plates are connected to each other at one end by a via.

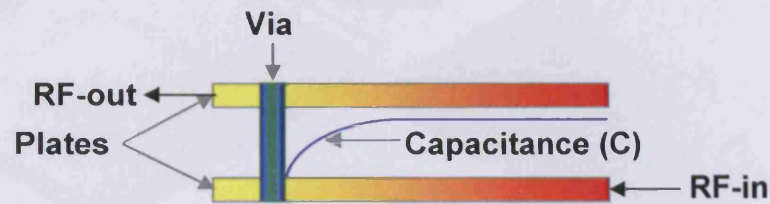


Fig. 3.5 Coupling capacitance distribution across parallel plates short circuited at one end

Based on the RF-in-out configuration shown in Fig. 3.5 above there will always be a coupling capacitance between the parallel plates that is caused by the electric field between these two plates. However the E-field distribution isn't linear along the parallel plates due to the fact that the via itself will short circuit any E-field around it. Based on the above package behaviour observations it is clear that in order to push any resonance frequency up (>50 GHz) it is essential to reduce the value of via inductance (L) and/or the RF path coupling capacitance (C_C) associated with the basic RF transition model of Fig. 3.4. The inductance associated with the via is unique and solely dependant on the via shape (geometry) and the pad rings around it. However, the exact dimensions of the via itself are governed by certain manufacturing rules. Therefore, control over the inductance associated with the via might be limited. As a first step towards optimising the RF transition a new package was designed with reduced coupling capacitance effect. This design was also used to verify the multi-tier calibration procedures and package model extraction presented in the previous chapter. The new package is described in the following section.

3.2 Reduced Capacitance Package Design and Measurement

New package was designed with reduced transition capacitance where the only overlap permitted between the package top and bottom metallization layers was around the via or what is so called the via pad rings, this is shown in Fig. 3.6 below,

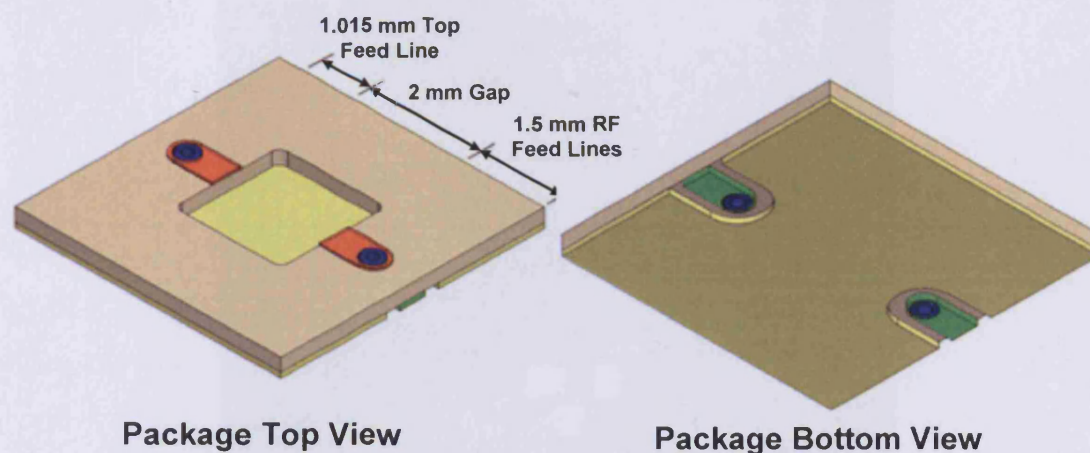


Fig. 3.6 Reduced coupling capacitance package

The package of Fig. 3.6 is made of $250\ \mu\text{m}$ thick of RO4350B laminate with $45\ \mu\text{m}$ gold plated metallization layers. The package consists of $50\ \Omega$ microstrip line on the package top metallization layer which is connected to the bottom $50\ \Omega$ coplanar transmission line using a normal through via, the package dimensions are shown in table 3.1 below.

Package Component	Dimension
Top microstrip line width	$550\ \mu\text{m}$
Bottom coplanar signal line width	$480\ \mu\text{m}$
Bottom coplanar line signal to ground spacing	$250\ \mu\text{m}$
Via radius	$150\ \mu\text{m}$
Via anti-pad ground radius	$490\ \mu\text{m}$
Via top pad radius (R_{top})	$275\ \mu\text{m}$
Via bottom pad radius (R_{Bottom})	$240\ \mu\text{m}$

Table 3.1 Package of Fig. 3.6 dimensions

The objective was first to make the via as big as possible to reduce its inductance and second and most importantly is to eliminate any unnecessary parallel plates which can introduce coupling effect. The package was verified at the design stage through the full EM simulation using HFSS for one package side ($1.5\ \text{mm}$ RF feed lines in Fig. 3.6).

The above package was manufactured and measured using a suitable mounting board that was fabricated to hold this package and to launch to it from its coplanar side. A set of mounting board TRL calibration standards were fabricated to help reach the package reference planes. The measurement system of Fig. 3.7 and Fig. 2.10 was used to measure the above package. This measurement system was calibrated in three calibration steps (tiers) as discussed in “*Setup-1*” of section 2.5 of this thesis.

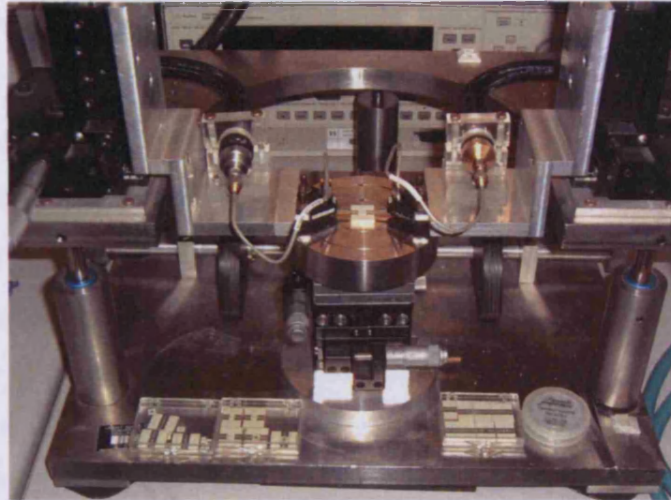


Fig. 3.7 Probe based measurement system used to measure the package of Fig. 3.6

The first calibration step (tier) involved using on-wafer (Picoprobe) calibration standards to calibrate the Vector Network Analyser (VNA) up to the probes tips using TRM calibration procedure. The second calibration step (tier) involved calibrating the measurement system up to the package reference plane using mounting board calibration standards and TRL calibration algorithm [1, 2].

The last calibration step (tier) involved calibrating the package itself (i.e. extracting the error coefficients of the package itself) to generate true package s-parameters. This is done using in-package calibration standards and TRL calibration procedures (Fig. 3.8).

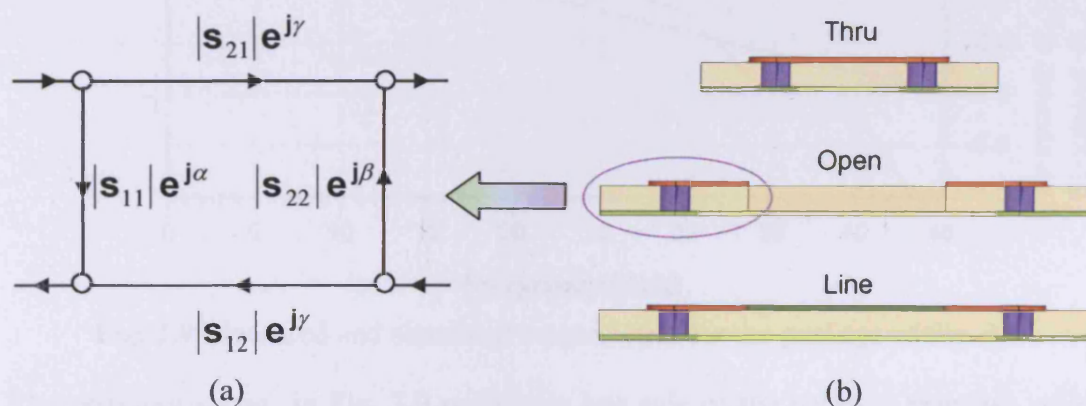


Fig. 3.8 (a) One package side error flow graph (s-parameters), (b) In package TRL calibration standards

From the TRL calibration (3rd tier) step a complete error model for the package was extracted, representing the actual package s-parameters. One draw back of this method of characterization is the fact that the actual insertion loss of the package is

not available as an independent parameter, but always as the product $|s_{21}| |s_{12}| e^{j2\gamma}$ (Transmission Tracking Coefficient) of s_{21} and s_{12} parameters.

In order to extract the insertion loss of the package the square root of the transmission tracking coefficient should be taken to obtain $\pm |s_{21}| e^{j\gamma}$. The resulting sign ambiguity can be resolved using the properties of the lossless reciprocal network [3]. The full analysis is presented in appendix B of this thesis.

Once the phase is decided, then the package s-parameters are available and can be readily imported into a CAD program (e.g. Advanced Design System-ADS) as a measurement based model, allowing its use within the design process of the MMIC. Having performed the above procedures, the actual s-parameters for one side of the package were measured and compared to HFSS simulation results as shown in Fig. 3.9 (note that the package and the mounting board were included in the EM-simulation).

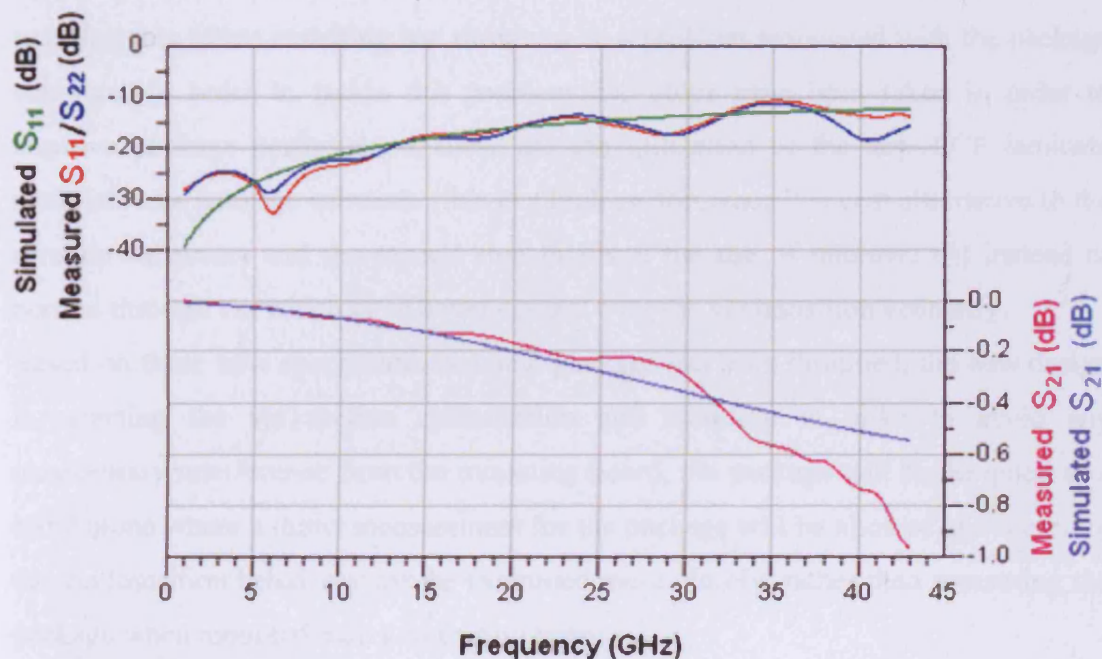


Fig. 3.9 Measured and simulated s-parameters for the package of Fig. 3.6

The response shown in Fig. 3.9 represents one side of the package response which goes up to 43 GHz (unfortunately the probes used at this stage couldn't make it to 50 GHz). It is clear from Fig. 3.9 that no resonances occurred over a wide frequency bandwidth which indicates that reducing the coupling capacitance effect had an impact in eliminating the resonances within the bandwidth of interest. However one can observe that the package has a moderated input and output match over a wide bandwidth, while the package insertion loss (S_{21}) starts to degrade beyond 30 GHz.

This is mainly due to a matching problem which comes from two sources, first the via transition mismatch and second the mounting board to package mismatch.

Since the new package has sustained a moderate response over quite a wide bandwidth, the focus from now on will be on providing a good matching all the way through from the mounting board up to the point where the device will be placed. Matching of the via transition to the connecting transmission lines represents one of the biggest design challenges. The next section deals with the via transition analysis, design and optimisation but implemented in the new cutting edge technology material namely Liquid Crystal Polymer (LCP) rather than previous laminate.

3.3 LCP Package Design and Modelling

It is clear from previous sections that the coupling capacitance associated with the via section transition can limit package performance, therefore reducing any parallel plate capacitance around the via transition section has shown to be a valid approach. While reducing this effect matching has shown to be a problem associated with the package structure. In order to tackle this problem two steps have been taken in order to improve package performance, these are the utilization of the new LCP laminate materials as a package substrate (this is a high performance low cost alternative to the ceramic substrate) and the second step involved the use of microvia [4] instead of normal through via which gave better control over the via transition geometry.

Based on these new specifications a new package has been designed, the new design is targeting the via section optimisation and therefore in order to avoid any unnecessary interference from the mounting board, the package will be designed as a stand alone where a direct measurement for the package will be allowed and therefore the via transition behaviour can be examined more closely, rather than measuring the package when mounted onto a mounting board.

Its worth mentioning that unlike other package technologies, for a $5 \times 5 \text{ mm}^2$ package a $2 \times 2 \text{ mm}^2$ cavity (Fig. 3.10) was introduced inside the dielectric for the direct mounting of MMICs die onto the solid bottom gold plated copper layer. This technique provides excellent thermal dissipation, thus eliminating the need for thermal vias and consequently reducing the package cost even further.

From the electrical point of view it is desirable to design a package with an all-pass filter characteristic with very low losses whilst introducing minimum interruption in the signal flow during the transition between the package top and bottom

metallization layers. Keeping that in mind a new package was designed (Fig. 3.10) which consists of 100 μm of LCP laminate (Rogers ULTRALAM3000/Rflex3000, D.K.=2.9, $\tan\delta=0.0025$) and two layers of metallization; the bottom plane consisting of a coplanar waveguide with 50 Ohm characteristic impedance from which the on-wafer probes will be launched to the package. On the top plane a 50 Ohm microstrip line is connected to the bottom plane using a micro via. The gold plated copper thickness on the package top and bottom is 45 μm and 100 μm respectively.

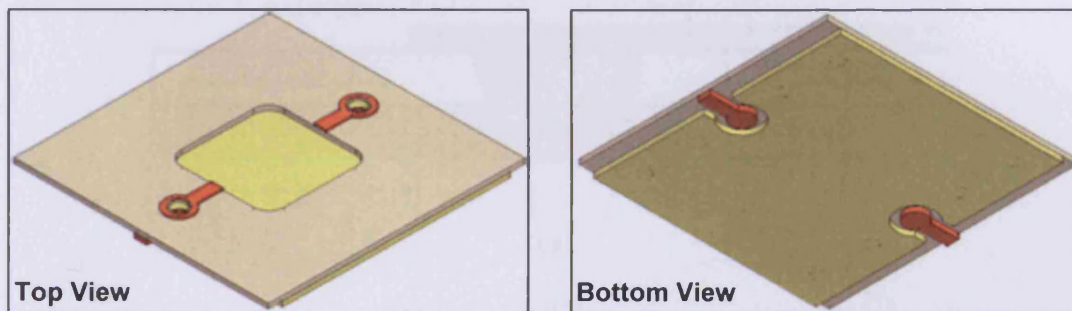


Fig. 3.10 Proposed thermally and electrically enhanced LCP package layout

Two important features have been added in the design of this package. These are the deliberate introduction of the via pad rings on the via top and bottom sides which provide a capacitance to ground effect. The other feature is the utilisation of the micro via which offset the via top and bottom pad rings from each other to minimise the coupling capacitance (C_C) effect between them.

Before reaching the final design of this package, a few modelling and optimisation steps were performed which established the design methodology for this kind of packages. The design methodology states that transmission lines are broadband in nature, therefore designing a package which emulates the function of a transmission line is preferred. Therefore a package which has an equivalent circuit similar to the transmission line electrical circuit may help improve the package performance and to make it work over large frequency bandwidth with minimum loss.

In an attempt to make a package which behaves like a transmission line, the package described above could be mapped into an equivalent circuit model similar to that of a transmission line. The unit cell model of a transmission line consists of either a cascade of T- or π -section networks of capacitances and inductances producing an all-pass filter. The cascade of networks can be extended through additional similar T- or π -sections without decreasing the bandwidth of the resulting new network. Thus,

matching the equivalent circuit model of the package to the equivalent circuit of the transmission line may ensure a minimal effect on the signal flow.

A small signal circuit model for the package structure of Fig. 3.10 (which is shown in detail in Fig. 3.11) can be derived (Fig. 3.12). The floating transmission line (T_1) at the bottom plane represents the launching point from a coplanar mounting structure where the signal starts to propagate to the package signal line.

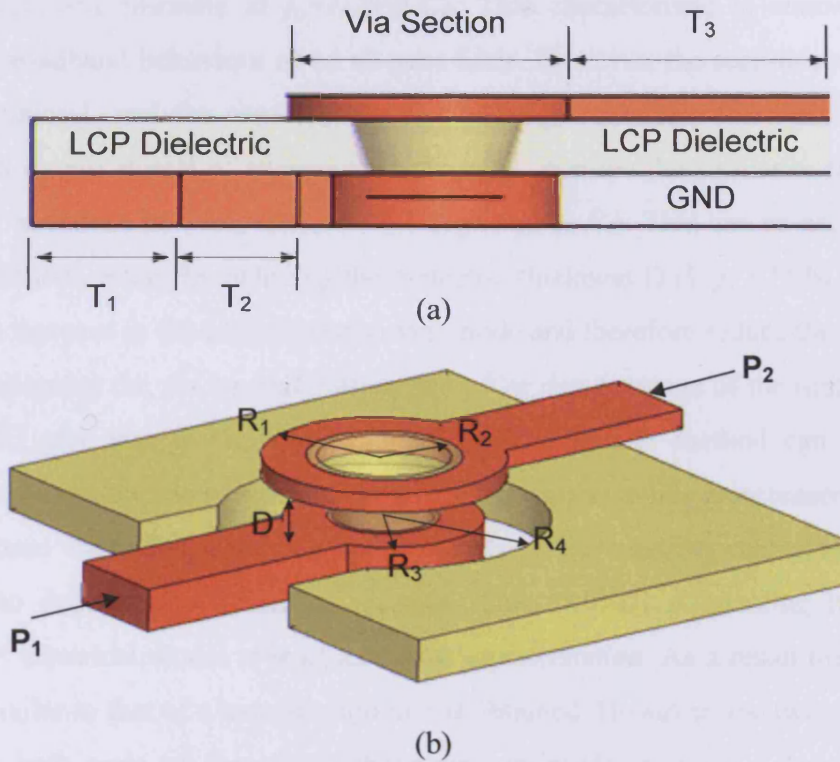


Fig. 3.11 One side of the LCP package (a) 2D representation, and (b) 3D representation. The coplanar transmission line T_2 represents the stage where ground energy will be transferred from the mounting board to the package ground structure, this line has a 50 Ohm characteristic impedance. This line in turn is connected through a via structure to 50 Ohm microstrip line T_3 on the top layer. Based on the package geometry shown in Fig. 3.11, a simple equivalent circuit can be derived (Fig. 3.12),

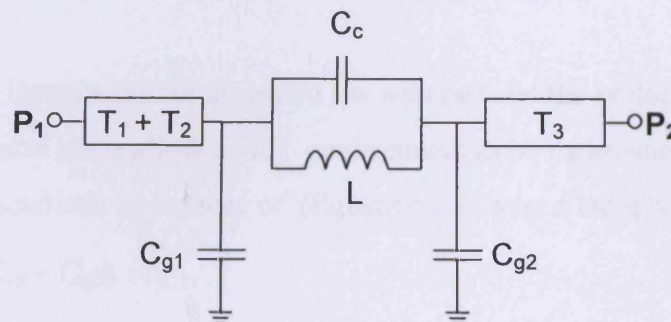


Fig. 3.12 Package equivalent electrical circuit

Here the via was modelled as an inductance in parallel with a capacitance, with the inductance L coming from the via's inductance, whilst the coupling capacitance C_C comes from the coupling between the top and bottom pads around the via. The capacitances to ground C_{g1} and C_{g2} represent the coupling of the bottom and top via pads to the ground plane respectively.

Within the resulting model, the parallel combination of L and C_C forms a bandstop filter which will resonate at $f_o = 1/2\pi\sqrt{LC_C}$. This characteristic is contrary to the required broadband behaviour of an all-pass filter. However, the section consisting of the inductance L and the capacitances C_{g1} and C_{g2} resembles the π -section of the equivalent circuit model of transmission line. To increase the similarity further it is important to reduce or even eliminate the capacitance C_C . This can be accomplished by two methods, either by reducing the dielectric thickness D (Fig. 3.11.b) which will lead to an increase in the capacitance's even mode and therefore reduce the odd mode, or by misaligning the via top and bottom pads. The disadvantage of the first method is that it will give rise to the capacitance C_{g2} . The second method can readily be achieved through the use of a micro via where the top via radius is increased relatively to the bottom via radius. Applying both methods on the coupling capacitance C_C it is possible to dramatically decrease its value, thus virtually eliminating it from the equivalent electrical model at least as a first approximation. As a result the simple π -section similar to that of a transmission line is obtained. However, the two capacitance values at both ends of the via, without any optimisation, yield a low-pass filter characteristic.

The capacitances C_{g1} and C_{g2} were formed by the introduction of two additional features within the LCP package; firstly the ground plane at the bottom layer and secondly the pads at the bottom and top layer connecting the micro via to the transmission lines T_2 and T_3 . Both can be controlled by either varying the gap between the bottom via pad and the ground plane ($R_4 - R_3$) and/or by varying the top via pad radius.

Conclusively, the introduction of the micro via with pads on the bottom and top layers as well as the ground plane allow a 50Ω environment to be maintained across the via section with characteristic impedance of (Equation 3.2) over a large bandwidth [3].

$$Z_o = \sqrt{L/(C_{g1} + C_{g2})} \quad (3.2)$$

In contrast to conventional through vias [5] the micro vias [4] can help miniaturise the package, allow hermicity (multi-layer) and also results in better control of the impedance of the via transition. However separating the via section components and simulating its parts individually is a very difficult task since there is no guarantee that when putting the components back together to form the via the components will behave similarly to when they are separated. Indeed, there is a very complex interaction between the via section components. Nevertheless, the above model provides a good understanding of package via component behaviour, interaction and how critical they are in the final package design.

To demonstrate the above procedures, the via section of the package presented in Fig. 3.10 has been split into individual components in order to extract the via components inductance and capacitances as shown in Fig. 3.13 below,

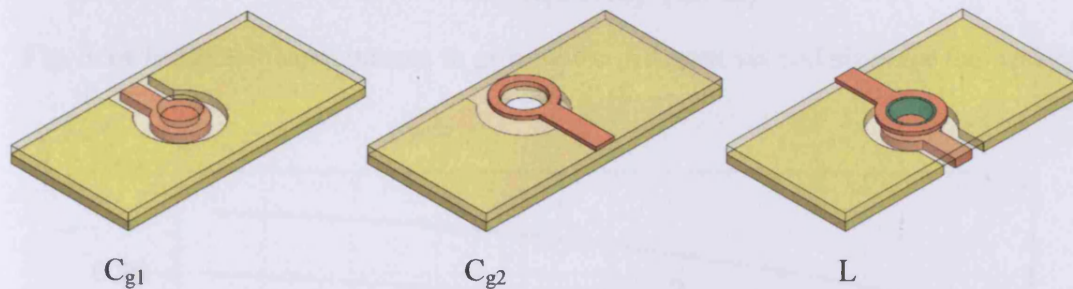


Fig. 3.13 HFSS representation for the via-section components of Fig. 3.10

The capacitances to ground can be extracted by simulating the via pad rings on their own as shown in Fig. 3.13, HFSS was used to simulate these structures for their s -parameters then these were converted into y -parameters from which the equivalent capacitances were extracted. For the inductance part the full via transition was used in the simulation, again 2-port s -parameters were converted into y -parameters from which the equivalent inductance was extracted.

Several via and via pad sizes were simulated and the equivalent capacitances and inductances were extracted as shown in Fig. 3.14 and Fig. 3.15 respectively. It is clear from these results that the via pads capacitance is increasing with increasing frequency due to package discontinuities (e.g. corners, sharp edges, etc...), also it indicates that the simulated structure is starting to behave as distributed element.

Similarly, the via inductance is decreasing with increasing frequency. One of the reasons for this inductance decrease is the effect of the via structure coupling capacitance to ground, the other reason is that at increasing frequency the flux linkage decreases due to skin depth effect (skin depth decreases as frequency increases).

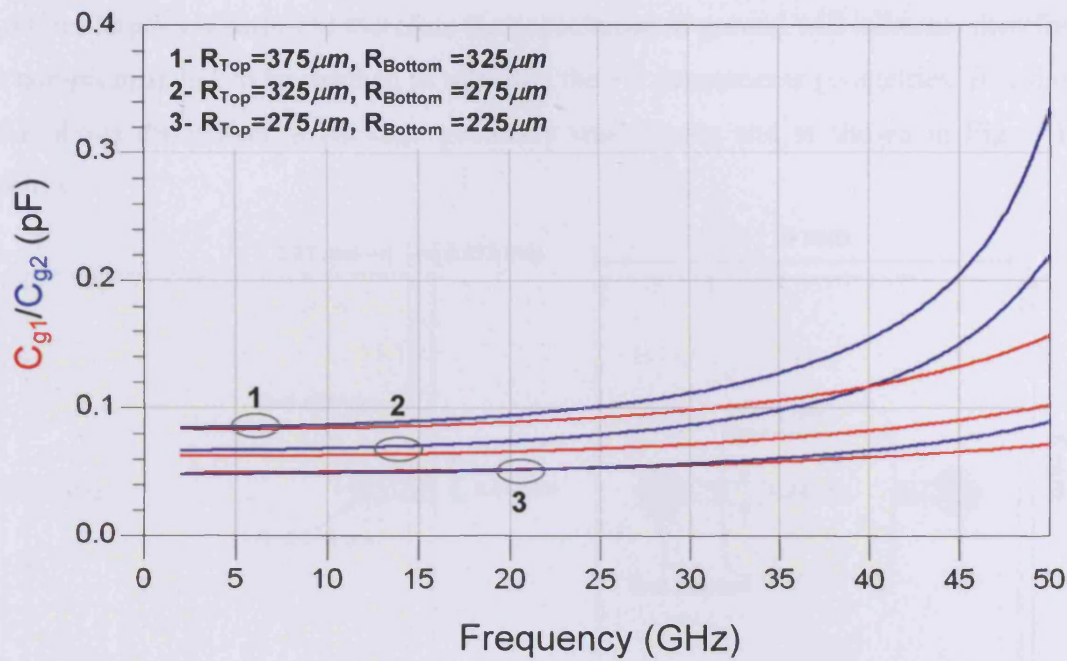


Fig. 3.14 Extracted capacitances to ground for different via pad sizes for the package of Fig. 3.10

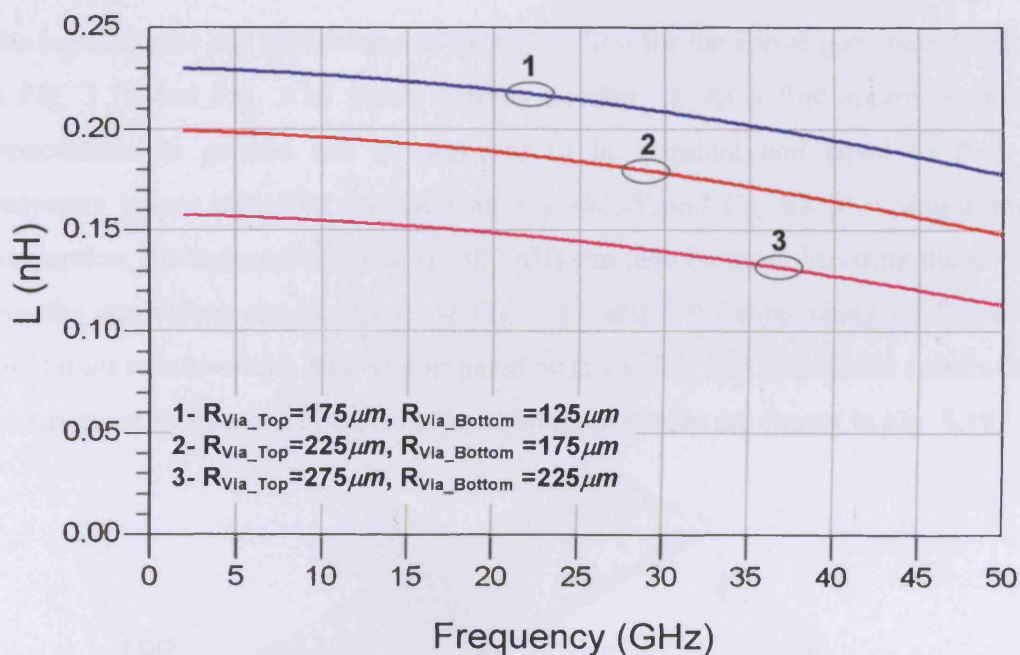


Fig. 3.15 Extracted inductance for different via sizes for the package of Fig. 3.10

It is desirable to make the via top and bottom pads capacitances to ground equal to each other ($C_{g1}=C_{g2}$). From the design perspective in order to increase the transition bandwidth it is desired to reduce the via inductance as well as the capacitance to ground while maintaining the relation between them using the impedance equation (3.2). The via inductance can be reduced by increasing its diameter however this

implies larger via pads and therefore the capacitance to ground will increase, therefore a compromise has to be reached in selecting the via components geometries. Based on the above discussion, a package geometry was chosen and is shown in Fig. 3.16 below.

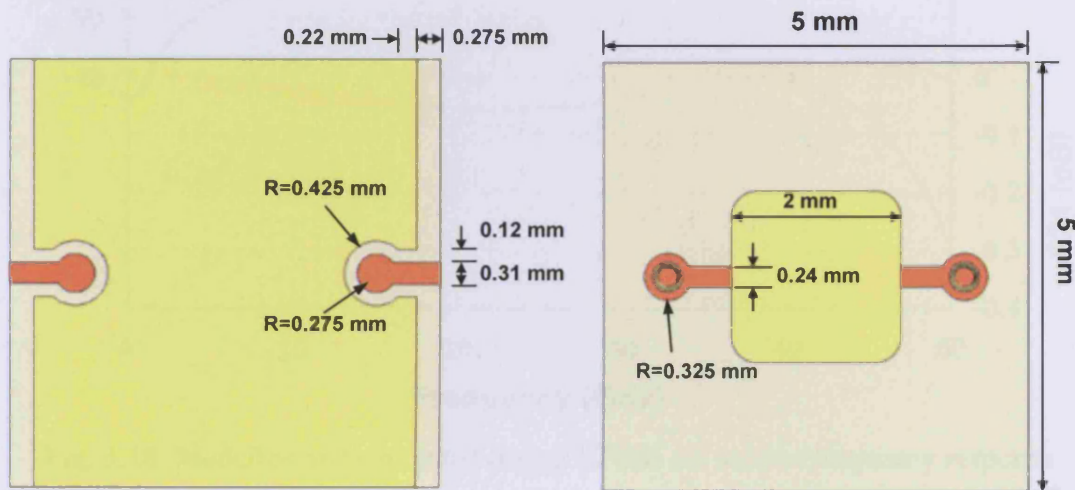


Fig. 3.16 LCP package of Fig. 3.10 dimensions

The capacitances and inductance of the via section for the above geometry are shown in Fig. 3.14 and Fig. 3.15 above (curves number 2). As a first approximation the capacitances to ground can be assumed to be constant and equal to their low frequency values which in this case are $C_{g1}=62$ fF and $C_{g2}=68$ fF. Using a similar assumption, the inductance value ($L=0.2$ nH) can also be used. Inserting these values into the equivalent circuit model of Fig. 3.12 and simulating using ADS provides simulation results which can be compared with the full EM simulation results of the via structure on its own (Fig. 3.17), the simulation results are shown in Fig. 3.18.

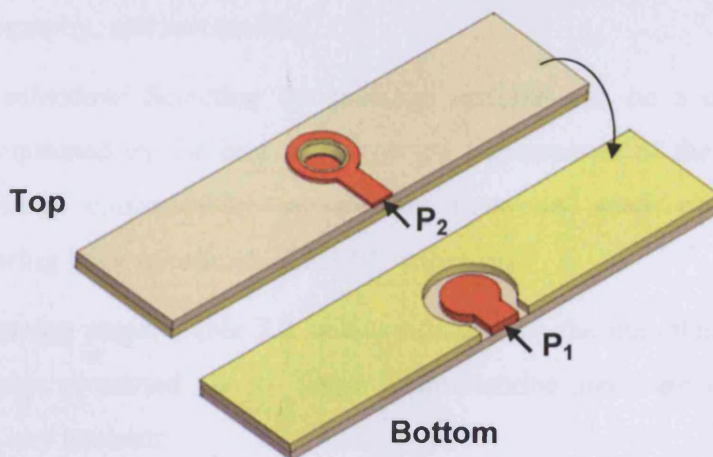


Fig. 3.17 One side LCP package representations using HFSS

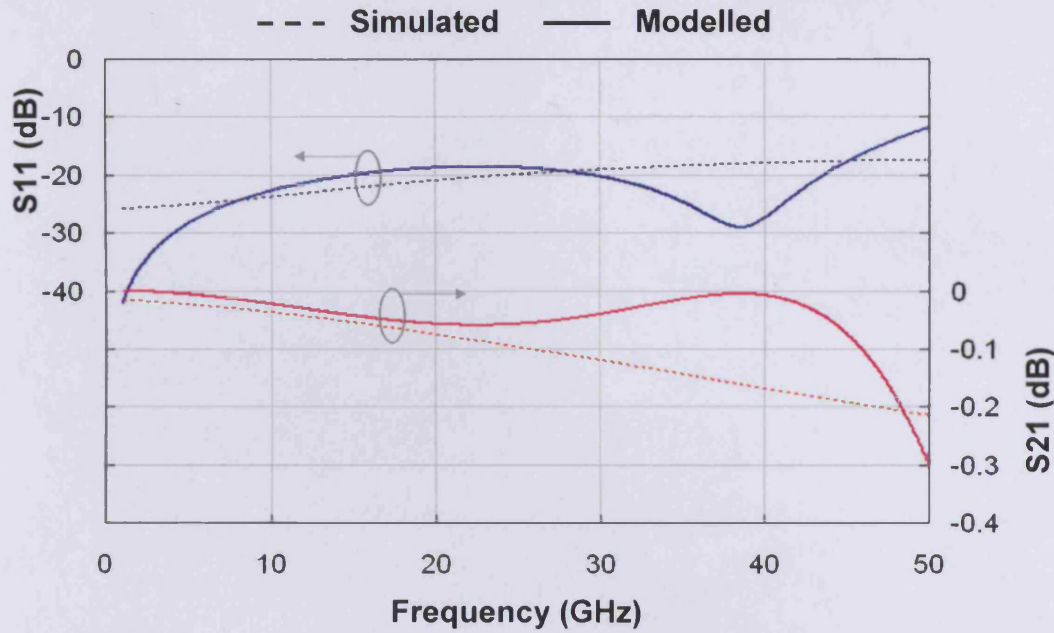


Fig. 3.18 Modelled and simulated (using HFSS) via section frequency response

The results above show reasonable response for the via section, however this is yet to be confirmed by the package measurement presented later on in this chapter. The following sections deal with the manufacturing and measurement techniques used to fabricate and measure the above package design.

3.4 Package Realization

Realizing a package can be achieved using a multitude of different approaches. Regardless of the process, the laminate to be used as a substrate should be chosen first, and subsequent steps will involve the processing of this laminate to form the package features. Package processing may include Laser machining, photolithography, and wet etching.

Material selection: Selecting the package material can be a difficult task and is usually dominated by the cost and expected performance of the final package. The manufacturing compatibility is another issue in need of consideration for manufacturing large quantities of MMIC packages.

Manufacturing steps: Table 3.2 below summarizes the manufacturing steps for the LCP package presented above. These manufacturing steps are versatile and can be applied to any laminate.

Seq	Process	Explanations
1	Laser Drill blind vias	Drill the vias using laser machine
2	Plasma	Pre-treatment process to clean the holes
3	Electroless plate	Add a thin layer of copper to the via
4	Flash Cu	Electroletic copper to add more copper to the via wall
5	Laminate photo-resist	Apply the photo resist
6	Expose top Layer	Expose the photo resist to define top copper pattern
7	Develop	Develop the photo resist
8	Top pattern plate	Add copper and flash of tin to the top tracks and vias
9	Strip Resist	Remove photo resist
10	Laminate photo-resist	Apply the photo resist
11	Expose	Expose photo resist to define bottom copper pattern
12	Develop	Develop the photo resist
13	Bottom pattern plate	Add copper and flash of tin to the bottom tracks
14	Strip Resist	Remove photo resist
15	Etch both sides	Chemically etch copper to define conductors
16	Strip Sn	Chemically remove tin
17	Laser pocket	Form MMIC pocket in LCP through to copper
18	Universal plate	Coat all copper surfaces with Ni Pd and Au
19	AOI	Inspect pattern using automatic optical inspection
20	Laser profile Array	Cut outer profile of package
21	Clean	Remove any debris
Supplied by kind permission of Labtech Ltd		

Table 3.2. LCP package manufacturing steps

3.5 LCP Package Measurement

The package presented above was manufactured by Labtech Ltd with a set of TRL calibration standards built in (Fig. 3.19). A measurement system similar to the one presented in chapter 2 of this thesis was used. For this measurement a 2-tier calibration approach was implemented where in 1st-tier the measurement system was calibrated up to the probes tips using on wafer TRM calibration standards.

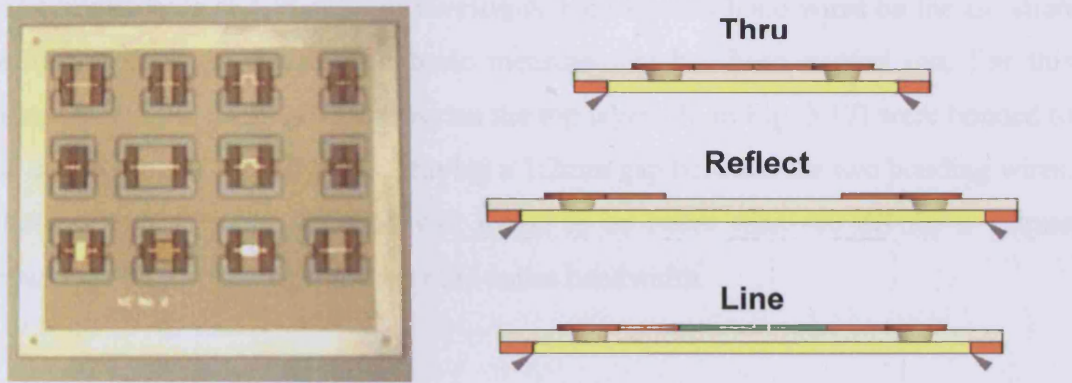


Fig. 3.19 In-package TRL calibration standards

The 2nd tier involved TRL calibration [2] using in-package calibration standards, these calibration standards consist of the package itself for the open standard and packages with a modified geometry to realize the thru and line standards.

From the TRL calibration (2nd tier) and by using the lossless reciprocal network analysis presented in appendix B of this thesis a complete error model for the package was obtained. Having performed the above procedures, the actual s-parameters for one side of the package were measured and compared to the simulation results as shown in Fig. 3.20 below,

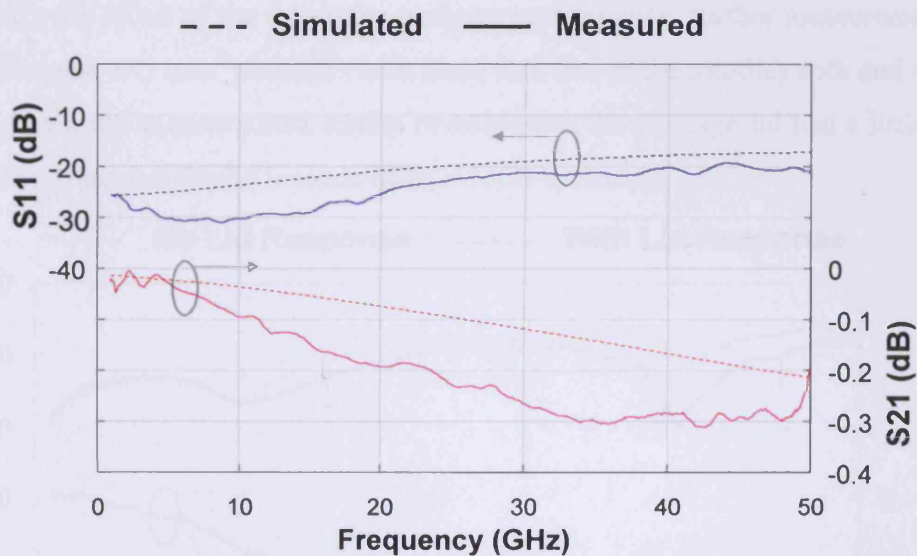


Fig. 3.20 Measured and simulated s-parameters for the package of Fig. 3.16

From these measurement results (Fig. 3.20) it can be seen that this package is behaving very well but degrading with increasing frequency. The package has sustained 20 dB of return loss and 0.3 dB insertion loss up to 50 GHz. Comparing the measured results to the corresponding simulated data shows good agreement.

For completeness and in order to investigate the effect of bond wires on the isolation performance of the package, a basic measurement has been carried out. For this measurement the package feed lines on the top layer (P2 in Fig. 3.17) were bonded to the cavity ground on both sides, leaving a 1.2mm gap between the two bonding wires. The resulting package isolation was found to be better than -40 dB for a 1.2mm separation distance (Fig. 3.21) over the entire bandwidth.

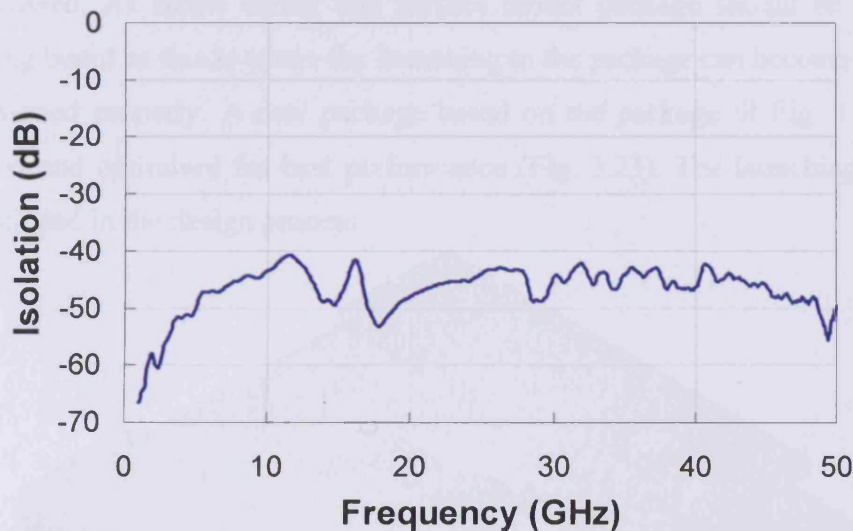


Fig. 3.21 Package isolation measured with bond wires to ground

To identify the effect of the lid on the package performance, further measurement was carried out on a $5 \times 5 \text{ mm}^2$ package (with 2mm thru line in the middle) with and without the lid. Again, the measurement results revealed that the package lid had a little effect (Fig. 3.22). Note that the lid is made of RO4350B dielectric.

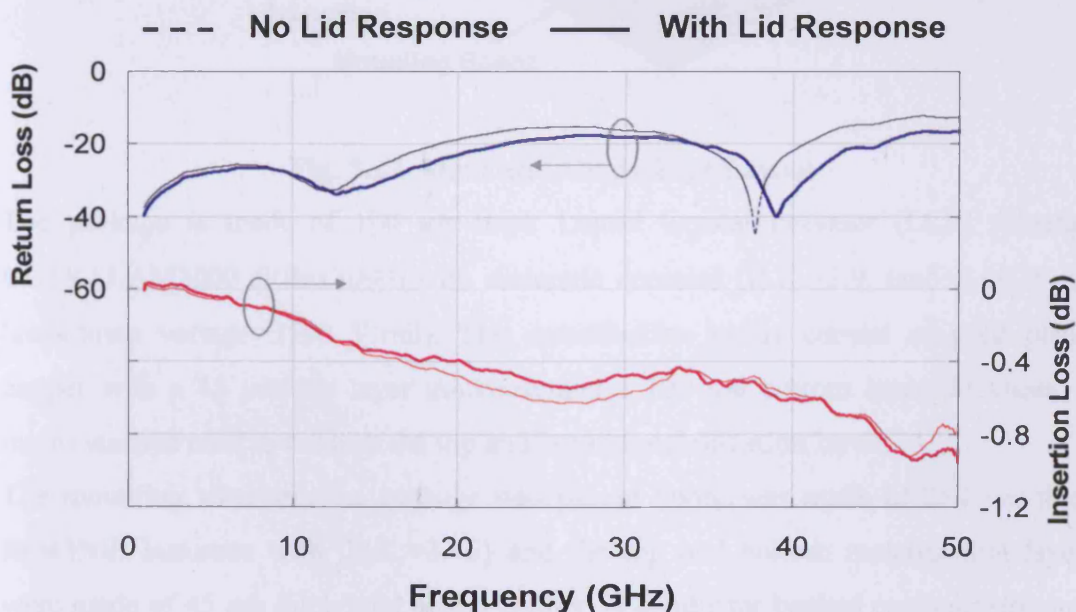


Fig. 3.22 Package performance with and without the lid

The above package performance is very promising; however the package has to be mounted onto a mounting structure in order for it to be used in the end application, the following section deals with the mounting issue.

3.6 LCP Package Design with Launching Structure

In this section the design of a complete package with cutting edge performance will be discussed. As stated earlier any surface mount package should be placed on a mounting board as this is where the launching to the package can become a problem if not designed properly. A new package based on the package of Fig. 3.10 has been designed and optimised for best performance (Fig. 3.23). The launching structure is also included in the design process.

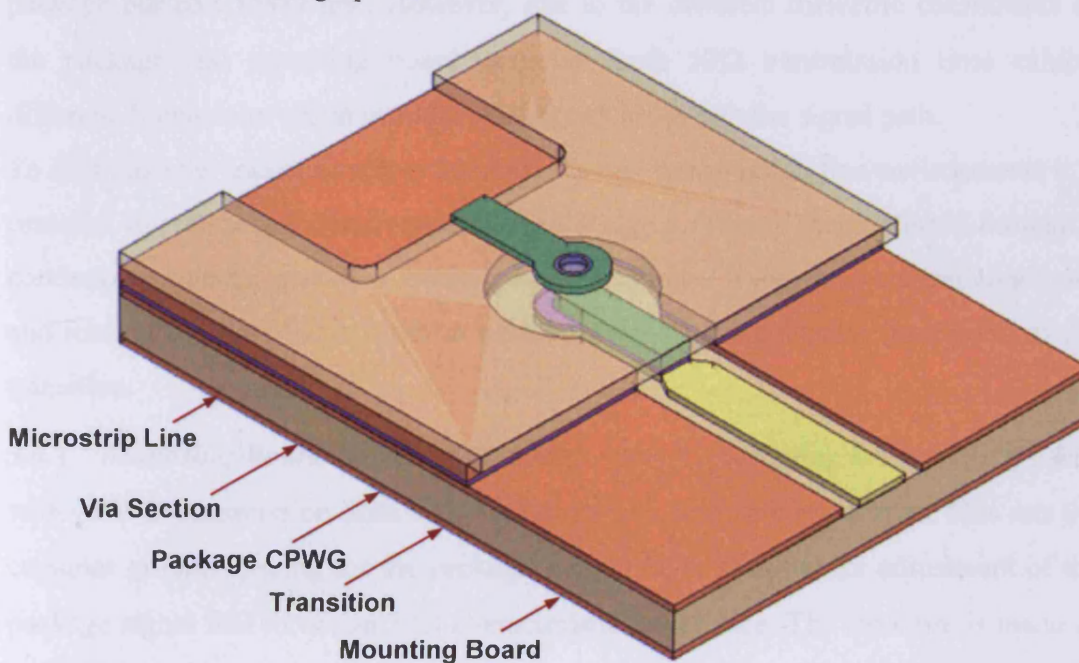


Fig. 3.23 Mounted LCP package Layout

The package is made of 100 μm thick Liquid Crystal Polymer (LCP) substrate ULTRALAM3000 (Rflex3000) with dielectric constant (D.K.=2.9, $\tan\delta=0.0025$ and breakdown voltage=3500 V/mil). The metallisation layers consist of gold plated copper with a 45 μm top layer thickness and a 100 μm bottom layer thickness. A micro via was used to connect the top and bottom metallization layers.

The mounting structure, the package was placed upon, was made of 254 μm thick RO4350B laminate with (D.K.=3.45) and the top and bottom metallization layers were made of 45 μm thick gold plated copper. A conductor backed coplanar structure

was adopted as a mean of transmission, whilst the vias used to connect the top and bottom metallization layers were made of normal through hole vias.

In order to present the design procedures for this package, consider the final package structure shown in Fig. 3.23. Note that each package part has been labelled and will be discussed separately.

The transmission line at the bottom side of the package consists of two different transmission line configurations as shown in Fig. 3.23. The first configuration is formed by the buried conductor backed coplanar (CPWG) transmission line on the bottom side of the package. The second transmission line is formed by the conductor backed coplanar transmission line of the mounting board which is used to feed the package buried CPWG line. However, due to the different dielectric coefficients of the package and mounting board materials both 50Ω transmission lines exhibit different dimensions which introduces discontinuities into the signal path.

To minimize the transition effect between the two transmission line environments it is essential to reduce any disturbance to the RF signal. This is accomplished through a continuous coplanar ground geometry which maintains the ground current continuity and leaving the signal line width as a variable for the optimisation (matching) of the transition.

3.6.1 Mounting Board Design: The design starts by designing the mounting board with CPWG transmission lines with 50Ω as the characteristic impedance. This sets the coplanar ground spacing for the package bottom layer to allow for adjustment of the package signal line to obtain 50Ω characteristic impedance. The structure is made of RO4350B laminate and the structure dimensions are shown in Fig. 3.24 below,

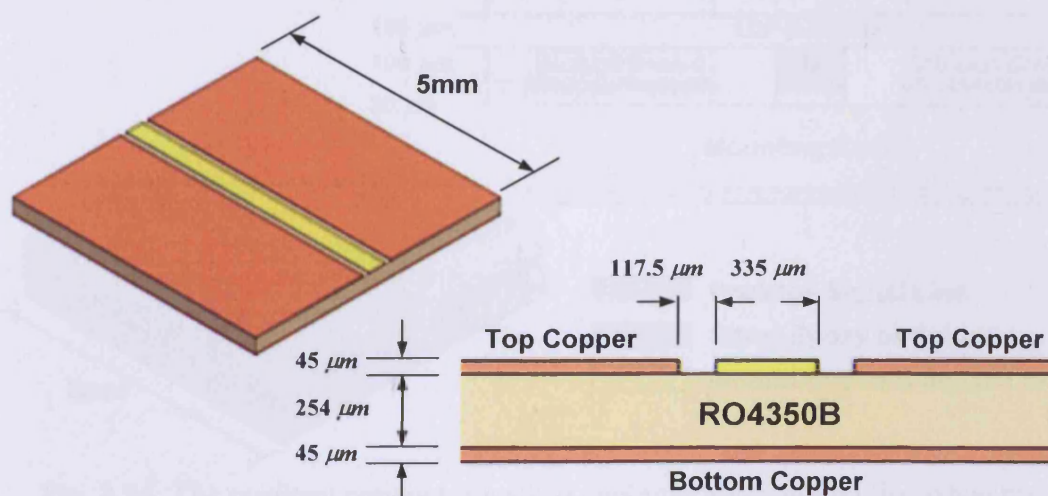


Fig. 3.24 Mounting board CPWG transmission line dimensions

Ansoft HFSS was used to simulate the behaviour of Fig. 3.24 transmission line, however the dimension was optimised to obtain a transmission line structure with 50 Ohm characteristic impedance. The simulation results normalised to 50 Ohm characteristic impedance are shown in Fig. 3.25 below,

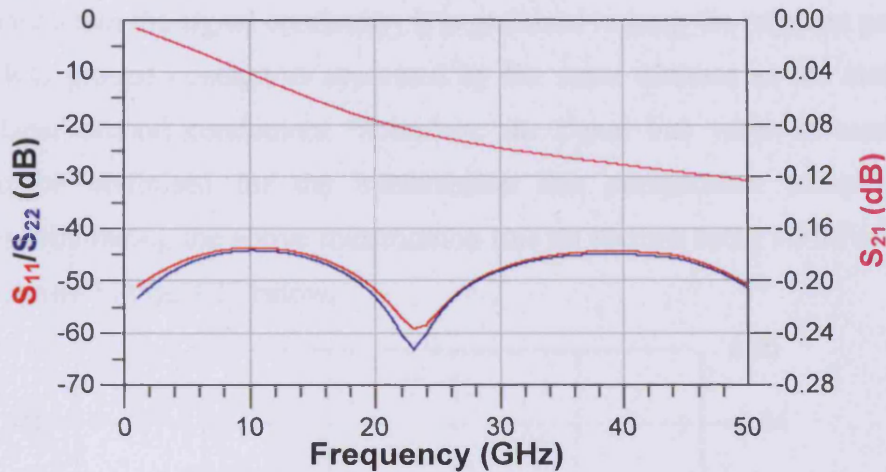


Fig. 3.25 HFSS simulation results for the CPWG transmission line of Fig. 3.24. The results above show a well behaved transmission line with more than 40 dB of return loss and less than 0.12 dB of insertion loss over the entire 50 GHz bandwidth.

3.6.2 Package Bottom (Buried) Conductor-backed Coplanar Transmission Line

Design: This line is formed by two different transmission lines, the first transmission line is a coplanar line on the package bottom side (Fig. 3.26) as stated earlier the package is made of LCP laminate with 100 μm of gold plated copper on the bottom side. The other transmission line is the continuity of the mounting board conductor backed coplanar transmission line (CPWG).

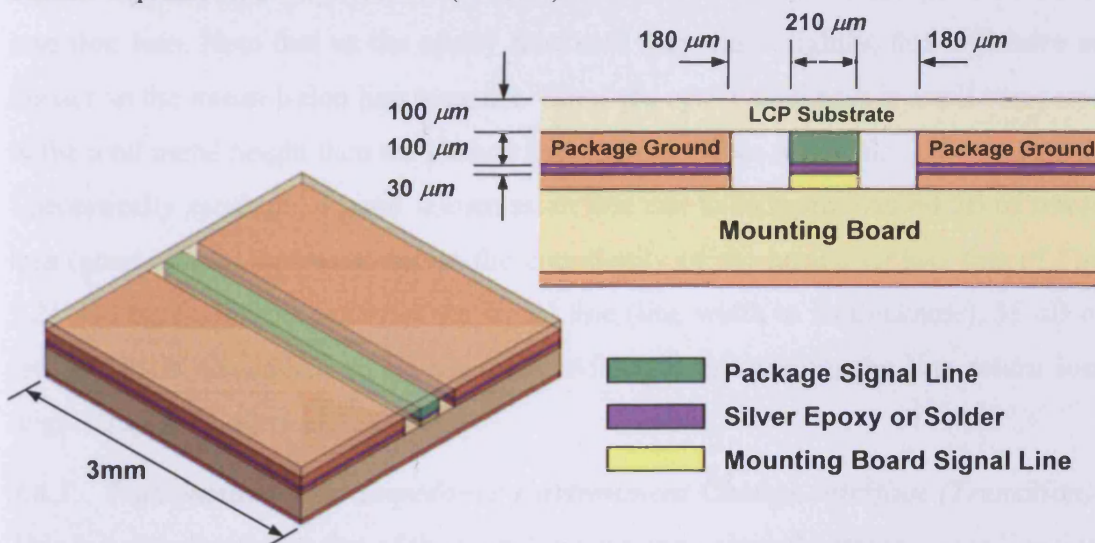


Fig. 3.26 The resultant conductor backed coplanar transmission line when the package is mounted onto the mounting board

By placing the two lines on top of each other while taking into account any solder/epoxy thickness, a new CPWG line can be realised and optimised to have 50 Ohm characteristic impedance.

As stated earlier in order to minimise the number of variables required to optimise this line and to maintain the signal continuity, it is preferred to keep the resultant package buried CPWG ground conductors separated by the same distance as the mounting board coplanar ground conductors. Therefore, the signal line width is used as a variable to be optimised for the transmission line performance (characteristic impedance). Simulating the above transmission line on its own using HFSS revealed the results shown in Fig. 3.27 below,

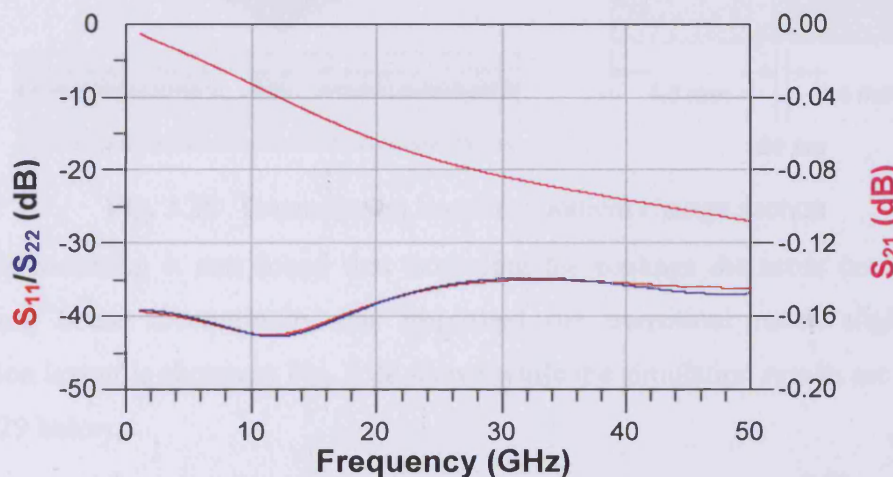


Fig. 3.27 HFSS simulation results for the CPWG line of Fig. 3.26

The results of Fig. 3.27 are normalised to 50 Ohm characteristic impedance and show a good transmission line with more than 35 dB return loss and less than 0.11 dB of insertion loss. Note that as the epoxy thickness may vary slightly, this will have an impact on the transmission line response. Since the epoxy thickness is small compared to the total metal height then the change in response will be minimal.

Theoretically speaking, a good transmission line can have more than 40 dB of return loss (good match), however due to the complexity of the buried CPWG line of Fig. 3.26 and the high aspect ratio of the signal line (line width to its thickness), 35 dB of return loss is considered to be adequate. After manufacturing, the line return loss might drop to 25 dB or slightly less.

3.6.3 Transmission Line Impedance Environment Change Interface (Transition):

This is a very important part of the launching structure since the transmission line will experience a change in dimension (discontinuity) and therefore the smaller the change

the better the performance will be. For this specific design the CPWG signal line of the mounting board has been reduced slightly (mitered) to mate with the CPWG signal line of the package to form a buried conductor backed transmission line (Fig. 3.28).

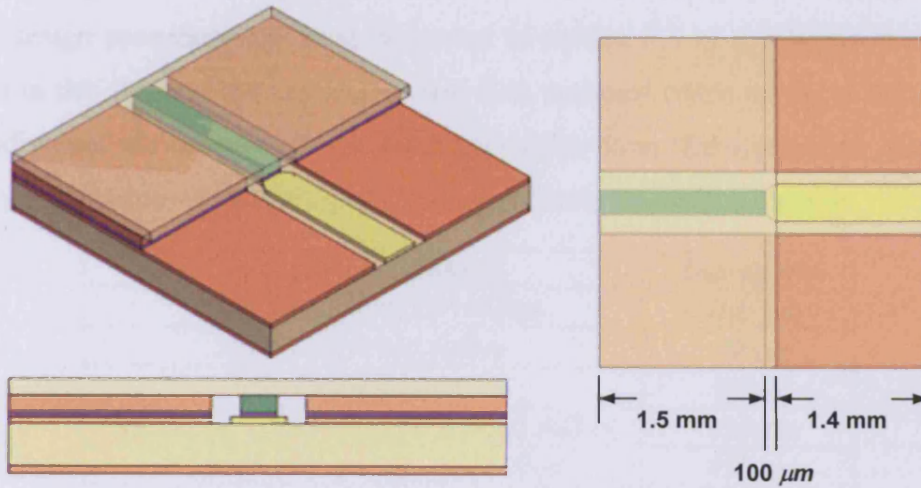


Fig. 3.28 Transmission line environment change section

For this transition it was found that extending the package dielectric on top of the mounting board discontinuity has improved the transition match slightly. The transition layout is shown in Fig. 3.28 above while the simulation results are shown in Fig. 3.29 below,

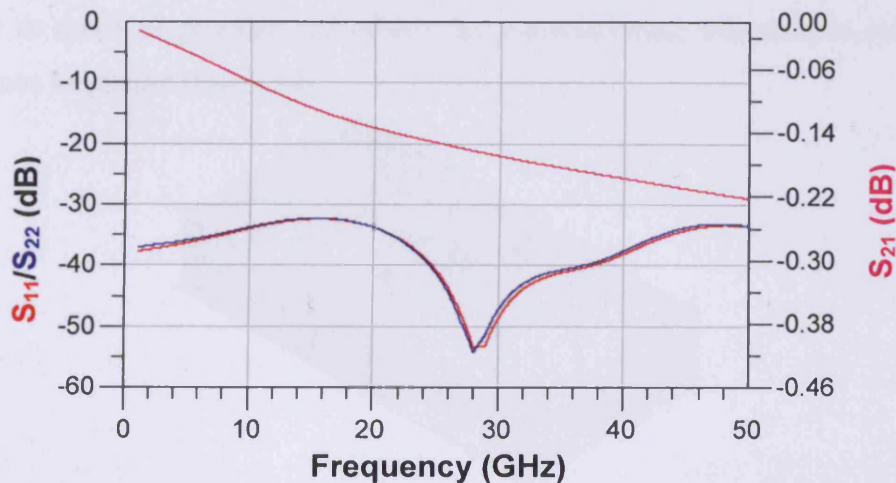


Fig. 3.29 HFSS simulation results for the structure of Fig. 3.28

The results of Fig. 3.29 above show that introducing a discontinuity in the CPWG line path has minimum effect with more than 30 dB return loss and 0.22 dB of insertion loss which is considered to be adequate from the design perspective.

3.6.4 Package Top Microstrip Transmission Line: This is one of the easiest lines to design since it is only a microstrip transmission line with 50 Ohm characteristic impedance. HFSS was again used to design and optimise such a line.

3.6.5 Package Via Section Design: The via section is a crucial part of this package; similar design procedures to those presented in section 3.3 of this thesis have been adopted in this design. The via section was first designed based on the simulation of each individual via components as discussed earlier, from that a selection was made for the via transition section geometry these are shown in Table 3.3 below.

Package Component	Dimension
Micro via bottom pad radius	105 μm
Micro via lower radius	50 μm
Via plating thickness	25 μm
Mounting board anti-pad ground radius	450 μm
Package anti-pad ground radius	450 μm
Micro via top pad radius (R_{top})	200 μm
Micro via upper radius (R_{Via})	100 μm
Mounting board pad radius (R_{Bottom})	200 μm

Table 3.3 Via section parameters definition

Note that the smallest chosen circular mounting board pad implied high capacitance to ground and larger than the top capacitance to ground value, therefore the pad was chopped as much as possible and within the manufacturing tolerance to reduce its capacitance to ground (Fig. 3.30).

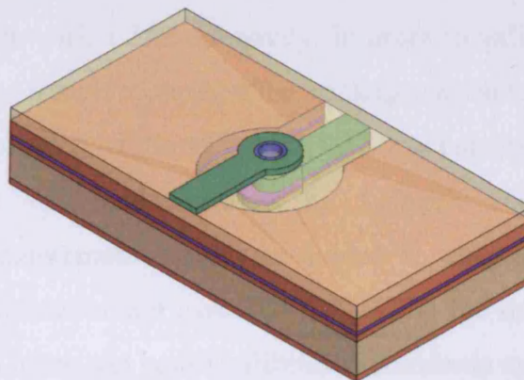


Fig. 3.30 Simulation setup using HFSS for LCP package when mounted onto a mounting structure (actual geometry)

For the above via section dimensions the via parameters value at lower frequencies were found to be $C_{g1}=58$ fF, $C_{g2}=49$ fF and $L=0.21$ nH.

Putting these values into the equivalent circuit of Fig. 3.12 and simulating it using ADS gave the frequency response shown in Fig. 3.31 below.

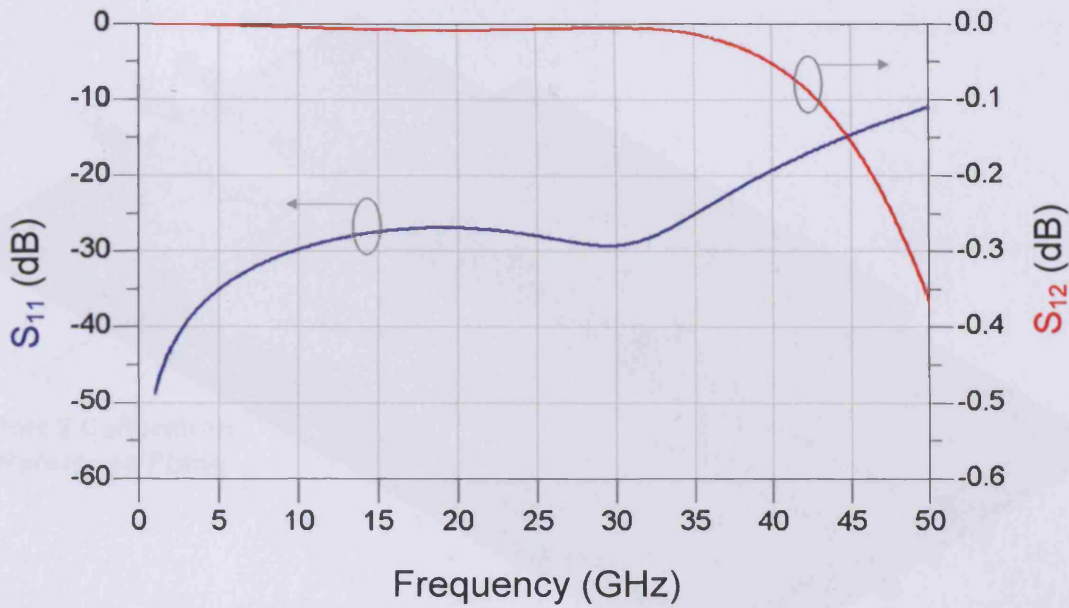


Fig. 3.31 ADS simulation results for the model of Fig. 3.30 with values $L=0.21$ nH, $Cg1=58$ fF, $Cg2=49$ fF

The results of Fig. 3.31 above show moderate performance. However there is no guarantee that when putting the via components together the package will behave as successfully as the above simulation.

3.7 LCP Mounted Package Measurement

Using the designed via components described above, a complete via section was extruded and the associated transmission lines were designed. The target package has a dimension of 5X5mm with a 2X2mm cavity. In order to validate the above design a 3mm thru line package which represents the package two sides connected together in a back-to-back configuration as shown in Fig. 3.32 was constructed.

The above package was manufactured by Labtech and measured. For this measurement, the measurement system presented in chapter 2 of this thesis was employed. A typical measurement involved calibrating the measurement system in a 1-tier TRL calibration using test board calibration standards made of RO4350B which have been manufactured by Labtech Ltd. These test board calibration standards included a 10mm line for the Thru standard and an 11mm line was used as the Line standard. A 5mm Open standard was used as the reflect standard and the 8510 VNA internal TRL calibration algorithm was used to implement the calibration with 256 averages. This calibration ensured that the measurement reference plane was shifted to the package reference plane.

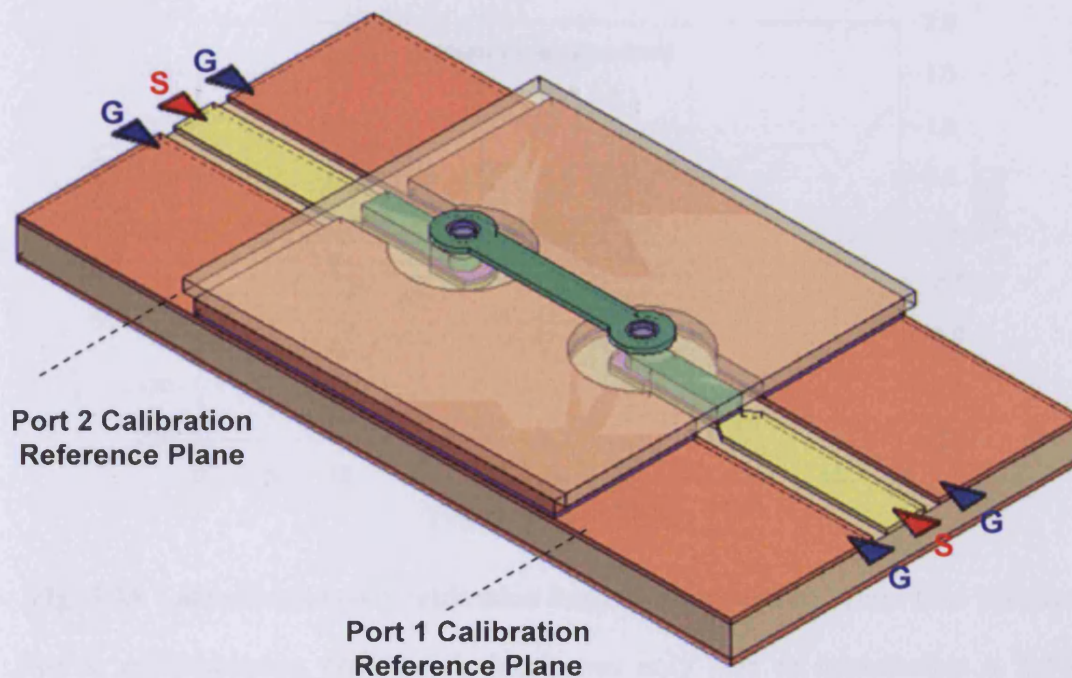
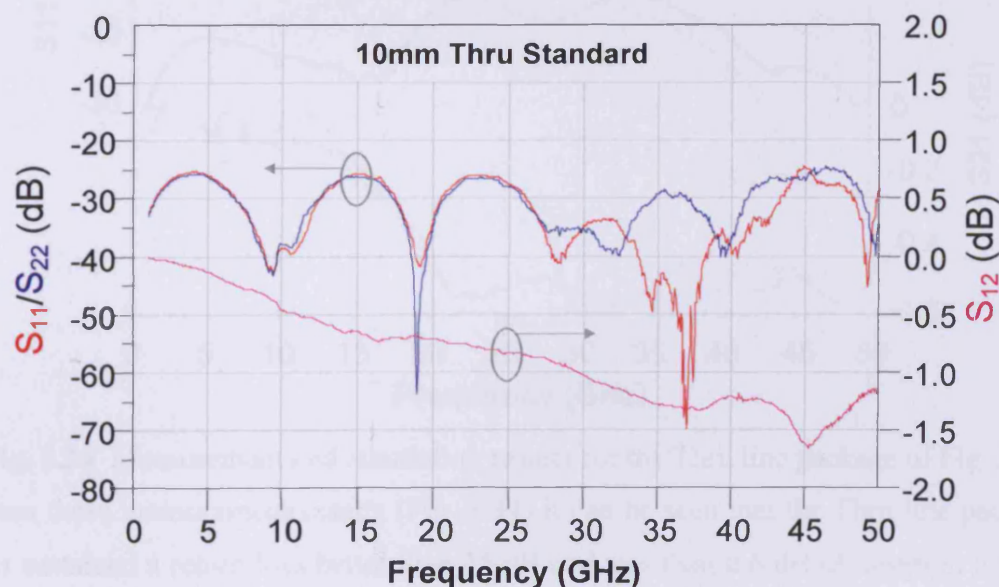


Fig. 3.32 Thru line LCP package mounted onto a test (mounting) board

Before performing this TRL calibration, the calibration standards were checked for quality and impedance consistency. This was performed by calibrating the measurement system up to the probe tips using an on-wafer TRM calibration up to 50 GHz, and then the Thru and Line standards were measured. The verification measurement results are shown in Fig. 3.33.

The response of these lines demonstrates that the line impedances are within the range 50 ± 0.5 Ohm over a 50 GHz bandwidth, verifying the lines are of high quality and with precise characteristic impedance.



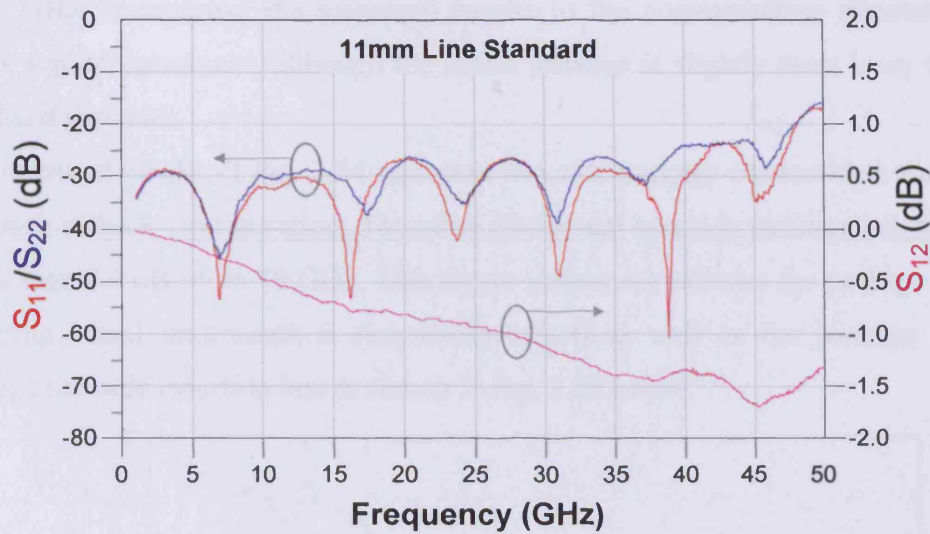


Fig. 3.33 Labtech test board calibration lines a) 10mm and b) 11mm Line standards

Due to manufacturing problems Labtech was only able to manufacture a 3x5mm package Thru standard which represent the package two sides connected in a back-to-back configuration as shown in Fig. 3.32. 400 μ m pitch GSG probes were used to launch onto the mounting board, having calibrated the measurement system, this Thru line package was mounted onto the test board (mounting board) and the Thru package was measured. The measurement results are compared to the simulated results as shown in Fig. 3.34 below.

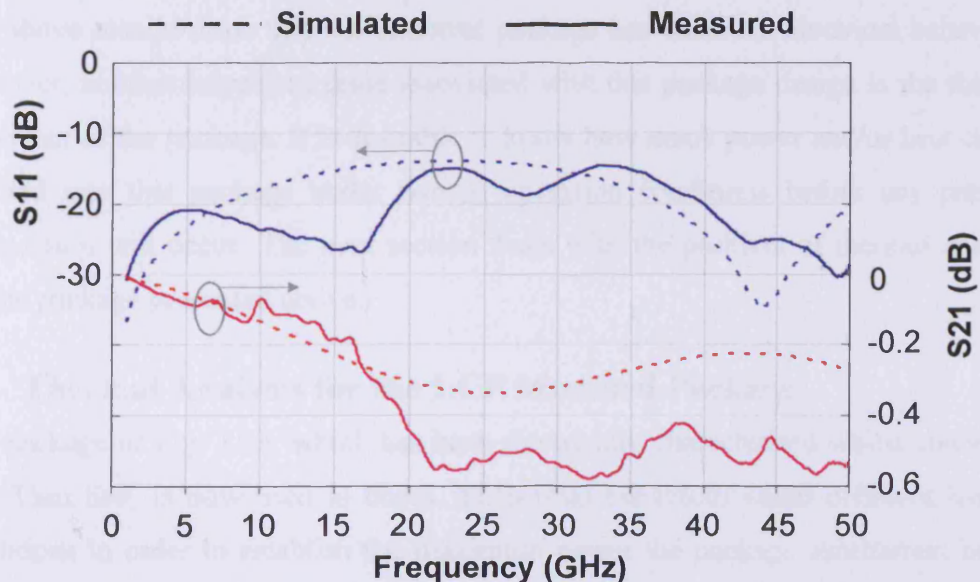


Fig. 3.34 Measurement and simulation results for the Thru line package of Fig. 3.32. From these measurement results (Fig. 3.34) it can be seen that the Thru line package has sustained a return loss better than 15 dB and less than 0.6 dB of insertion loss up

to 50 GHz. Comparing the measured results to the corresponding simulated data shows a good agreement, although the actual package is slightly more lossy than the simulated structure.

The measured results of Fig. 3.34 represent two side package connected to each other in a back-to-back configuration. Therefore, the actual one side package insertion loss is less than 0.3 dB up to 50 GHz. This figure (response) includes the package and the mounting board underneath it (launching effect) as well as the package lid, the package one side insertion loss is shown in Fig. 3.35 below.

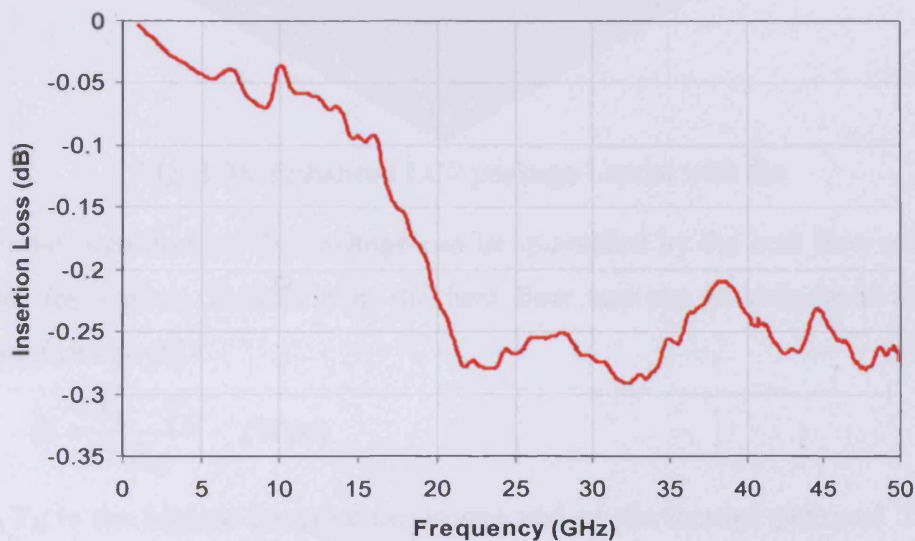


Fig. 3.35 Package of Fig. 3.32 one side insertion loss

The above results show that the mounted package has excellent electrical behaviour. However, another important issue associated with this package design is the thermal behaviour of the package. It is desirable to know how much power and/or heat can be injected into this package under normal operation conditions before any package degradation will occur. The next section deals with the problem of thermal analysis for the package presented above.

3.8 Thermal Analysis for the LCP Mounted Package

The package of Fig. 3.23, which has been electrically characterised whilst connected to a Thru line, is now used to check its thermal behaviour under different loading conditions in order to establish the maximum power the package can sustain before any degradation occurs. This in turn will define the maximum allowable MMIC power that can exist within this package, and will also optimise the heat dissipation method. To investigate this effect, consider the package shown in Fig. 3.36 with 2X2

mm² cavity. The die size was chosen to be 1.5X1 mm² and was placed in the centre of the package cavity.

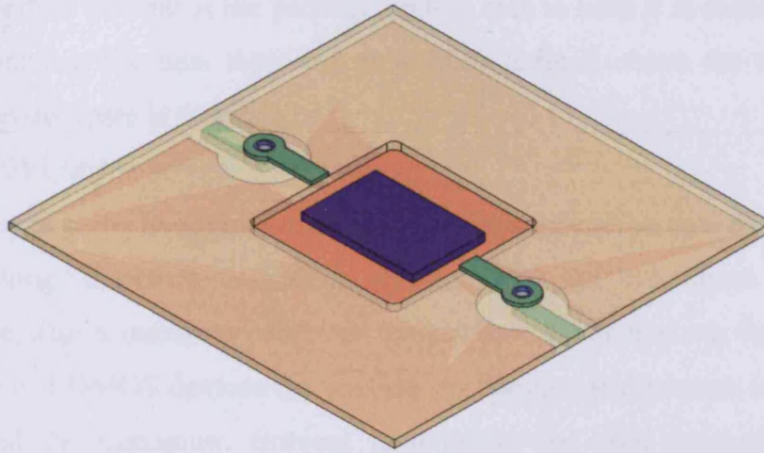


Fig. 3.36 Enhanced LCP package Layout with die

The thermal behaviour of the package can be quantified by the heat flow rate it can dissipate; for a given thermal path the heat flow rate can be calculated using the following formula [6]

$$H = \frac{T_H - T_L}{R_{th}} \quad (\text{Watt}) \quad (3.3)$$

Where, T_H is the highest temperature on one end of the thermal path and T_L is the lowest temperature on the other side of the thermal path. R_{th} is the thermal resistance of the heat path which is defined as

$$R_{th} = \frac{L}{k.A} \quad (^\circ\text{C/Watt}) \quad (3.4)$$

Where L is the height of the thermal path in (m), k is the material thermal conductivity in (W/m.K) and A is the area of the thermal path perpendicular to the heat flow direction in (m²).

For the above die area (1X1.5 mm²) placed onto a package base copper of 0.1 mm thickness and k , the copper thermal conductivity (390 W/m.K), the package base thermal resistance can be found using equation (3.4) to be $R_{th}=0.166$ °C/W.

The other thermal resistance which has to be included in the thermal analysis is the Silicon thermal resistance. The Silicon has thermal conductivity of $k=149$ W/m.K and for the die area specified above with 0.2 mm thickness, the thermal resistance of the die is found to be $R_{th}=0.895$ °C/W. Therefore the total thermal resistance of the package is the summation of the die and copper heat sink thermal resistances (since they are in series). The total thermal resistance is $R_{th-tot} = 0.166+0.895 = 1.061$ °C/W.

In order to calculate the absolute maximum power the package can sustain, then few assumptions have to be made. These are the die breakdown temperature is 200 °C and there is a perfect cooling at the package bottom side to keep it at room temperature of 20 °C. Applying the heat flow equation (3.3) defined above the total power the package can dissipate is found to be

$$H = (200-20)/1.061 = 169.65 \text{ Watt}$$

If the device is going to operate at its break down temperature then the device will not live for long therefore manufactures normally set maximum die operating temperature, also a maximum ambient temperature the device can work in has to be specified. For LDMOS devices the maximum operating temperature is specified to be 125 °C and the maximum ambient temperature for civil applications is 85 °C. Applying these figures on the heat flow equation (3.3) reveal $H=(125-85)/1.061=37.7$ Watt however this figure can go down when non-ideal die to package base is involved. In addition this type of surface mount packages are usually mounted on a PCB board, since the PCB board has its own thermal resistance, the above power will go down accordingly.

The package of Fig. 3.36 was simulated for its thermal behaviour using SolidWorks software. The junction temperature was set to 200 °C, which represents the worse case scenario. The first thermal simulation assumed that the package bottom plane (ground plane) is exposed to room temperature (by attaching a perfect heat sink) and therefore this surface was set to 20°C.

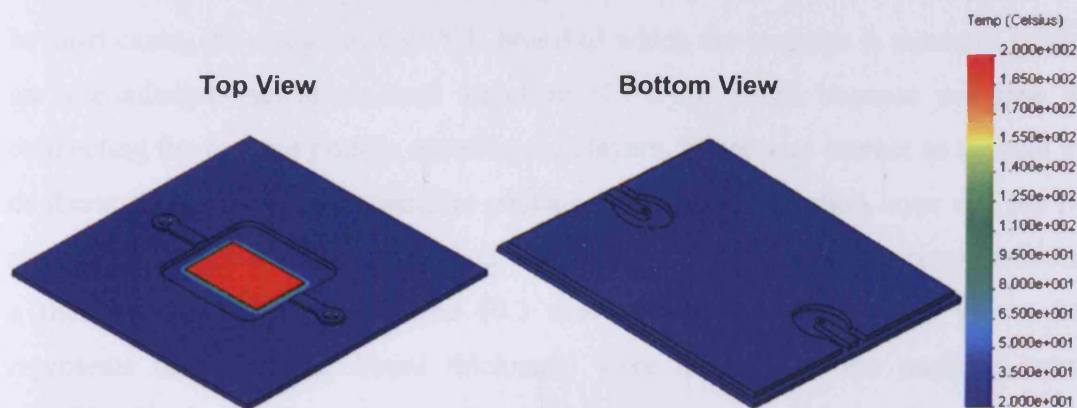


Fig. 3.37 Package heat distribution when package exposed directly to room temperature from the bottom side

The above simulation results show no problem for the package to dissipate the heat generated by the MMIC inside. Since the package is normally mounted on a test (PCB) board; therefore if the test board supporting the package is a coplanar structure, then the heat will be enclosed within the area directly beneath the package and the only way for this heat to escape is through the package bottom metal plane sides which are set to room temperature during the simulation shown in Fig. 3.38 below.

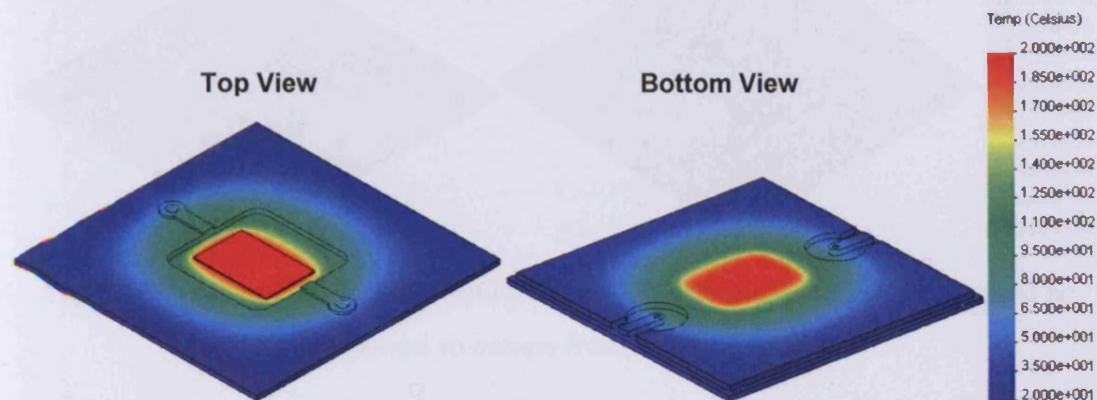


Fig. 3.38 Package thermal distribution when no heat sink underneath the package is present but only the bottom metallization layer sides are exposed to room temperature

The results of Fig. 3.38 above shows that the temperature across the package will reach 130 C° near the via section, which represents a significant problem as the LCP material has a very high z-axis thermal expansion coefficient. Consequently, this extreme temperature might lead to cracks in the connection between the via and the via pads which would compromise package reliability and mechanical stability.

In most cases, the design of the PCB board to which the package is mounted is based on a conductor-backed-coplanar structure (CPWG) which imposes multiple vias connecting the top and bottom metallization layers. These vias can act as thermal vias or thermal escape path between the package bottom metallization layer and the heat sink where the PCB board is attached. This condition was taken into consideration in a thermal simulation where nine (0.3 mm diameter) 250 um high vias (which represents the mounting board thickness) were attached to the package bottom metallization layer. To represent the worse case scenario the whole package was assumed to be isolated from the outside world with the only way for heat to be dissipated being through the mounting board thermal vias (in this simulation the mounting board vias bottom surface was set to room temperature, i.e. 20°C). The simulation results are shown in Fig. 3.39. It is clear that the whole package will be

exposed to very high temperatures, risking excessive thermal expansion in all directions, especially in the z-axis. A solution is therefore required to minimise this problem.

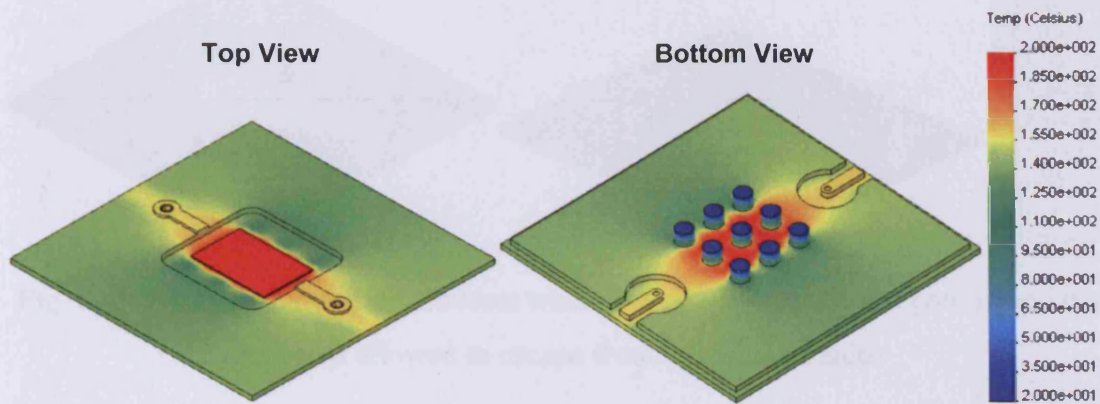


Fig. 3.39 Package thermal distribution when nine thermal vias are present and no heat allowed to escape from the package sides

One solution is to increase the number of thermal vias underneath the package. An attempt was made to do this by increasing the number of vias underneath the package from nine to sixteen. The simulation results are shown in Fig. 3.40 below.

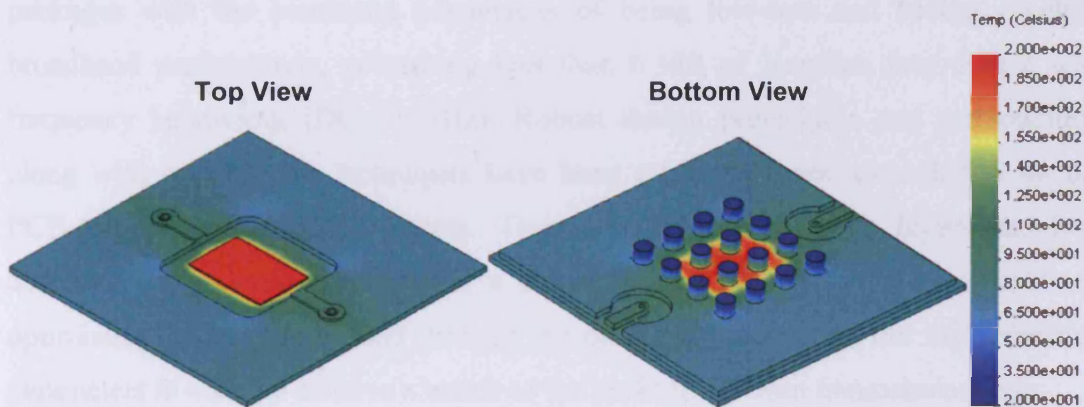


Fig. 3.40 Package thermal distribution when sixteen thermal vias are present and no heat allowed to escape from the package sides

As expected the extra thermal vias have reduced the temperature across the package from 130 C° down to 70 C°, which represents a considerable heat reduction.

The final simulation attempt was based on the setup shown in Fig. 3.40 where it is assumed that the heat can escape through the PCB board vias and from the package bottom metallization layer (plane) sides as well. The simulation results show a significant improvement in the package heat dissipation, and are shown in Fig. 3.41.

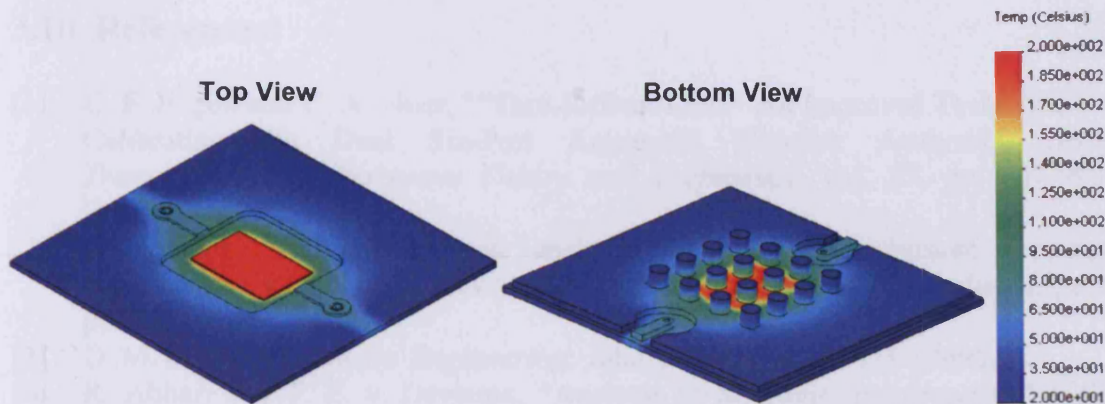


Fig. 3.41 Package thermal distribution when sixteen thermal vias are present and the heat was allowed to escape from the package sides

This is a considerable reduction in the heat distribution across the package therefore it is important to provide enough space around the package bottom metallization layer for the heat to escape efficiently.

3.9 Summary

This chapter details the development of novel, low-loss, thermally enhanced LCP packages with the combined advantages of being low-cost and having excellent broadband performance, possessing less than 0.3dB of insertion loss over a wide frequency bandwidth (DC-50 GHz). Robust design procedures and methodology, along with optimisation techniques have been established, and extended to include PCB-to-package launching effects. Transition between package layers has been achieved using micro-vias. This is a technique that has proven to be effective in optimising the transition itself through the proper adjustment of the via's electrical parameters in order to achieve a match to the package 50 Ohm transmission lines.

Thermal analysis and optimisation has been carried out, and is used as a design guide to determine the maximum power handling and heat dissipation constraints of the packages.

In summary, LCP material has been used as a low-cost alternative to expensive ceramic substrates. The excellent characteristics of the LCP materials coupled with the optimised micro-via design has resulted in impressive package performance up to 50 GHz.

3.10 References:

- [1] G. F. Engen and C. A. Hoer, "“Thru-Reflect-Line:” An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer," *IEEE Transactions on Microwave Theory and Techniques*, vol. 27, pp. 987-993, December 1979.
- [2] D. Rytting, "Appendix to an analysis of vector measurement accuracy enhancement techniques," *Hewlett-Packard RF Microwave Symposium Digest*, pp. 1-42, March 1982.
- [3] D. M. Pozar, *Microwave Engineering*: John Wiley, ISBN 0-471-17096-8.
- [4] R. Abhari and T. E. v. Deventer, "Analysis of Microvia Interconnects," *IEEE MTT-S International Microwave Symposium Digest.*, vol. 3, pp. 1925 – 1928, June 1998.
- [5] W. Simon, R. Kulke, A. Wien, M. Rittweger, I. Wolff, A. Girard, and J. P. Bertinet, "Interconnect and transitions in multilayer LTCC multichip modules for 24 GHz ISM-Band applications," *IEEE MTT-S International Microwave Symposium Digest*, vol. 2, pp. 1047 - 1050, June 2000.
- [6] Y. Freedman, *University Physics*: Addison Wesley, ISBN 0-321-20469-7.

CHAPTER 4

HIGH-POWER PACKAGES AND THEIR CHARACTERIZATION TECHNIQUES

The aims of this chapter are to present a literature review of the various packaging technologies, to identify the considerations relating to packaging of high-power active devices, and to discuss in detail the different systems used to measure high-power devices. A new and novel non-linear measurement system is presented that has been designed to characterise the high-power packaged devices discussed in this thesis. This is presented along with the results of measurement-based verification.

4.1 High-Power Package Technologies

Packaging is crucial factor in maximizing the performance of RF power transistors. Regardless of the type of active device, a high-power package is always required to provide an electrical (RF) signal path, DC feeds and most importantly a means of dissipating the excessive heat that is associated with high power devices. Since the RF power device tends to be the most expensive component within high-power Power Amplifiers (PAs) [1], and the PA itself is the most expensive component in a cellular base station, there is substantial market pressure to reduce the cost of the transistor and its packaging without sacrificing performance.

With these market pressures driving improvements in device technologies, the power rating of high-power solid state devices has increased over time. This has however placed additional pressure on the high-power packaging industry; to cope with increasing semiconductor devices performance whilst keeping package cost to a fraction of the active device cost. Two main types of high-power package have become very popular for high-power applications. These are firstly ceramic packages, that offer high performance but tend to be expensive, and over-molded plastic packages, that offer moderate performance at low cost.

4.1.1 High-Power Ceramic Packages

For many years ceramic packages [2, 3] have been used to house RF power transistors due to their good thermal and electrical performance. This kind of package has

consistently managed to fulfil the performance and reliability demands imposed upon them. However, the resulting cost-per-package can represent a significant portion of the overall price of the high-power transistor; hence numerous developments have been undertaken in the past to develop more cost-effective packaging.

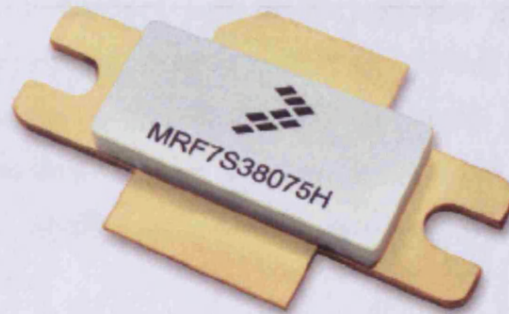


Fig. 4.1 High power ceramic package [4]

The package of Fig. 4.1 combines a thermally and electrically conductive metal base with a ceramic ring to isolate the input and output leads. The base is made of a copper-tungsten alloy where the ceramic ring is attached to it by means of a high-temperature brazing process. Additionally, the package base is gold plated to allow the die to be attached by means of a second high-temperature process, conventionally called eutectic bonding. Finally, the package is capped with a ceramic lid that is glued to the ceramic ring and the input and output leads for environmental protection.

Depending on the transistor technology, different heat transfer mediums have been introduced to dissipate the heat from the high-power transistor. For example, the die can be attached directly to the package heat sink via a eutectic bonding process (this normally happens at 320 C° for Gold-tin attachment and at 400 C° for Gold-silicon attachment). This kind of heat dissipation technology is considered to be the most efficient and lowest cost solution. Since the package is normally placed directly onto a heat sink, this will provide a direct thermal path to dissipate the heat from the package bottom side.

Another suggested technique which is applied to MOSFET power transistors include the use of diamond as a thermal transfer medium [5], which is a very expensive solution. Other methods engineer the package metal heat sink to dissipate the heat from the package top side by inverting (flipping) the die inside to allow maximum heat dissipation through air convection [6, 7].

4.1.2 High-Power Plastic Packages

This is a well established technology [8, 9] for normal power integrated circuits (IC) applications, but it has recently improved to serve the needs for RF power transistors (Fig. 4.2). These improved capabilities include lower moisture absorption and a stable dielectric constant. The technology provides the necessary technical performance at costs roughly one order of magnitude less than the existing ceramic approach. The cost reductions are achieved by eliminating the costly ceramic ring, and its cumbersome and expensive brazing process. Innovations in polymer materials (plastics) have made it possible to use these packaging types for demanding high-power RF PA applications.

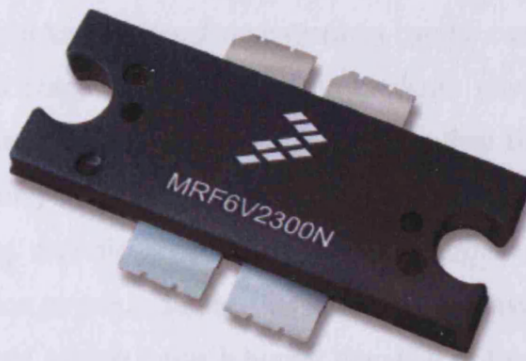


Fig. 4.2 350 Watt high power plastic package [4]

There are two classes of synthetic polymers used in RF packaging today [10]: thermoplastic and thermosetting polymers. Thermoplastics are processed by means of heat and pressure alone, without a chemical reaction. Upon cooling, thermoplastics either crystallize or transform to a glassy state. Thermosetting polymers (epoxies, bakelite, Formica) chemically react upon the application of heat, causing an increase in the molecular weight. This chemical reaction leads to full conversion of all reactive groups to produce a polymer with substantial hardness, high heat distortion temperatures, and both good chemical and physical resistance.

The chip is normally bonded to the lead frame using wire bonding, then the whole package is encapsulated in a polymer which acts as a dielectric insulator shield against the outside environment. Since the polymer acts as a dielectric, it can give rise to package parasitics and degrade the transistor performance. However, this effect can be compensated or minimized with a proper matching design.

The manufacturing process for this kind of package involves complex assembly and aligning machines. It involves a large metal frame with numerous transistor frames connected to each other. The dies are attached one by one to each transistor frame and bonded. Then the whole assembly is injected with plastic mold to form the complete transistor. Finally bonded transistors are cut (either saw or laser machined) to obtain individual transistors; this makes this kind of technology suitable only for high volume production.

Different applications require different package size, power handling capability and bandwidth. In terms of physical size, the smaller the package the less it will cost, and for high power applications, the less heat it will dissipate. Therefore a compromise solution has to be selected which provides good package thermal management at lower cost. However package thermal management can be controlled and designed at the material selection stage as well as at the package physical design stage. For example the above described ceramic package has excellent thermal dissipation but it is very expensive. Conversely, the above described plastic package is much cheaper than its corresponding ceramic counterpart, but its thermal management is heavily dependant on the device power rating and its technology, polymer used, as well as the moisture absorption rate, which is much higher than that of the ceramic solution.

An optimized solution, which combines the high electrical and thermal performance of the ceramic packages with the low-cost of the plastic packages is under continuous demand. The objective of the high-power package part of this thesis is to investigate this optimum solution. Therefore, and based upon the laminate properties discussed in Chapter 2 of this thesis, a high-power laminate has been deployed in this work to investigate its suitability for high power packaging applications. The laminate based package solution can fill the missing gap between the ceramic and plastic packages in terms of cost versus performance, and this is illustrated in Fig. 4.3 below.

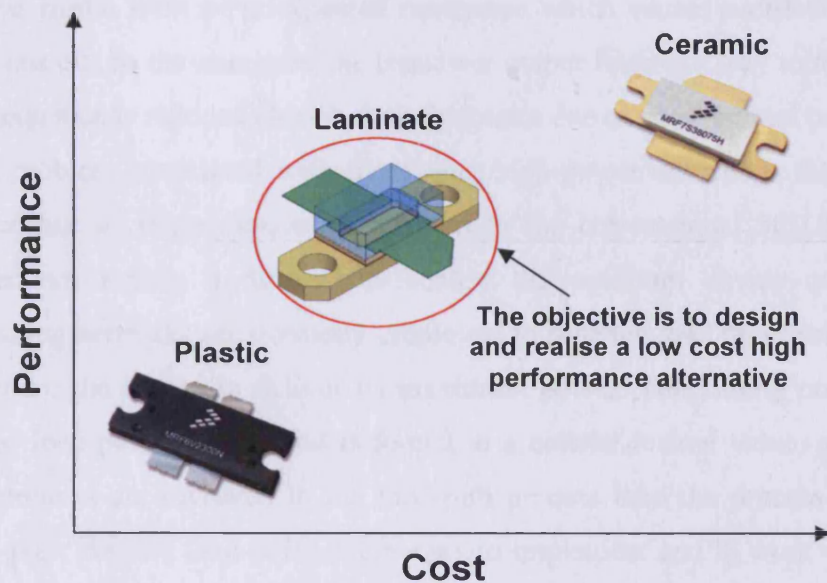


Fig. 4.3 Cost versus performance for different high power packaging technologies

Laminate based high-power packages are based on the PCB manufacturing technology and are therefore most suitable for batch processing and lower manufacturing volumes than plastic equivalents. With the excellent electrical and thermal performance and low moisture absorption properties of laminate, this technology has a promising future.

With advances in semiconductor technologies, high-power semiconductor devices are increasingly cooler under loaded operation. Thermal simulations are normally carried out to characterise the package's thermal behavior and optimize its performance. For the high-power package discussed in this thesis, only thermal simulations were performed.

The other important aspect of the package is its electrical performance. Ideally the package should provide a transparent transition between the die and the outside world. This of course is not the case in reality; conventionally, the package is designed using an electromagnetic (EM) simulation tool to make sure that the package components are behaving within the package specifications such as insertion loss, return loss, isolation, as well as checks for any cavity resonances. However, in high-power applications, electromagnetic simulation may not offer adequate accuracy in order to guarantee that the package will work properly when the die is attached and bonded. This is simply because at high power levels and when the device is encapsulated inside the package, there will be significant electromagnetic interaction. This might

appear in the form of unexpected resonance which causes oscillation (this normally happens due to the energy at the transistor output finding a way to the input), another consequence is reduced electrical performance due to poor thermal properties.

One problem associated with measuring high-power devices is that the low output impedance of these devices in relation to the conventional 50 Ohm measurement impedance makes it difficult to realise the optimum device output impedance. Matching networks are normally employed to tune the load presented to the device in order for the device to deliver its maximum power. This tuning process is normally called load-pull (i.e. the load is forced to a certain desired value) and when passive components are involved in the load-pull process then the process is called passive load-pull. Passive load-pull is very easy to implement and to work with up to certain limits. These limits are set by the losses associated with the passive load-pull system components (e.g. tuners, stub-tuners, etc...). Hence the load(s) presented by the measurement system cannot reach the boundary of the Smith Chart due to these losses, and in the case of very high-power devices, it becomes difficult, if not impossible to present the required impedance to the Device Under Test (DUT).

The other important factor associated with package performance is the effect the package has on the harmonics generated by the DUT. Modern PA design employs waveform engineering using voltage and current waveforms generated by the DUT to optimize performance in terms of efficiency, linearity, etc. This can be achieved using either a passive or active load-pull systems. In the active load-pull process the load is 'pulled' to a certain value electrically using an external RF source with frequency identical to the DUT frequency.

Additionally, the need to accurately measure these harmonically rich waveforms requires careful calibration of the measurement system in order to obtain the required information. Initially power measurement systems are usually calibrated using standard calibration procedures, such as those presented in chapter 2 of this thesis. However, these calibration procedures can give only the product of the system transmission tracking ($e_{10}e_{32}$ and $e_{01}e_{23}$) and reflection tracking ($e_{10}e_{01}$ and $e_{32}e_{23}$) coefficients. Additional calibration steps are thus required to separate the product error coefficients into their individual components (e_{10} , e_{01} , e_{32} and e_{23}). The magnitude, the minimum requirement for scalar power measurement, can be easily achieved by attaching a spectrum analyzer or power meter to the system calibration ports. Separate the phase information of each error coefficient, essential for

waveform measurements, requires extra calibration step. This involves either attaching a very specialized phase calibration standard or a calibrated sampling receiver to the system calibration ports. This step allows non-linear measurement systems to obtain the phase information not just at the fundamental but also of each harmonic [11]. This type of system is thus able to reveal a lot of information about the DUT but its implementation is rather complicated and can be more expensive than the basic scalar power measurement load-pull systems. The package measurement techniques using these systems along with the basis of operation of the passive and active load-pull systems are discussed in the next section.

4.2 Measurement Techniques for High Power Packages

The electrical measurement of high-power packages can be classified into two main categories, specifically passive and active measurements. Passive measurements similar to those discussed in Chapter 2 and 3 of this thesis can be implemented with some modification which involves placing a transmission line inside the package and bonding it to the package leads [12]. This method provides valuable information about the package, but as discussed earlier more advanced measurements which include placing an active device inside the package may become necessary.

For the active measurement approach, the measurement system is required to provide the appropriate source and load impedances in order for the device to deliver its maximum power. Note that different impedances are required to maximize device power, gain and efficiency.

This process is denoted as source and load-pull, where the source and load impedances presented to the DUT are tuned externally to obtain optimum device operation. This impedance tuning can be performed at the fundamental frequency of operation, as well as at the harmonic frequencies, and in this case is termed harmonic source and load-pull.

Unfortunately, most if not all measurement systems are based on a 50 Ohm characteristic impedance. This in turn creates a large mismatch between the system characteristic impedance, and the high-power DUT input and output impedances.

The source impedance mismatch can be overcome by increasing the drive level (drive the device harder). On the other hand, at the device output, due to the high mismatch between the measurement system characteristic impedance and the DUT output impedance (e.g. sub 2 Ohm for a 100W LDMOS device) the only way to get the

device to deliver its maximum power while reaching its optimum equivalent thermal state is by providing a proper matching at the device output plane. Hence, output load-pull is essential if high power devices are to be characterized under system relevant operating conditions; this can be achieved using either a passive or active load-pull systems.

These passive and active load-pull systems come with their own advantages and disadvantages which are summarised below [13]:

Passive Load-pull Measurement System: Passive load-pull can be easily implemented by attaching a load tuner, usually comprising a phase shifter and variable attenuator to the output of the DUT (Fig. 4.4). This configuration allows control of the magnitude and phase of the reflection coefficient presented to the DUT (Γ_{Load}). This reflection coefficient can be quantified in terms of the impedance presented to the device.

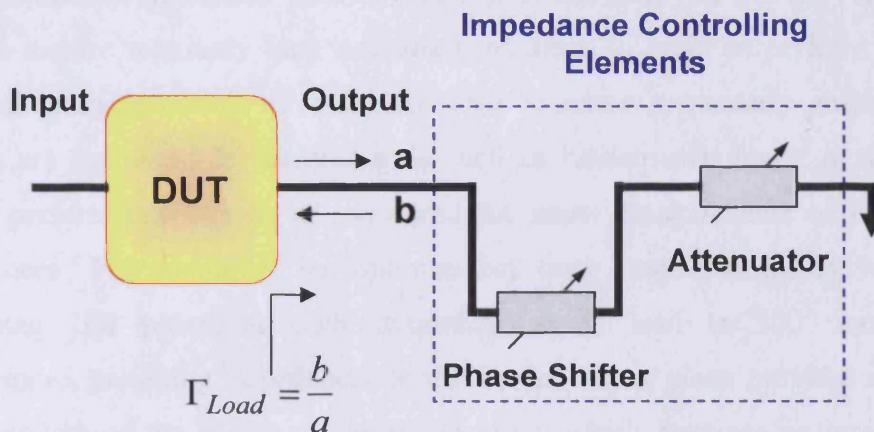


Fig. 4.4 Passive load-pull measurement system concept

In the system shown in Fig. 4.4, and while the DUT is delivering energy into the measurement system (**a**), the impedance controlling elements will reflect part of that energy back to the DUT (**b**). The maximum theoretical reflection coefficient which can be obtained from this method is $|\Gamma_{Load}|=1$ (all injected energy is reflected back to the DUT) and the minimum is zero (all injected energy is absorbed by the impedance controlling element). However, in a real-world implementation, any losses introduced between the DUT and the impedance controlling elements or losses introduced by the impedance controlling elements themselves will reduce the amount of energy reflected back to the DUT (**b**) and therefore will limit the synthesised reflection coefficient to a value $|\Gamma_{Load}|<1$.

Practically, the impedance controlling elements in Fig. 4.4 above can not be placed immediately after the DUT due to the presence of other components such as launchers, mounting board, test fixtures, couplers, etc. These components are normally lossy. In addition, impedance controlling elements themselves will add loss with even the very highest quality tuners being reported as introduce some degree of loss [14]. Therefore, when load-pulling a high power device that requires very low output impedance and a reflection coefficient approaching unity, the passive load-pull system may fail to reach these extremes. This limitation significantly reduces the suitability of passive load-pull systems for fully characterising high power devices, hence package evaluation.

The package itself could also have a huge impact on the harmonics generated by the DUT and therefore characterising the packaged device at the harmonics is necessary.

This issue has attracted researchers to develop systems that use classical passive load-pull systems in conjunction with a Vector Network Analyser (VNA) [15, 16]. Such systems require relatively long measurement times in order to perform a complete load-pull characterisation of a device. This becomes particularly noticeable when devices are optimised for harmonic, as well as fundamental loads, in this case the device performance has to be measured for many combinations of the harmonic impedances. For example, an optimisation over three harmonics with a grid containing 100 points at each frequency would lead to 100^3 measurements. Furthermore, sweeping impedances at the device output plane provides only limited understanding of the device mode of operation, which becomes an important point when analysing the device or amplifier's performance. The ability to measure and control the relative phase of all harmonics is critical when characterising more complex, multiple-device structures such as the Doherty amplifier. One issue associated with these systems is the need for a sensing coupler to be inserted into the load-pull path. The couplers themselves introduce losses which limit the area of Smith chart that can be scanned, and hence limits the ability of these systems to characterise high-power, very low impedance devices. When characterising high-power devices with output impedance near the boundary of Smith chart using passive load-pull measurement system it is essential to attach the passive load-pull tuner between the device under test and the sensing coupler. Thus measurement accuracy will suffer, even when the tuner s-parameters are accurately measured. This is because when the tuner reflection coefficient is set near the boundary of Smith chart then most of the

energy will be reflected back to the device under test. This makes it difficult to compute accurately the power delivered by the device under test from measurements that are now performed on the other side of the passive tuner.

Fortunately, active load-pull systems are capable of overcoming these limitations, thus avoiding the need to relocate the sensing coupler; these systems are discussed in more detail in the following section.

Active Load-Pull Time Domain Measurement Systems: The disadvantages associated with the passive load-pull systems described above can be overcome by using time domain/waveform measurement systems in conjunction with an active load-pull. This setup allows for device optimisation through waveform engineering [11, 17]. The basic concept for the active load-pull technique can be explained using the open loop architecture shown in Fig. 4.5 below. In this model the passive impedance controlling element used in the passive load-pull system is replaced by a load-pull power source with full control over the load-pull signal magnitude and phase. By injecting energy from the load-pull source (**b**) to the DUT output, any impedance can be synthesised, including impedances that lay outside the Smith Chart area i.e. $|\Gamma_{Load}| > 1$.

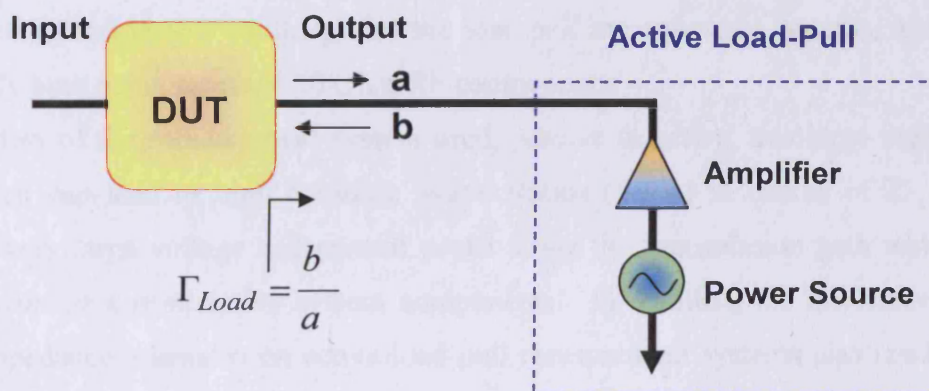


Fig. 4.5 Open loop active load-pull measurement system concept

A number of different, active load-pull measurement systems have been developed to enable the characterisation of high-power transistors. Among these is the feedback architecture [18, 19] where part or all of the DUT signal is amplified and injected back to the DUT in order to synthesize an impedance at the device reference plane. This kind of load-pull techniques is prone to oscillation in the feedback loop causing device instability and measurement failure. In this case, incorporating narrow-band

filters for the fundamental and every harmonic in the feedback loop becomes essential in preventing oscillation problems.

Another active load-pull technique is feed forward [20, 21]. In this kind of architecture a single load-pull source is used to both drive and load-pull the DUT with the output path being tuned and boosted via the use of impedance controlling elements and a power amplifier. This kind of system can be operated in a stable condition but since mechanical tuners are involved in the load-pull measurement, the process can be quite slow.

The open-loop load-pull concept shown in Fig. 4.5 above is adopted in this thesis as a basis for the new design of the high-power time-domain measurement system, with active harmonic load-pull that is capable of characterising high-power LDMOS devices used to measure the packaged high-power devices presented in this thesis.

4.3 High-Power Time-Domain Active Harmonic Load-pull Measurement System Overview

Characterizing high-power packaged devices in excess of 30 Watt can become problematical. This is mainly due to the relatively low voltage swing of these devices which means that the optimum output impedance is in the range 0.5-2 Ohms. This provides a considerable challenge for the load-pull measurement systems, which are normally built using standard 50 Ohm RF components.

Regardless of the measurement system used, passive or active, this large impedance mismatch can lead to high Standing Wave Ratios (SWR) in excess of 25, which causes very large voltage and current peaks along the transmission path which can easily damage cost-sensitive system components. In addition, the implication of a high impedance mismatch on active load-pull measurement systems also results in a rapid increase of the load-pull power levels required to emulate such low impedances. Simple scaling of the output power capabilities of the active load-pull would become rapidly prohibitive.

For the novel design presented in this thesis, a comprehensive and in depth analysis of the active load-pull systems, coupled with the theoretical understanding has been applied to passive and active load-pull systems in order to identify the key constraints of both systems, when operating at high powers. The results of the analysis have been used to develop the new high-power active load-pull system by incorporating two broadband impedance transformers that dramatically reduce the power levels required

from the active load-pull system, needed for device characterization. The analyses of the impedance transformer designs and impedance value optimisation are discussed in great detail. Also, a novel approach which involves combining passive and active load-pull systems into one powerful system is discussed.

4.3.1 Load-pull Measurement Systems Limitations

The consequences of combining high output power and low output impedance can create two significant problems that must be addressed in the design of load-pull systems. The first relates to the large voltage standing wave introduced when the impedance controlling element is not directly located at the device output terminals. This is a constraint for both active and passive load-pull systems alike, even if sensing components are not required. The second factor relates to the ability of active load-pull systems to achieve impedance control at high-power levels.

4.3.2 Voltage Standing Wave Effect in Load-pull Systems

The voltage standing wave (VSWR) effect can be analysed initially using a passive load-pull measurement system (Fig. 4.4), and the results applied directly to active load-pull systems. In order to quantify the impedance controlling element offset constraint, consider the simple passive load-pull measurement system model of Fig. 4.6 below where the DUT is represented as a voltage source V_d in series with an impedance Z_d . The DUT is connected to the passive load-pull measurement system via a 50 Ohm transmission path. In order for the DUT (Fig. 4.6) to deliver its maximum rated power P_d , it needs to see the complex conjugate of its effective internal, large-signal output impedance.

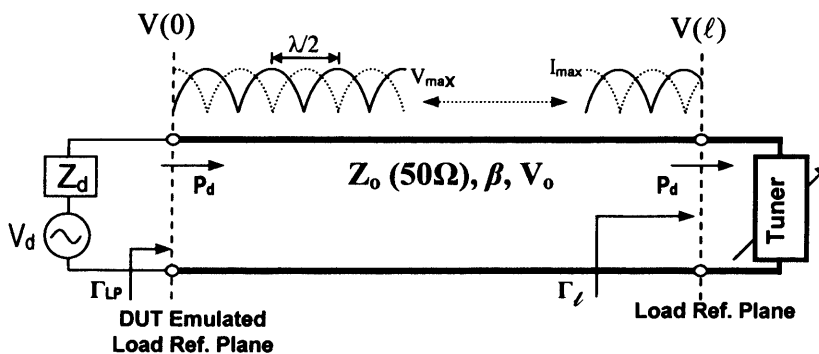


Fig. 4.6 Passive load-pull measurement system methodology

Ideally, the impedance controlling elements (e.g. RF tuner) should be connected directly to the DUT without any transmission line in between. Practically however,

this is either not possible or not desirable. For example, in order to be able to perform waveform measurements, sensing couplers have to be inserted between the DUT and the impedance controlling element. Due to this offset length between the DUT and impedance controlling element and depending on the frequency of operation, a voltage standing wave is introduced. The greater the distance between the DUT and impedance controlling element, the higher the probability for peak voltages to occur within the transmission path.

The voltage standing wave along the system transmission path can be defined in terms of delivered power (please refer to appendix C for full derivations) as follows,

$$V(z) = \sqrt{\frac{2 P_d Z_o}{1 - |\Gamma_{LP}|^2}} \cdot (1 + \Gamma_{LP} e^{-2j\beta z}) \quad (4.1)$$

Here, β is transmission line propagation constant and Γ_{LP} and Γ_ℓ are the Load-pull and impedance controlling element reflection coefficients respectively (Fig. 4.6). The term $e^{-2j\beta z}$ represents the reflection coefficient phase along the system transmission path, and the maximum voltage can be written as

$$V_{\max} = \sqrt{2 P_d Z_o \text{SWR}} \quad \text{where} \quad (4.2)$$

$$\text{SWR} = \frac{1 + |\Gamma_{LP}|}{1 - |\Gamma_{LP}|}$$

Note that if Γ_{LP} in equation (4.1) is greater than 1 then in this case the load-pull source will act as generator while the DUT will act as sink and therefore the Γ_{LP} term should be replaced by $1/\Gamma_{LP}$.

To visualize the problem, consider as an example a 100W device with a 1 Ω optimum impedance, being load-pulled at 2.1 GHz using passive load-pull system. The wavelength at this frequency is $\lambda \approx 15$ cm, and plotting the voltage using equation (4.1) as a function of the electrical length (Fig. 4.7) reveals that a massive voltage peak (707 Volts) could occur within the passive system transmission path.

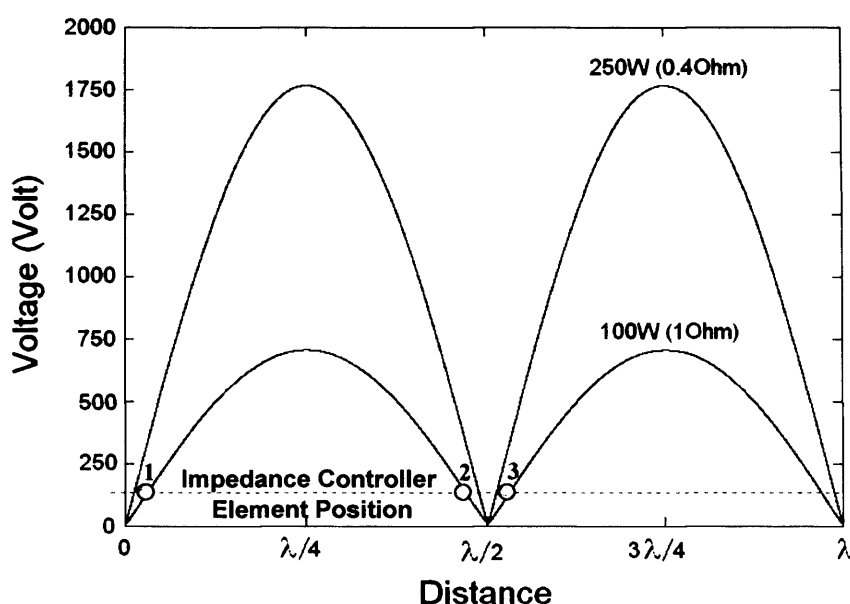


Fig. 4.7 Voltage standing wave in passive load-pull measurement system when characterizing 100 Watt (1Ω) and 250 Watt (0.4Ω) devices, similar curves obtained for active load-pull system

To avoid this massive voltage peak, the impedance controlling element would have to be placed as near as possible to the device (point 1 in Fig. 4.7).

From a practical point of view, even in pre-calibrated commercial impedance controlling tuners which avoid the need for sensing couplers; this is very difficult to achieve. Connectors and mounting board generally have to be placed between the tuner and DUT. This will force the impedance controlling element to work at either point 2 or 3 (Fig. 4.7), introducing at least one voltage peak.

A voltage breakdown between the signal line and ground may occur at this peak consequently damaging the tuner; this behaviour is conventionally described as the “Corona” effect.

This problem will get worse when emulating even lower impedances (<0.5 Ohm) for devices with higher output powers resulting in excessive peak voltages (Fig. 4.7), and leading to potential damage within the transmission path connecting the DUT and tuner. Clearly, the current approach which utilizes 50 Ohm impedance lines faces limitations when applied to high-power devices.

Note that the above SWR analysis and results are also valid for the active measurement system since the only change involves replacing the passive tuner with an active load-pull source, as will be seen in the next sub-section.

4.3.3 Load-pull Power Levels Associated with the Active Load-pull Measurement Systems

The model of Fig. 4.6 can be extended to an active load-pull measurement system by replacing the passive tuner with an active load-pull source (Fig. 4.8).

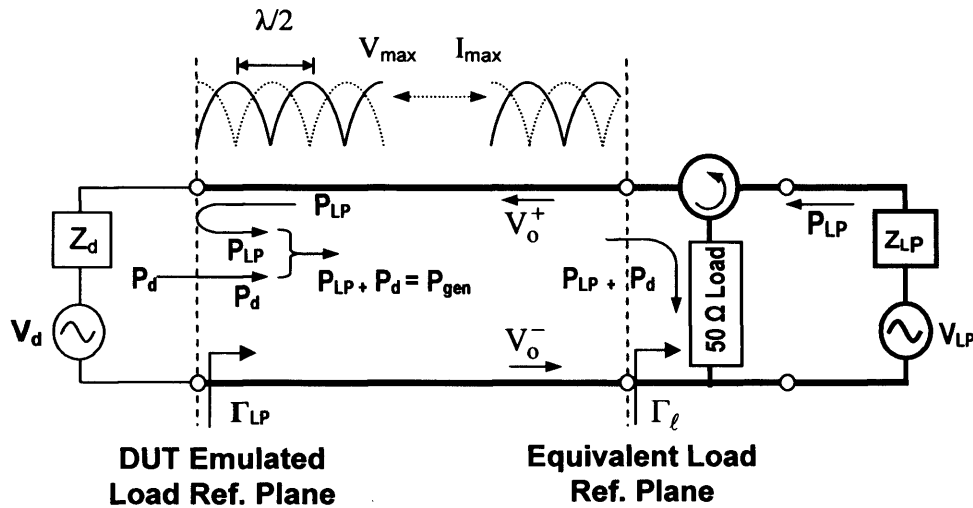


Fig. 4.8 Active load-pull measurement system model representation

In this model the load-pull source is represented as a voltage source V_{LP} in series with impedance Z_{LP} , which in this case is set to the system characteristic impedance $Z_0=50\Omega$. The circulator is inserted just before the load-pull source to dissipate the energy delivered by, and reflected back from the DUT into the 50Ω load which can be defined as $P_{LP} + P_d$. Again, in order to eliminate the voltage standing wave peak in the measurement system transmission path, the circulator would have to be placed as near as possible to the DUT. This again is not practical as in the active load-pull case, it is generally necessary and desirable to insert sensing couplers between the DUT and the active load-pull system as this allows waveform measurement. Hence such systems are subject to repeated voltage and current standing wave peaks.

For the same 100W device defined previously being actively load-pulled, the voltage standing wave across the system would have the same values to the voltage standing wave in the passive system (Fig. 4.7). In contrast to the passive load-pull measurement system however, the corona effect in the active system is minimized due to the elimination of the airline tuners, although the system is more susceptible to repetitive peaks.

The load-pulling process in active load-pull systems is achieved by injecting a phase coherent RF signal from the load-pull source (P_{LP}) to interact with the RF power wave delivered by the device (P_d).

As well as the voltage standing wave issue, the power levels can become prohibitive when extending the active load-pull measurement system to characterize high power low impedance devices.

The load-pull power problem can be quantified using the model illustrated in Fig. 4.8, since the load-pull source is connected to the measurement system via the circulator then ideally, it will see a perfect match regardless of the device condition. On the DUT side, the load-pull signal V_0^+ generated from the load-pull source will travel via the circulator, propagating towards the DUT output and combining at the DUT with the DUT output to generate the signal V_0^- . Note that the V_0^- signal passes into the circulator and gets dissipated into the load connected to the circulator.

V_0^+ relates to the load-pull power P_{LP} whilst V_0^- relates to the generated power P_{gen} . Both signals will see the same impedance which is normally set to the system characteristic impedance Z_0 (50 Ohm). Therefore V_0^+ and V_0^- could be written as a function of P_{LP} and P_{gen} respectively, as follows,

$$P_{LP} = 0.5 \cdot \text{Re}\left(\left|V_0^+\right|^2 / Z_0\right) \quad \text{and} \quad P_{gen} = 0.5 \cdot \text{Re}\left(\left|V_0^-\right|^2 / Z_0\right) \quad (4.3)$$

The synthesized load-pull reflection coefficient seen by the DUT can be written as

$$\Gamma_{lp} = \frac{V_0^+}{V_0^-} \quad (4.4)$$

Therefore Γ_{lp} in equation (4.4) can be written as

$$\left|\Gamma_{lp}\right| = \sqrt{\frac{P_{lp}}{P_{gen}}} \quad (4.5)$$

Based on the energy flow in Fig. 4.8, the following power equation can be written,

$$P_{gen} = P_{LP} + P_d \quad (4.6)$$

Since the delivered power (P_d) is directly dependant on the emulated load impedance, an expression for P_d can be written as

$$P_d = P_{av} \frac{\left(1 - \left|\Gamma_{lp}\right|^2\right)\left(1 - \left|\Gamma_d\right|^2\right)}{\left|1 - \Gamma_{lp}\Gamma_d\right|^2} \quad (4.7)$$

Where P_{av} is the maximum available power delivered by the device under optimum load (please refer to Appendix C for detailed derivations). Substituting equation (4.5) into (4.6) and re-arranging yields

$$P_{LP} = P_d \frac{|\Gamma_{LP}|^2}{1 - |\Gamma_{LP}|^2} \quad (4.8)$$

Equation (4.8) can be represented by the following signal flow graph (Fig. 4.9).

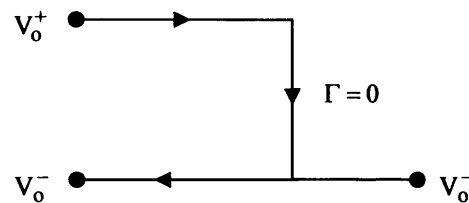


Fig. 4.9 Signal flow graph for the measurement system model of Fig. 4.8

For example, in order to load-pull the above 100W (1Ω) device, the load-pull power requirements can be plotted as a function of the emulated load reflection coefficient, as shown in Fig. 4.10 below.

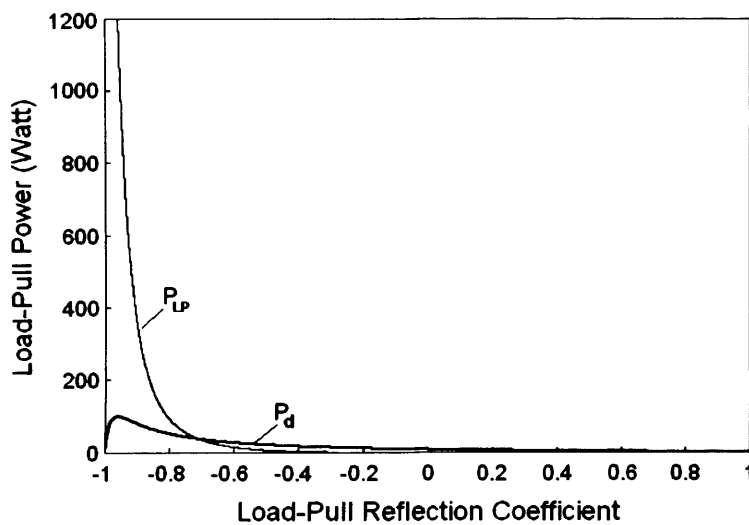


Fig. 4.10 Load-pull power requirements as a function of the emulated load-pull reflection coefficient when characterizing 100W (1Ω) device

Note that the load-pull power required to emulate such low impedance (1Ω) is 1200W [22], which represents a power level significantly larger than the device output power. Based on the example above, in such cases, it is therefore necessary to reduce the load-pull power levels and consequently the voltages in both active and passive systems down to a reasonable level if load-pull characterization of present and emerging high-power devices is to be achieved. This could be achieved by lowering

the system impedance to levels closer to the DUT impedance. This can be realized via the integration of an impedance transformer or matching network in between the measurement system and the DUT.

4.4 New Measurement System Description

A new measurement system that combines time-domain waveform and active load-pull entities has been developed, and it is based on previous open-loop system developed at Cardiff University in the past few years [17, 23].

Fig. 4.11 illustrates the block diagram of this new system, which essentially measures the absolute incident and reflected voltage waveforms at the calibrated reference plane(s), and is based around the two-channel Microwave Transition Analyser (MTA). The synthesized sweeper is used as a source signal generator, while the active load-pull system comprises a set of phase-coherent signal generators and amplifiers that are responsible for presenting the desired fundamental and harmonic impedances. With the exception of the DUT, the characteristic impedance of the system is 50 Ohm.

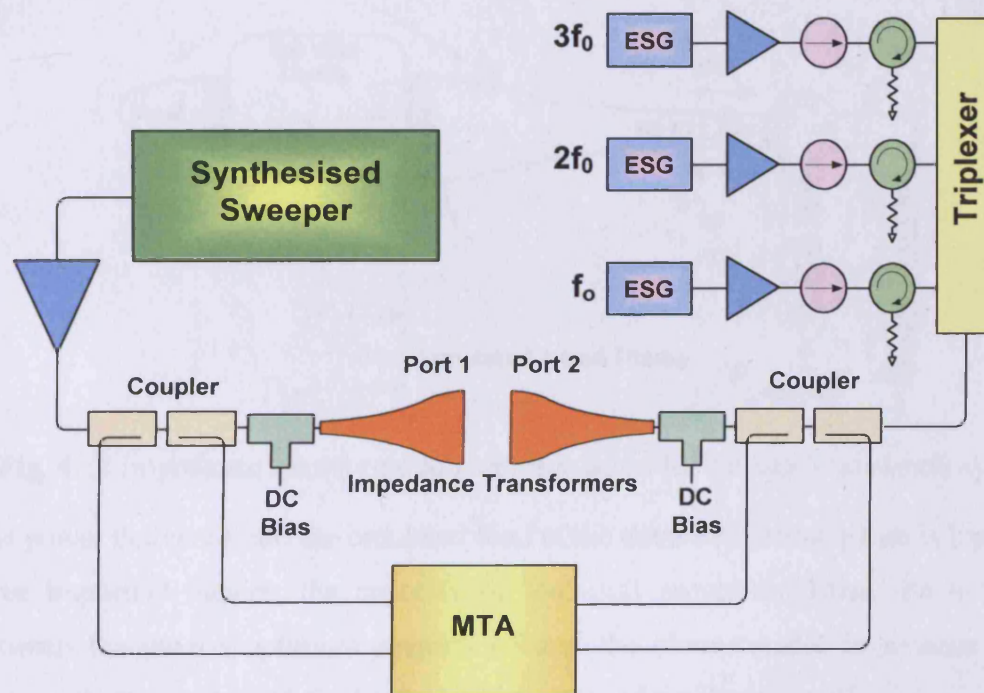


Fig. 4.11 Active load-pull measurement system including impedance transformers

The large relative difference between the system and DUT impedances effectively limits system capabilities. The system has therefore been modified to accommodate impedance transformers at the DUT input and output ports to bring the system

characteristic impedance down (device impedance up) to a level that allows high-power devices to be load-pulled quite easily.

4.5 Impedance Transformation Solution

Incorporating impedance transformers between the DUT and the load-pull measurement system changes the impedance demands on the system. This change has an immediate impact in reducing the voltage standing waves in the system as well as the required load-pull power levels.

However, introducing a matching network in the passive load-pull system limits the area of the Smith chart that can be synthesized due to the losses associated with these networks.

To analyze the impedance transformer effect, consider the model of Fig. 4.12 where a 100 Watt device is connected to the load-pull measurement system via two impedance transformers.

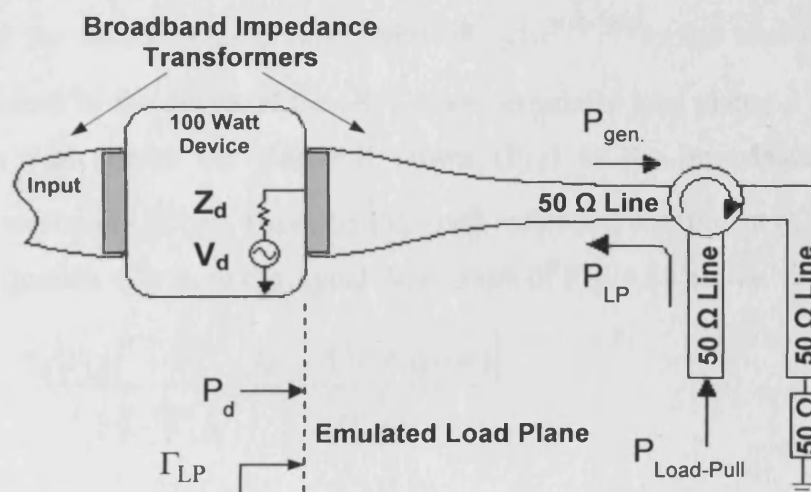


Fig. 4.12 Impedance transformation representation for the active load-pull system

The power delivered into the emulated load at the device reference plane is limited by three important factors; the capacity of load-pull power amplifier, the difference between the device optimum impedance and the characteristic impedance of the measurement system, and finally the power rating of the device itself.

The process of active load-pull involves injecting a phase coherent RF signal from the load-pull source (P_{LP}) in order to balance the RF power generated by the device (P_{gen}) such that the required load is presented. The difference $P_{gen} - P_{LP}$ gives the net power delivered (P_d) to the emulated load at the device reference plane.

The transformer effect on the load-pull power levels could be modelled and derived using the simple Signal Flow Graph (SFG) of Fig. 4.13 below.

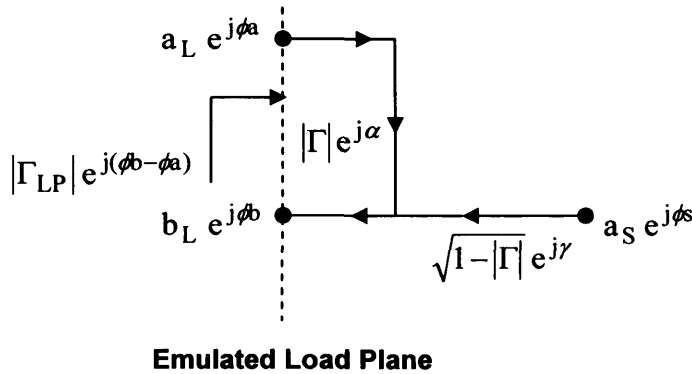


Fig. 4.13 Lossless impedance transformer signal flow graph (SFG) representation on the measurement system load side of Fig. 4.12

Where $a_S e^{j\phi_s}$ represents the injected complex signal to the transformer from the load-pull source, $|\Gamma|$ is the impedance transformer reflection coefficient which is basically a measure of the transformation ratio, while $|\Gamma_{LP}| e^{j(\phi_b - \phi_a)}$ is the load-pull reflection coefficient seen by the device at the DUT plane (emulated load plane).

A formula that relates the load-pull power (P_{LP}) to the impedance transformer reflection coefficient ($|\Gamma| e^{j\alpha}$) and the load-pull reflection coefficient ($|\Gamma_{LP}| e^{j\phi}$) can be deduced (equation 4.9) from the signal flow graph of Fig. 4.13 above.

$$P_{LP} = \frac{P_d \left(|\Gamma_{LP}|^2 + |\Gamma|^2 - 2|\Gamma_{LP}||\Gamma| \cos(\phi - \alpha) \right)}{\left(1 - |\Gamma_{LP}|^2 \right) \left(1 - |\Gamma|^2 \right)} \quad (4.9)$$

Where,

$$\phi = \phi_b - \phi_a$$

It's clear from (4.9) that the load-pull power requirements depend on the relative difference between the load-pull reflection coefficient phase ϕ and the phase of the impedance transformer reflection coefficient α . The minimum power occurs when $\phi - \alpha = 0$ and the cosine term goes to 1. Therefore in order to minimize the load-pull power requirement it is essential to have $\alpha = \phi$, which can be achieved by adding a length of the low impedance line or line-stretcher (the effect of this extra line can be easily removed using conventional TRL calibration procedure). If this is not the case, the load-pull power requirement will increase as the angle ϕ departs from α , with the resultant load-pull power being obtained from (4.9).

In order to demonstrate the impact of the impedance transformer on the load-pull measurement system, consider again the 100W (1Ω) device being load-pulled using either a passive or active load-pull measurement system. By introducing an impedance transformer between the DUT and the measurement system and applying equation (4.1), it can be observed that the voltage standing wave will decrease with an increased transformation ratio (Fig. 4.14).

Note that in the above graph the impedance transformer losses have been ignored which could create a problem for passive load-pull systems.

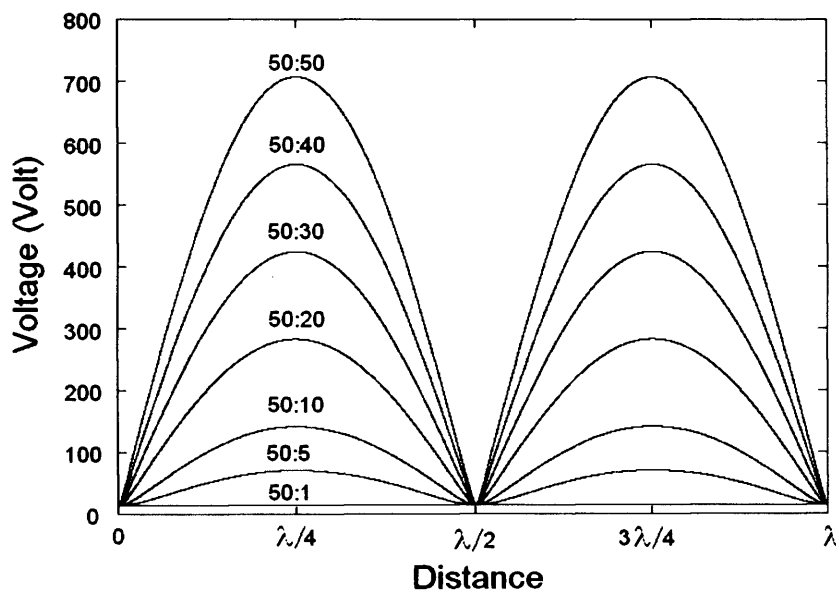


Fig. 4.14 Voltage standing wave for different transformation ratios in the active and passive load-pull measurement systems, when characterizing a 100 Watt (1Ω) device

In addition, in the case of active load-pull systems, the impedance transformer also reduces the load-pull power demand when synthesizing different load impedances. Consider the same 100 Watt device specifications when substituted into equation (4.9) while setting the cosine term to unity (optimal condition) and plotting the results for different transformation ratios as shown in Fig. 4.15 below. Note that the delivered power curve (P_d) was calculated using equation (4.7) and added for clarification.

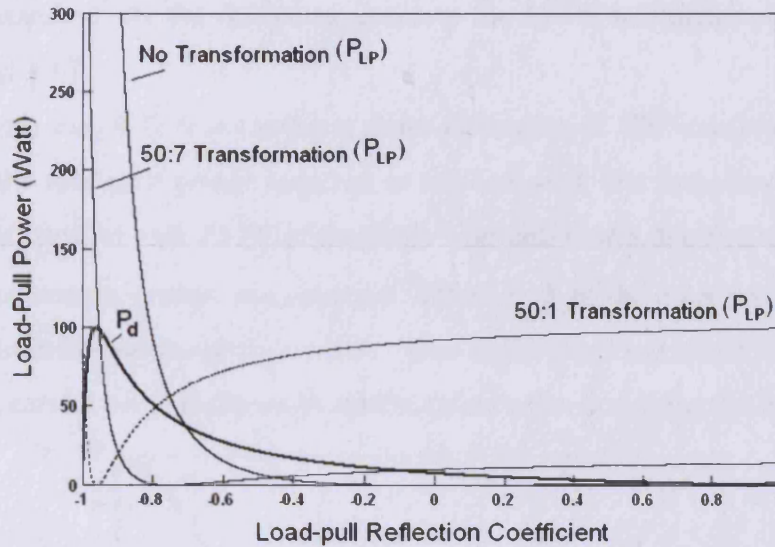


Fig. 4.15 Load-pull power levels vs synthesized load-pull reflection coefficients using different transformation ratios for 100W (1 Ω) device

Similarly, using equation (4.9), another useful result that summarises the relationship between load-pull power requirement and impedance transformation ratios, can be obtained and is shown in Fig. 4.16 below.

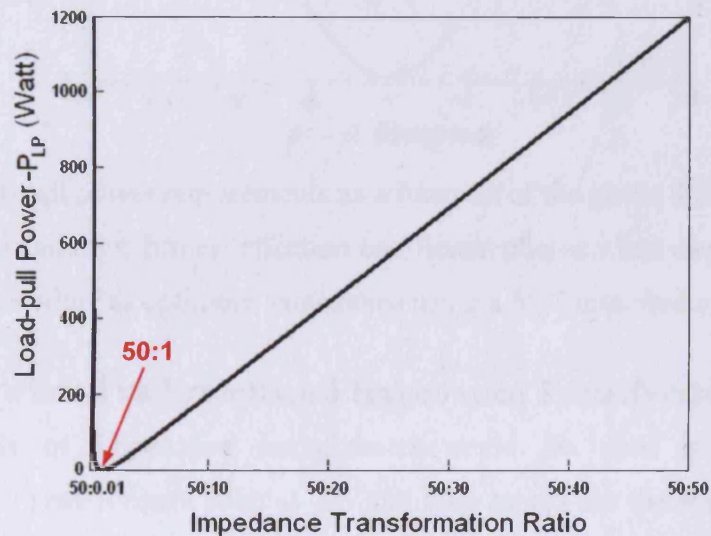


Fig. 4.16 Load-pull power requirements vs impedance transformation ratio when characterizing 100W transistor with 1 Ω optimum load impedance

Using equation (4.9) and fixing the magnitude values of the load-pull and transformer reflection coefficient while sweeping the relative phase difference between transformer and optimum load, the phase alignment sensitivity on the load-pull power requirements can also be quantified. The power necessary to emulate the load

impedance required for the device to generate the 100W maximum rated power is shown in Fig. 4.17.

It is clear from Fig. 4.17 that having a phase difference of 180° can result in a huge increase to the load-pull power required to emulate such low impedances. However for a load-pull system with 200W of available load-pull power, the above result shows that the measurement system can function within $\pm 10^\circ$ of the optimum phase, hence location of transformer is not so critical. This angle is a function of transformation ratio, hence, careful considerations should be taken when designing the transformer.

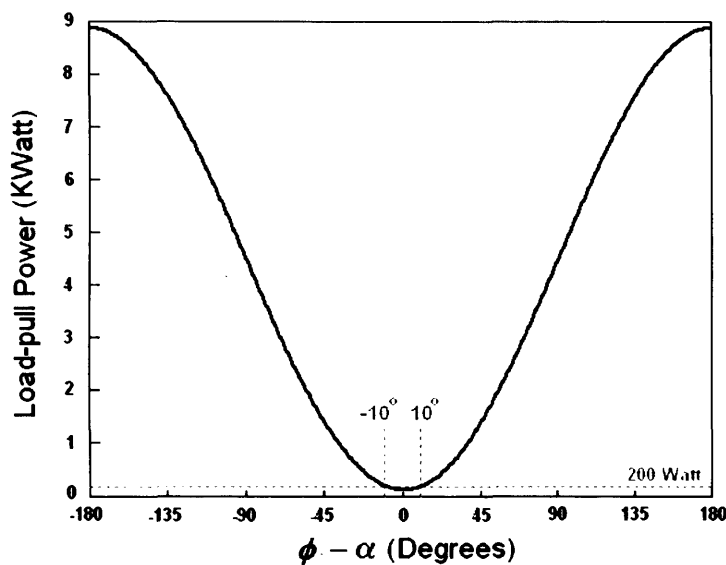


Fig. 4.17 Load-pull power requirements as a function of the phase difference between the load-pull and transformer reflection coefficient phases when characterizing a 100W device with 1Ω optimum impedance using a 50:7 impedance transformer

4.5.1 Narrowband vs Broadband Impedance Transformers

Different kinds of impedance transformers could be used as a means of transformation. Transformers such as $\lambda/4$ and stub tuners are the simplest, but they are relatively narrow-band, and when it comes to load-pulling the device over several harmonics, these transformers become very difficult to control and calibrate. As a result, these transformers are very limited when it comes to performing time domain waveform measurements.

One solution is to use broadband impedance transformers. These cover a wide frequency bandwidth, and since these transformers are resonance-free, the system can be calibrated using standard calibration procedures. Consequently, this approach

allows the direct measurement of the waveforms at the device reference plane, as well as making the harmonic load-pull process more flexible.

4.5.2 Optimum Impedance Transformer Design

Initial analysis might suggest that a high transformation ratio may be optimal. For example, a 50:1 transformation ratio would require no power to load-pull the 100 W (1Ω) device (Fig. 4.16). However, in this case the load-pull measurement system power demand could be significantly increased if the optimum deviates slightly from the 1 Ohm point. In practice, characterizing unknown devices using a high transformation ratio is problematic since the device optimum impedance is unknown. In order to understand the effect of the impedance transformer, “constant load-pull contours (P_{LP})” can be derived. These define the area on the Smith Chart where the optimum device impedance can be located for a given available load-pull power.

Analysis indicates that for constant P_{LP} and P_d , equation (4.9) transforms to circular contours around the centre on a Smith chart normalized to the transformer characteristic impedance. This can then be re-mapped onto the 50 Ohm impedance Smith Chart producing contours about the impedance transformer reflection coefficient. To determine the location of the contour on the Smith Chart real axis, define K as

$$K = \frac{P_d}{P_{LP}} \quad (4.10)$$

Substituting equation (4.10) into (4.9) and solving for Γ_{LP} with $\cos(\phi - \alpha) \rightarrow 1$ gives,

$$\Gamma_{LP} = \frac{K \cdot \Gamma \pm (1 - \Gamma^2) \sqrt{1 + K}}{1 + K - \Gamma^2} \quad (4.11)$$

Equation (4.11) thus gives the two values which represent the contour crossing points on the Smith Chart real axis. When no impedance transformation is present, or for a 50:50 impedance transformer, $\Gamma \rightarrow 0$ and equation (4.11) reduces to

$$\Gamma_{LP} = \pm \frac{1}{\sqrt{1 + K}} \quad (4.12)$$

To visualize the problem, consider a load-pull measurement system with 200W maximum available load-pull power that is used in characterizing a 100W transistor using a 50:7 impedance transformer. Plotting the circles using (4.11) and (4.12) on the Smith Chart reveals the results shown in Fig. 4.18 below.

The area inside each circle (Fig. 4.18) represents the capability of the load-pull measurement system to present the optimum load impedance to the device in order for the device to generate its maximum rated power (P_d).

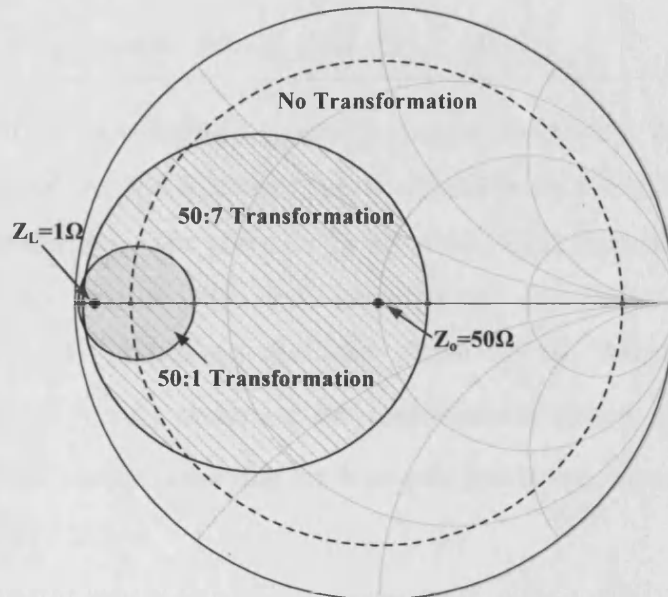


Fig. 4.18 Areas covered by the load-pull measurement system for $P_{LP(max)}=200W$, when characterizing 100 Watt device with and without using impedance transformer

It's clear that using an impedance transformer will limit the area on Smith Chart that can be synthesized by the load-pull measurement system. This is especially true for high-impedance transformation ratios where, if the optimum is misjudged, the reduced load-pull power demand advantage of using the transformer will be completely eliminated.

Therefore, for an unknown device, a coarse scan without the impedance transformer may become necessary in order to identify in which quarter of Smith Chart the optimum impedance is located. With this known, the appropriate offset impedance transformer could then be designed.

4.6 System Mismatch Issue

In practice, measurement systems do not present a perfect 50 Ohm match, hence the system reflection coefficient (Γ_L) is not zero. This effect, ignored in the previous analysis, was included in the full formulation (D.7) derived in appendix D which is restated here for simplicity (4.13).

$$\begin{aligned}
 P_{LP} = P_d [& |\Gamma_{LP}|^2 + |\Gamma|^2 + |\Gamma_L|^2 + |\Gamma_{LP}|^2 |\Gamma|^2 |\Gamma_L|^2 - 2|\Gamma_L| \cdot |\Gamma| \cdot (1 + |\Gamma_{LP}|^2) \cdot \cos(\beta + \phi_L) \\
 & - 2|\Gamma_{LP}| \cdot |\Gamma| \cdot (1 + |\Gamma_L|^2) \cdot \cos(\phi - \alpha) + 2|\Gamma_{LP}| \cdot |\Gamma_L| \cdot |\Gamma|^2 \cdot \cos(\beta + \phi_L + \phi - \alpha) \\
 & - 2|\Gamma_{LP}| \cdot |\Gamma_L| \cdot \cos(\phi - 2\gamma - \phi_L)] / (1 - |\Gamma|^2)(1 - |\Gamma_{LP}|^2) \tag{4.13}
 \end{aligned}$$

Consider the affect of utilizing a typically mismatched system where $\Gamma_L=0.1$, for the characterization of the 100W device specified previously using 50:7 Ohm broadband impedance transformer. The phase α in equation (4.13) is usually set to π since the transformer only works on real impedances, and this implies the phase difference $\phi - \alpha = 0$. Assuming that the phase of the transformer transmission coefficient (γ) is $\gamma = \pi$, sweeping the measurement system reflection coefficient phase ϕ_L in (4.13) while observing the load-pull power requirements gives the results shown in Fig. 4.19 below.

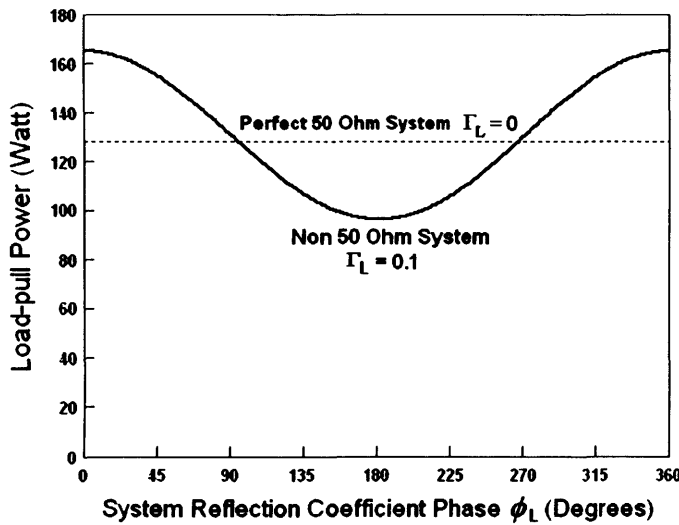


Fig. 4.19 Load-pull power requirements as a function of measurement system reflection coefficient ($\Gamma_L=0.1$) phase ϕ_L compared to a perfect 50 Ohm system (50:7 Ohm impedance transformer and 100W, 1Ω device assumed)

Therefore a small difference in the system reflection coefficient (Fig. 4.19) if it is not correctly accounted for, can dramatically increase the load-pull power requirement. On the other hand this mismatch problem could be used to further help reduce the load-pull power requirements by introducing the hybrid measurement system discussed below.



4.7 Hybrid Load-pull Measurement System

It is possible to exploit the system impedance mismatch by using a set of tuneable impedance transformers in the load-pull system to deliberately offset the system impedance as shown in Fig. 4.20 below.

Here, the measurement system is equipped with tuneable impedance transformers in an attempt to develop a hybrid load-pull measurement system comprising both passive and active load-pull elements into one unified, powerful measurement system. This additional feature can further reduce the load-pull power requirements when characterising high-power devices, which is of particular benefit when the system load-pull source has limited power rating.

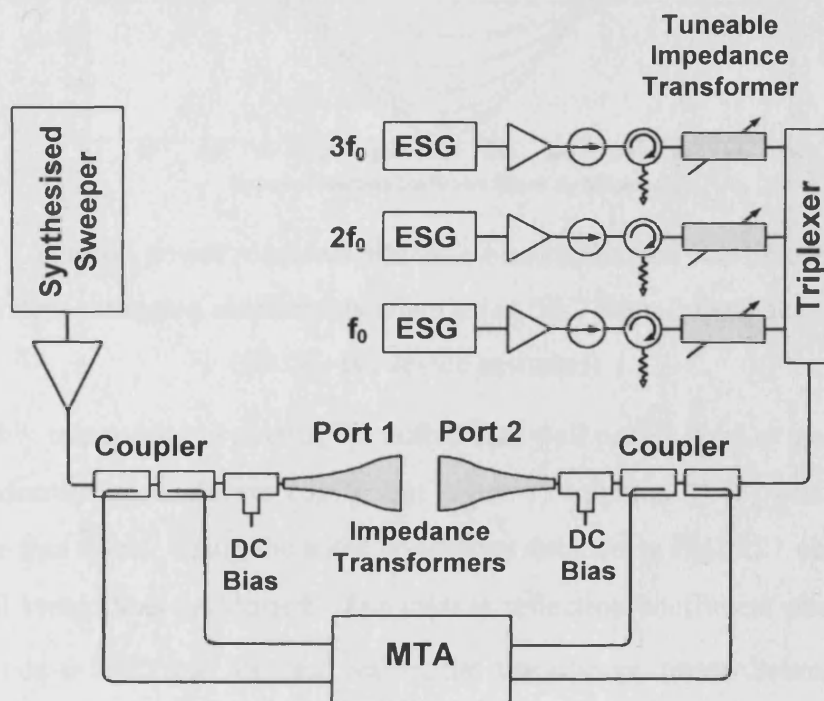


Fig. 4.20 Impedance controlling element integration into an active load-pull measurement system

In this case, a deliberately introduced mismatch can be utilised to reduce dramatically the load-pull power requirement. For example, when load-pulling a 100W (1Ω) device using a measurement system with $\Gamma_L=0.754$ and a pair of transformers with $\sim 7:1$ transformation ratio, zero load-pull power will be required to emulate such low impedance. Again, to illustrate the principle idea, any losses within the transmission path have been omitted.

It can be seen that increasing the system reflection coefficient magnitude will result in load-pull power requirements that vary more significantly with phase changes in the system reflection coefficient (Fig. 4.21).

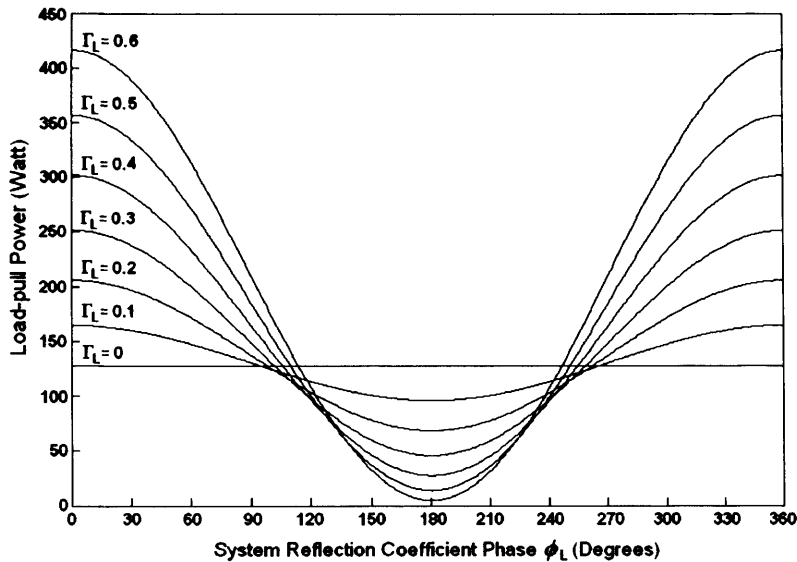


Fig. 4.21 Load-pull power requirements vs. system reflection coefficient phase for different system reflection coefficients when using 50:7 Ohm impedance transformer (100W, 1Ω device assumed)

In such highly mismatched systems, the active load-pull power level is more sensitive to the transformer transmission coefficient phase γ , equation (4.13) can be used to demonstrate this effect. Using the same conditions detailed in Fig. 4.21 above, a two-dimensional sweep was performed. The system reflection coefficient phase ϕ_L was swept between 0-360° and for each value, the transformer transmission coefficient ($\Gamma_L=0.1$) phase γ was swept between 0-180°. At each of these values the load-pull power was calculated and plotted as shown in Fig. 4.22 below.

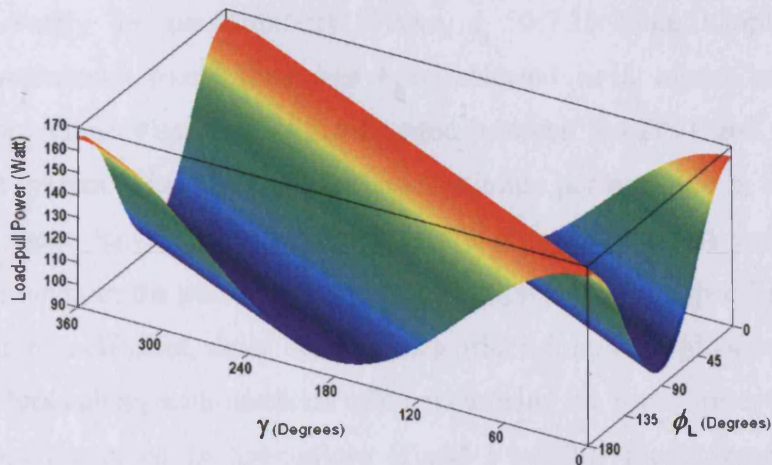


Fig. 4.22 Load-pull power level as a function of the load-pull measurement system reflection coefficient phase ϕ_L and transformer transmission coefficient phase γ , (100W, 1 Ω device and $\Gamma_L=0.1$ assumed)

It can be clearly observed that γ has a significant impact on the load-pull power requirements. However, adding a line stretcher between the measurement system and the DUT test fixture alleviates this problem by adjusting the system reflection coefficient phase such that when combined with γ , and the transformer reflection coefficient phase (β), the minimum load-pull power levels can be practically achieved. Otherwise, the tuneable impedance controlling element phase can be adjusted accordingly to solve this problem.

4.8 Measurement System Calibration

Using the calibration analysis presented in chapter 2 of this thesis, a 2-tier calibration approach was adopted to calibrate the load-pull measurement system presented above. The first tier involves calibrating the system up to the coaxial reference plane using traceable coaxial standards. Also, during this calibration step, an additional non-linear calibration technique which involves separating the transmission and tracking error coefficients is applied. This extra step has been termed “Full calibration” which means all measurement system error coefficients can be quantified individually. Although this extra calibration step is used in the measurement of the active devices discussed in this thesis, its details is beyond the scope of this thesis, and is comprehensively documented elsewhere [17].

The second tier of the calibration involves calibrating the system up to the DUT reference plane. For this step, a standard TRL calibration [24, 25] has been used.

In order to verify the measurement system, a 50:7.15 Ohm Klopfenstein [26] broadband impedance transformer has been selected as a means of impedance transformation. These transformers are inserted between the DUT and the load-pull measurement system (Fig. 4.11), and deliver optimum performance in the sense that for a given taper length, they have the minimum magnitude of input reflection coefficient throughout the pass-band. At the same time, and for a specified magnitude of the reflection coefficient, these transformers offer a minimum physical length. The design procedures along with methods of characterising the transformer characteristic impedance are presented in appendices E and F of this thesis respectively. The measured transformer characteristic impedance (low-impedance side) was found to be 7.15 Ohm at 2GHz. The measurement system test fixture setup is shown in Fig. 4.23 below.

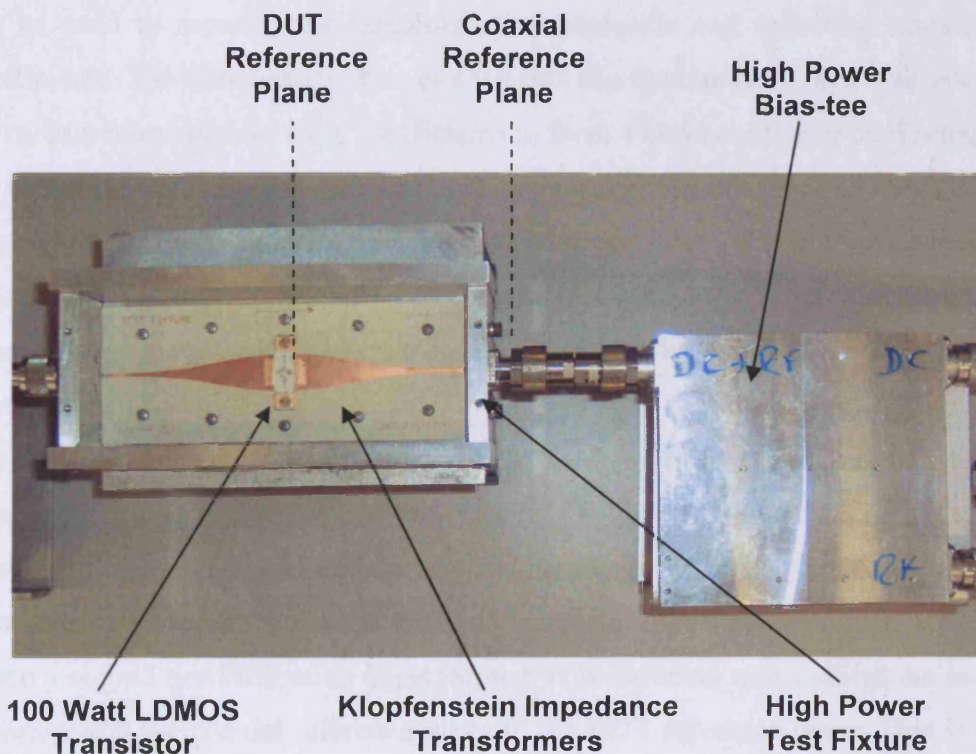


Fig. 4.23 High-power test fixture suitable for measuring high power devices (>100W)

Since the calibration procedures involve a 2-tier calibration, in the first tier the measurement system was calibrated using N-type coaxial TRM calibration up to the system coaxial ports (reference plane). This calibration step is already a function of the measurement software and is able to remove all systematic errors and account for any switching effects. Following this step, the system was considered to be calibrated to international traceable standards specified by NIST. Standard verification

procedures were adopted to check the calibration quality, and this included the measurement of standards different to those used in the calibration itself.

The second step (tier) involved TRL calibration using in-fixture standards attached to broadband impedance transformers in order to remove the errors associated with components of the test fixture, including the impedance transformers themselves as well as the launchers that attach to them. The certainty of this calibration step is subject to the calibration standards quality and their characteristic impedance measurement accuracy.

One of the advantages of a 2-tier calibration approach is that TRL calibration only needs to be performed once, because the error coefficients that describe the actual test fixture s-parameters are constant. Since the calibration deals with passive components only, the lossless reciprocal network analysis presented in appendix B of this thesis can be used to separate the transformer transmission and reflection tracking error coefficients. The transformer error coefficients can then be combined (cascaded) with the measurement system error coefficients to form a new set of error coefficients (Fig. 2.9.c) which represent the measurement system and the test fixture. This calibration step will move the measurement reference plane up to the DUT reference plane.

This 2-tier approach also allows the immediate switching between the measurement observations at two different reference planes. The embedding techniques are presented in Chapter 2 of this thesis.

The measurement system presented so far is capable of performing time domain waveform measurements. When the system is calibrated up to the coaxial reference plane, the measured waveforms at that plane are normalised to the calibration standards characteristic impedance, which is usually a nominal 50 Ohms.

When a second tier calibration is performed, it is desirable to transform the measured waveforms at the coaxial reference plane to the DUT reference plane. This is usually done by cascading the error coefficients for the two tier calibration using T-matrix format to form a new, combined error model. Consequently, the waveforms at the device plane can be extracted. Another method which works directly on waveforms is by using the ABCD matrix analysis, which works directly with currents and voltages, Consider the measurement system test fixture representation in terms of ABCD matrix and voltage and current nodes shown in Fig. 4.24 below.

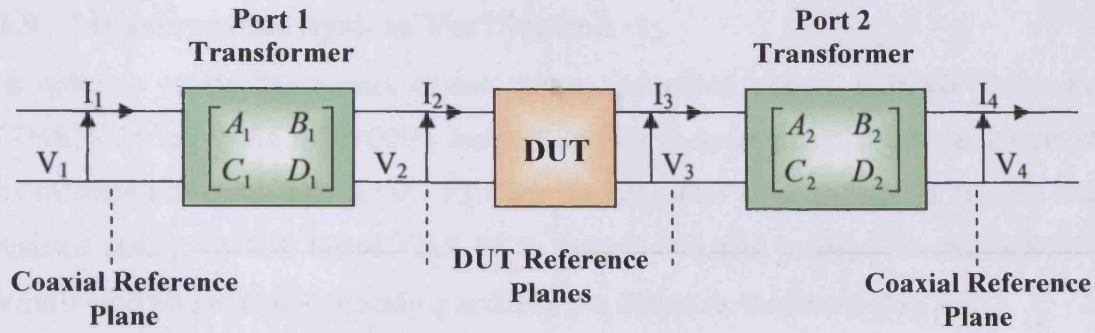


Fig. 4.24 Measurement system test fixture representations in terms of ABCD matrix and voltage and current waveforms

Having determined the transformer characteristic impedance, the S to ABCD parameters conversion can be written as [27],

$$A = \frac{(1 + S_{11})(1 - S_{22}) + S_{12}S_{21}}{2S_{21}}$$

$$B = Z_0 \frac{(1 + S_{11})(1 + S_{22}) - S_{12}S_{21}}{2S_{21}}$$

$$C = \frac{1}{Z_0} \frac{(1 - S_{11})(1 - S_{22}) - S_{12}S_{21}}{2S_{21}}$$

$$D = \frac{(1 - S_{11})(1 + S_{22}) + S_{12}S_{21}}{2S_{21}}$$

Where Z_0 in the above equations represent the impedance transformer characteristic impedance. If (V_1, I_1) and (V_4, I_4) are the voltage and current waveforms measured at the measurement system input and output coaxial reference planes respectively. In order to transform these waveforms to the DUT reference planes and obtain the voltage and current waveforms (V_2, I_2) and (V_3, I_3) at the DUT input and output reference planes respectively, the following equations can be applied.

$$\text{For input taper, } \begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} \Rightarrow \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix}^{-1} \begin{bmatrix} V_1 \\ I_1 \end{bmatrix} \quad (4.14)$$

$$\text{For output taper, } \begin{bmatrix} V_3 \\ I_3 \end{bmatrix} = \begin{bmatrix} A_2 & B_2 \\ C_2 & D_2 \end{bmatrix} \begin{bmatrix} V_4 \\ I_4 \end{bmatrix} \quad (4.15)$$

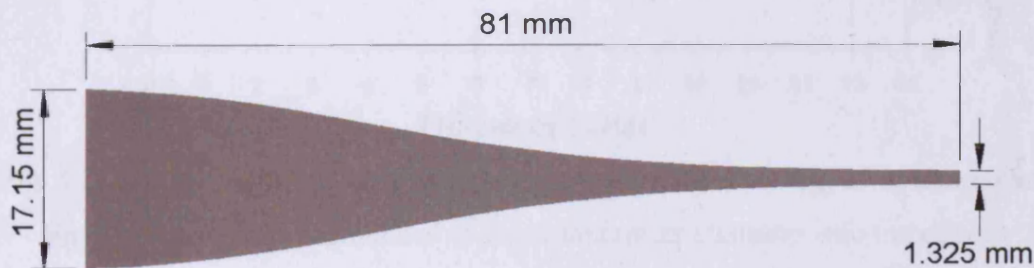
4.9 Measurement System Verification

In order to verify the measurement system presented above, a 100W Freescale LDMOS device (MRF5S21100H) was selected for measurements to test the system at its extreme limits. Firstly a 50:7.15 Ohm Klopfenstein taper (81mm in length) was realised using TMM4 board (D.K.=4.5, $\tan\delta=0.002$ and voltage breakdown=750 V/mil) with 68 μm copper cladding and 762 μm dielectric thickness (Fig. 4.23).

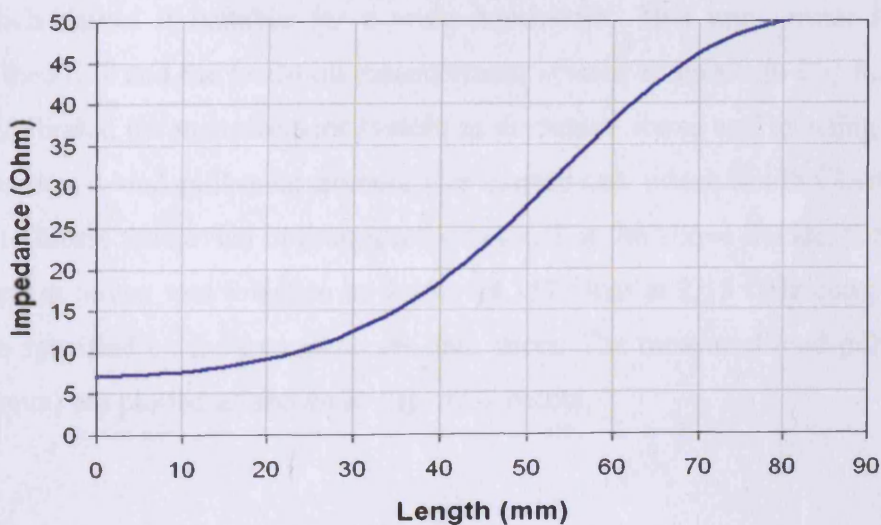
The transformer impedances is first calculated as a function of transformer length using the analysis and associated MathCAD program presented in appendix E of this thesis. This program will generate a set of points where the impedance is calculated for each point (impedance step).

Using these impedances Agilent LineCalc program was used to calculate the equivalent transformer width at each impedance step. These points are collected in a table format and then drawn in AutoCAD software against transformer length steps.

The transformer used in the test fixture setup of Fig. 4.23 was designed and realised as shown in Fig. 25 below.



(a)



(b)

Fig. 25 Klopfenstein impedance transformer a) physical layout realised in the test fixture setup of Fig. 4.23, b) transformer impedance as a function of its length

The impedance transformer was simulated using HFSS in order to obtain its s -parameters; and these simulation results are compared to measured values (Fig. 4.26). Note that the transformer measured values are obtained by calibrating the 8510 VNA up to the coaxial reference plane, then a 2nd tier TRL calibration was performed using transformer TRL calibration standards. The obtained TRL error coefficients represent the actual response of the transformer.

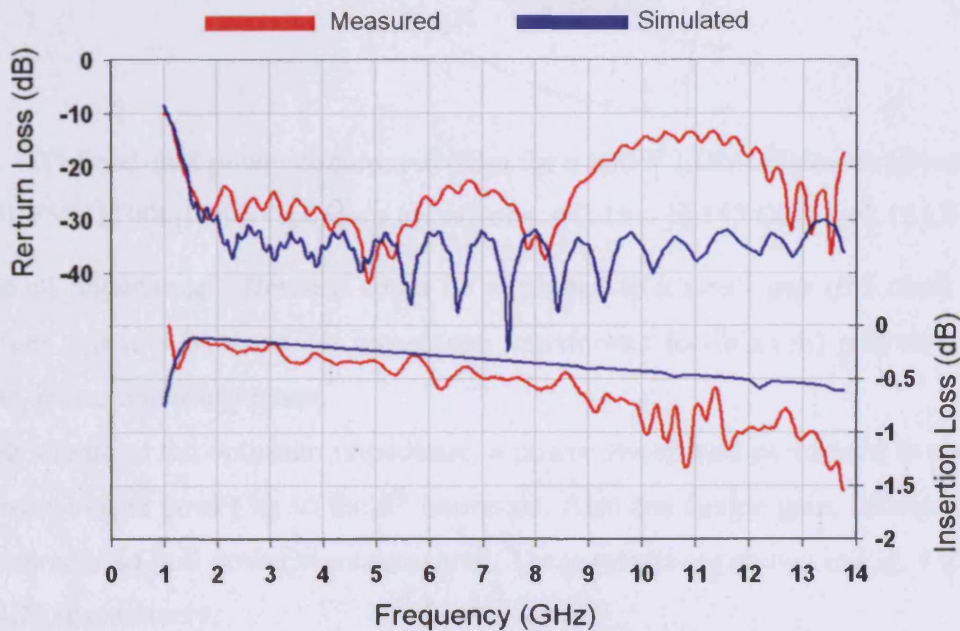


Fig. 4.26 50:7.15 Ohm (81 mm long) Klopfenstein taper of Fig. 25 measured and simulated response normalised to the transformer characteristic impedance

The results of Fig. 4.26 show very good transformer response (broadband with low loss) which makes it suitable for a wide bandwidth. This transformer is inserted between the DUT and the load-pull measurement system as shown in Fig. 4.23.

Having calibrated the measurement system as discussed above and by using the above configurations, a load-pull measurement was carried out, where Smith Chart had been scanned to locate the device optimum impedance. For the above device, the optimum for maximum power was found to be $2.18 - j4.157$ Ohm at 2.15 GHz compared to $2 - j2.9$ Ohm specified by the manufacturer data sheet. The measured load-pull contours (P_d Contours) are plotted as shown in Fig. 4.27 below.

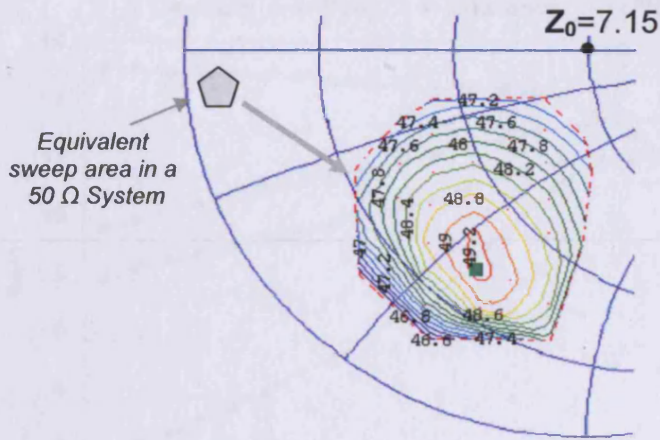


Fig. 4.27 Load-pull power contours in dBm for a 100W LDMOS device (freescle MRF5S21100H) with Optimum impedance of $2.18 - j4.157$ Ohm at 2.15 GHz

The small impedance difference could be attributed to a small gap (0.5 mm) in the mounting structure between the impedance transformer (calibration) reference plane and the device under test plane.

Having identified the optimum impedance, a power sweep was performed to measure the device output power up to the 5th harmonic. Also the device gain, efficiency and the required load-pull power were measured. These results are shown in Fig. 4.28 and Fig. 4.29 respectively.

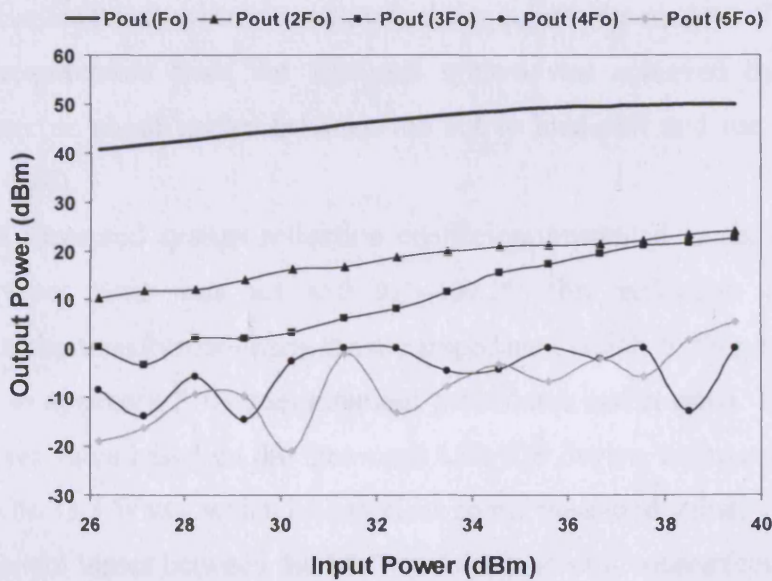


Fig. 4.28 Measured output harmonic power for a 100W LDMOS device (freescle MRF5S21100H)

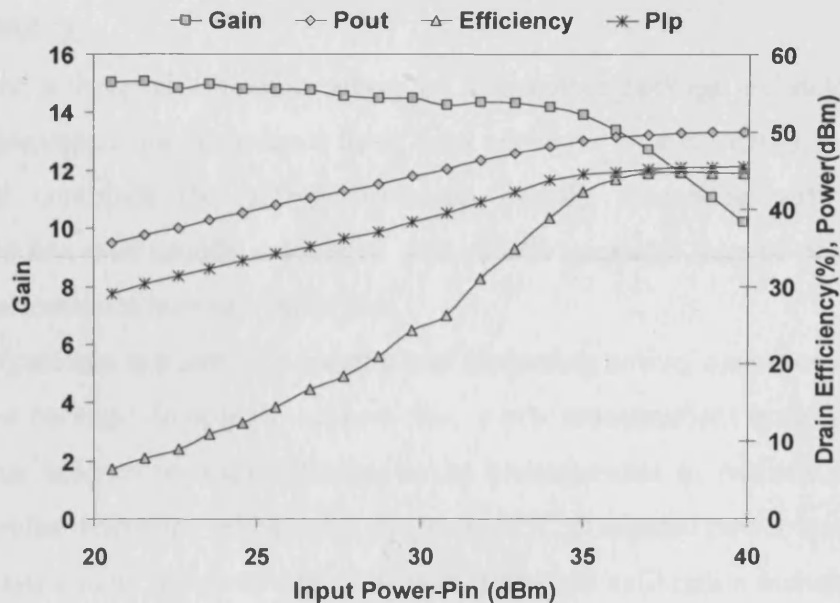


Fig. 4.29 Measured Pout (at f_0), Efficiency, Gain and Load-pull power (P_{LP}) vs Pin when load-pulling the device to its optimum impedance thus delivering over 100W

The results of

Fig. 4.29 also show the load-pull power required (P_{LP}) for the Pout versus Pin (drive power at the transistor input) measurements. It is worth noting that the maximum measured device delivered output power was $P_d=103W$ and only 35.5W was required from the active load-pull system to emulate the required impedance. This relatively low power requirement from the load-pull system was achieved by deliberately placing a tuner or phase shifter between the active load-pull and the measurement system (Fig. 4.20).

The resultant measured system reflection coefficient presented to the device at the device reference plane was set to $0.19\angle -109.2^\circ$; this reflection coefficient is normalized to the transformer characteristic impedance which is found to be 7.15Ω (please refer to appendix F for measurement procedures and results). The calculated load-pull power value based on the measured LDMOS device, using equation (4.13), was found to be 33.3 Watts, which is very close to the measured value.

Due to the system losses between the DUT and the load-pull source (couplers, cables, circulator, etc...), an extra 1.8 dBm was required from the load-pull source to compensate these losses. As a result the load-pull source had to deliver 50 Watt in total in order to synthesis the necessary load at the DUT plane.

4.10 Summary

In this chapter, a thorough literature survey of high-power package technologies and associated characterisation techniques have been presented in great detail. A package solution that combines the high-performance usually associated with ceramic packages, and low-cost usually associated with plastic packages, can be achieved by using high performance laminate materials.

The ultimate package test involves placing and measuring active, operational devices inside the new package. In order to achieve this, a new measurement system has been developed that enables packaged devices to be characterized in realistic operating conditions, whilst delivering realistic RF output and DC dissipated power levels.

The new measurement system is equipped with advanced calibration techniques that enabled measurements to be performed at a defined coaxial plane, as well as at the device-package plane through the use of multi-tier calibration. The new measurement system is also capable of measuring voltage and current waveforms at different reference planes. This was achieved through the use of ABCD matrix techniques to shift the measurement reference plane from the coaxial reference plane to the device-package reference plane.

Advanced techniques have also been applied with an aim to reduce the power required to load-pull high power devices. This was achieved by using broadband impedance transformers which enabled the necessary power reduction, as well as allowing calibration of the system up to the device reference plane, over a wide frequency bandwidth. Further power reduction was achieved by utilizing a hybrid measurement system in which passive load-pull techniques were embedded into the active load-pull system in order to optimise the system power performance, whilst maintaining accurate calibration across the entire bandwidth (up to 12 GHz).

4.11 References

- [1] F. Lepine, A. Adahl, and H. Zirath, "L-Band LDMOS Power Amplifiers Based on an Inverse Class-F Architecture," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, pp. 2007-2012, 2005.
- [2] K. W. Corporation, *LDMOS Packages High-Power Amplifiers, Push-pull Devices*: Product Information Sheet.
- [3] P. Semiconductor, "SOT540A Package Outline," *Ceramic Package Data Sheet*, January 2000.
- [4] J. McCaffrey, P. Piel, K. Tilley, and M. Williams, "RF Power Devices Meet Wireless Challenges Head On," *Microwave and RF Online Journal*, pp. 1-3, July 2006.
- [5] P. M. Fabis, "Thermal Engineering of Electronics Packages Using CVD Diamond," *Proceedings, International Symposium on Advanced Packaging Materials: Processes, Properties and Interfaces.*, pp. 125 - 132, March 1999.
- [6] N. Chen, H. Lin, and J. Lai, "Cost-Effective Chip-on-Hest Sink Leadframe Package for 800-Mb/s Applications," *IEEE Transactions on Advanced Packaging*, vol. 29, pp. 364 - 371, May 2006.
- [7] H. Shaukatullah, M. A. Gaynes, and L. H. White, "Thermal Enhancement of Surface Mount Electronic Packages with Heat Sinks," *Proceedings, Electronic Components and Technology Conference, 43rd*, pp. 256 - 263, June 1993.
- [8] K. Chen, H. Li, T. Nemoto, S. Huang, and T. Fukui, "Development of Novel Packaging Structures, Encapsulation Process, Materials and Reliability for Matrix Array Over-Molded Flip Chip CSP," *IEEE/CPMT/SEMI 29th International Electronics Manufacturing Technology Symposium*, pp. 119 - 123, July 2004.
- [9] A. K. Knudsen, K. E. Howard, J. Braley, D. Magley, and H. Yoshida, "Reliability, Performance and Economics of Thermally Enhanced Plastic Packages," *IEMT/IMC Symposium, 2nd*, pp. 374 - 379, April 1998.
- [10] D. Boulon and H. Safar, "Plastic Packages Take On High-Power Devices," *Microwave and RF Online Journal*, pp. 1-2, February 2004.
- [11] J. M. Nebus, P. H. Bouysse, J. M. Coupat, and J. P. Villotte, "An active load-pull set-up for the large signal characterization of highly mismatched microwave power transistors," *IEEE Instrumentation and Measurement Technology Conference*, pp. 2 - 5, May 1993.
- [12] T. Liang, J. Pla, and M. Mahalingam, "Electrical Package Modeling for High Power RF Semiconductor Devices," *IEEE Radio and Wireless Conference*, pp. 359 - 362, August 1998.
- [13] J. E. Müller and B. Gyselinckx, "Comparison of active versus passive on-wafer load-pull characterisation of microwave and MM-wave power devices," *IEEE MTT-S International Microwave Symposium Digest*, pp. 1077-1080, 1994.
- [14] F. Microwaves, "Prematching Tuners for Very High SWR and Power Load Pull Measurements," *Microwave Journal*, pp. 176 - 178, January 2000.
- [15] M. M. Corporation, "Device Characterization with Harmonic Source and Load Pull," *Application Note 5C-044*, December 2000.
- [16] F. Microwave, "Load Pull Measurements on Transistors with Harmonic Impedance Control," *Technical Note*, August 1999.
- [17] J. Benedikt, R. Gaddi, P. J. Tasker, and M. Goss, "High-power time-domain measurement system with active harmonic load-pull for high-efficiency base-

- station amplifier design," *IEEE Transactions on Microwave Theory and Techniques*, vol. 48, pp. 2617 - 2624, December 2000.
- [18] D. Barataud, M. Campovecchio, and J. M. Nebus, "Optimum Design of Very High-Efficiency Microwave Power Amplifiers Based on Time-Domain Harmonic Load-Pull Measurements," *IEEE Transactions on Microwave Theory and Techniques*, vol. 49, pp. 1107-1112, June 2001.
- [19] R. B. Stancliff and D. P. Poulin, "Harmonic load-pull," *IEEE MTT-S International Microwave Symposium Digest*, vol. 79, pp. 185 - 187, April 1979.
- [20] P. Bouysse, J. M. Nebus, J. M. Coupat, and J. P. Villotte, "A Novel, Accurate Load-Pull Setup Allowing the Characterisation of Highly Mismatched Power Transistors," *IEEE Transactions on Microwave Theory and Techniques*, vol. 42, pp. 327 – 332, February 1994.
- [21] R. Larose, F. M. Ghannouchi, and R. G. Bosisio, "A New Multi- Harmonic Method for Non Linear Device Characterisation and Modeling," *IEEE MTT-S International Microwave Symposium Digest*, 1990.
- [22] Z. Aboush, J. Lees, J. Benedikt, and P. Tasker, "Active Harmonic Load-pull for Characterizing Highly Mismatched High Power Transistors," *IEEE MTT-S International Microwave Symposium Digest*, pp. 1311-1314, June 2005.
- [23] J. Benedikt and P. J. Tasker, "High-power time-domain measurement bench for power amplifier development," *ARFTG Conference Digest, Fall 2002. 60th*, pp. 107 - 110, December 2002.
- [24] G. F. Engen and C. A. Hoer, "'Thru-Reflect-Line:' An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer," *IEEE Transactions on Microwave Theory and Techniques*, vol. 27, pp. 987-993, December 1979.
- [25] D. Rytting, "Appendix to an analysis of vector measurement accuracy enhancement techniques," *Hewlett-Packard RF Microwave Symposium Digest*, pp. 1-42, March 1982.
- [26] R. W. Klopfenstein, "A transmission line taper of improved design," *Proceedings IRE.*, vol. 44, pp. 31-35, January 1956.
- [27] D. M. Pozar, *Microwave Engineering*: John Wiley, ISBN 0-471-17096-8.

CHAPTER 5

HIGH-POWER PACKAGE DESIGN AND MEASUREMENTS

In this chapter a high power laminate based package design is presented. Thermal analysis is also carried out to explore the maximum power rating of the device to be placed inside. The new measurement system described in the previous chapter was setup and equipped with new impedance transformers to enable the measurement of the developed high power package.

5.1 High-Power Package Description

The high power package presented in this thesis utilises a high performance laminate (RO3003) made of ceramic-filled PTFE composites, which provide an excellent and stable dielectric constant, coefficient of thermal expansion and mechanical stability over a wide temperature range of -55 to $+250$ C°. These specifications make this laminate very suitable for high power applications. The package technology is demonstrated using a 30 Watt package design for LDMOS devices (Fig. 5.1).

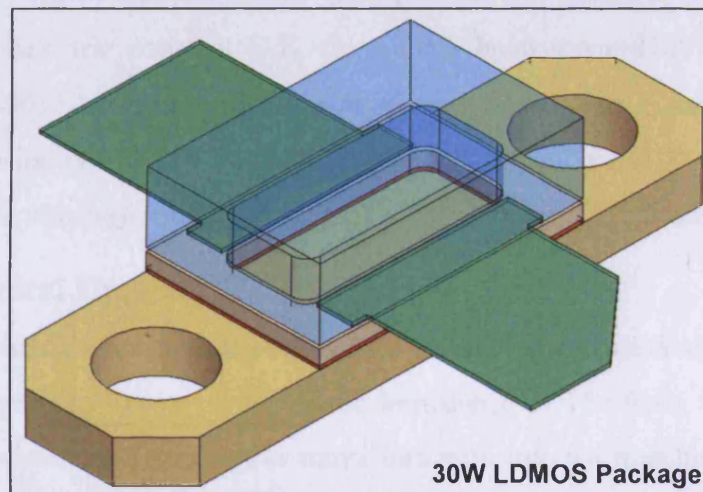


Fig. 5.1 HFSS representation for 30 Watt LDMOS package structure

The new package consists of a 1 mm thick gold plated copper heat sink with a laminate frame that has been cut using laser technology to form a laminate ring that isolates the input and output leads from the electrically conductive heat sink; the laminate structure is bonded to the heat sink using electrically conductive film.

For environmental protection, the package is capped with a lid made of the same laminate material (or any other suitable material) which in turn is bonded to the laminate ring and the input and output leads. The thickness of the gold plated copper leads is $100\ \mu\text{m}$, whilst the laminate thickness can be chosen to mate with the particular thickness of the die in order to reduce the required bond wire length (but not too thin to create voltage breakdown issues).

5.2 Package Design

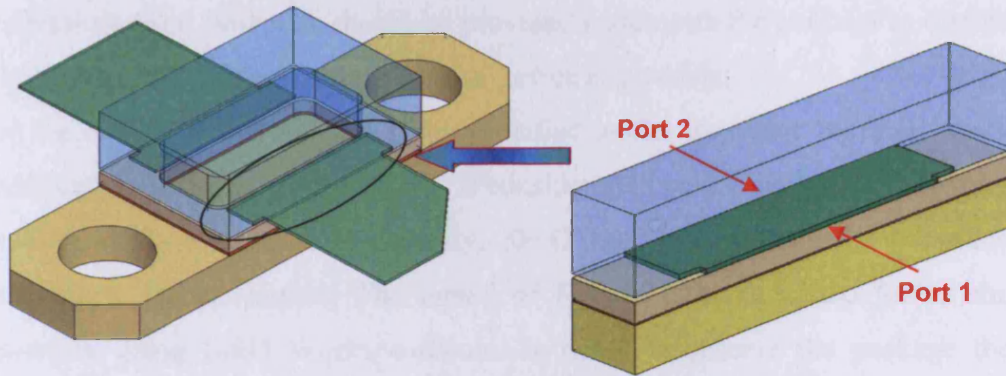
The package design process starts by specifying the power rating and the physical size of the device which the package is going to enclose. Having determined this, a suitable laminate can then be selected, based on different parameters such as the stability of the dielectric constant with temperature, maximum XYZ coefficients of thermal expansion and the temperature range the board can sustain under maximum loading conditions. A ceramic substrate would be the ideal candidate so a material is chosen with similar properties to ceramic to ensure good performance. The primary limiting factor that makes laminate substrates less attractive is less favourable thermal performance. Therefore, if a package is designed to dissipate heat efficiently without compromising the laminate substrate performance, then the laminate based high power package can become practical. The laminate used for this package is RO3003 ($635\ \mu\text{m}$ thick) which exhibits a very good thermal and electrical performance. The board has a dielectric constant $D.K.=3$, voltage breakdown= $850\text{V}/\text{mil}$, dissipation factor $\tan\delta=0.0013$ which represents a very low dielectric loss, and coefficients of thermal expansion (CTE) of $17\ \text{ppm}/^\circ\text{C}$ in the X,Y direction and $27\ \text{ppm}/^\circ\text{C}$ in the Z direction which although roughly twice that of the ceramic CTE, is still very low.

5.2.1 Electrical Design

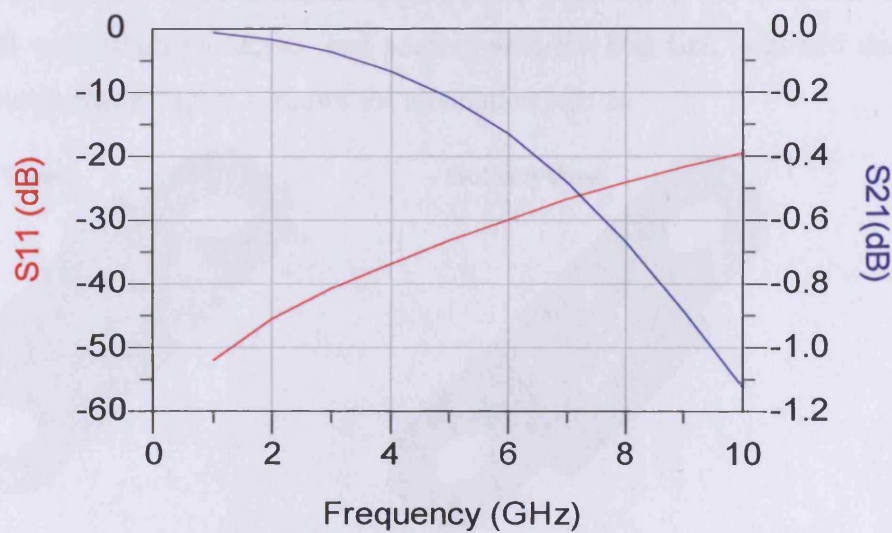
The package was designed to accommodate a 30 Watt LDMOS die. The package leads are designed to have a characteristic impedance of 15 Ohms, which is a good compromise when using high power transistors with internal matching networks. To compensate for the wire bonding effect the package leads were extended laterally to improve the package overall performance. Practically the package leads normally sit on a PCB board therefore the characteristic impedance of this part of the package is determined by the PCB board properties. However for measurement purpose, the measurement system is normally calibrated up to the package reference plane, hence the package leads will be within the measurement system calibration plane. This

leaves only a small part of the package shown in Fig. 5.2.a, which has to be designed and verified. Therefore a full EM simulation was performed on that small part of the package which represents the package I/O ports.

Ansoft's HFSS simulator was used to investigate the package's RF s-parameter behaviour and the package single-port response is shown in Fig. 5.2.b below.



(a)



(b)

Fig. 5.2 HFSS simulation of one package port using RO3003 ($635 \mu\text{m}$ thick) laminate
 At 2.1 GHz the package EM simulation shows -45 dB return loss and -0.1 dB insertion loss normalised to 15 Ohm I/O port characteristic impedance. The simulation results of Fig. 5.2 above indicate that this package is broadband in nature, however, it should be mentioned that the performance of the device mounted within the package will be more narrowband due to the performance of the device itself in combination with the physical mounting, including the bond wires. This observed response suggests that the electrical design of the package is effective and very well suited for many existing and future communication systems subject to package measurements and verification.

5.2.2 Thermal Analysis

To analyse the thermal behaviour of the package consider the package shown in Fig. 5.1, where the high power transistor die will be attached to the copper heat sink directly. Due to the fact that the die temperature is concentrated on the die top surface, some of the heat will flow inside the package including the laminate and the lid. Therefore a good heat sink should be provided underneath the package to dissipate as much of the heat generated by the active device as possible.

For the LDMOS devices, 125 C° is specified as the transistor ‘normal’ maximum operating temperature, whilst 200 C° is considered to be the limit where the transistor junction will breakdown. Consequently, 200 C° has been chosen as the worse case die temperature for simulation. The model of Fig. 5.1 was simulated for its thermal behaviour using Solid Works software. In order to observe the package thermal capabilities, two thermal simulations have been performed, one when no heat sink provided underneath the device and another with the heat sink is placed underneath the whole package, Fig. 5.3 shows the simulation results.

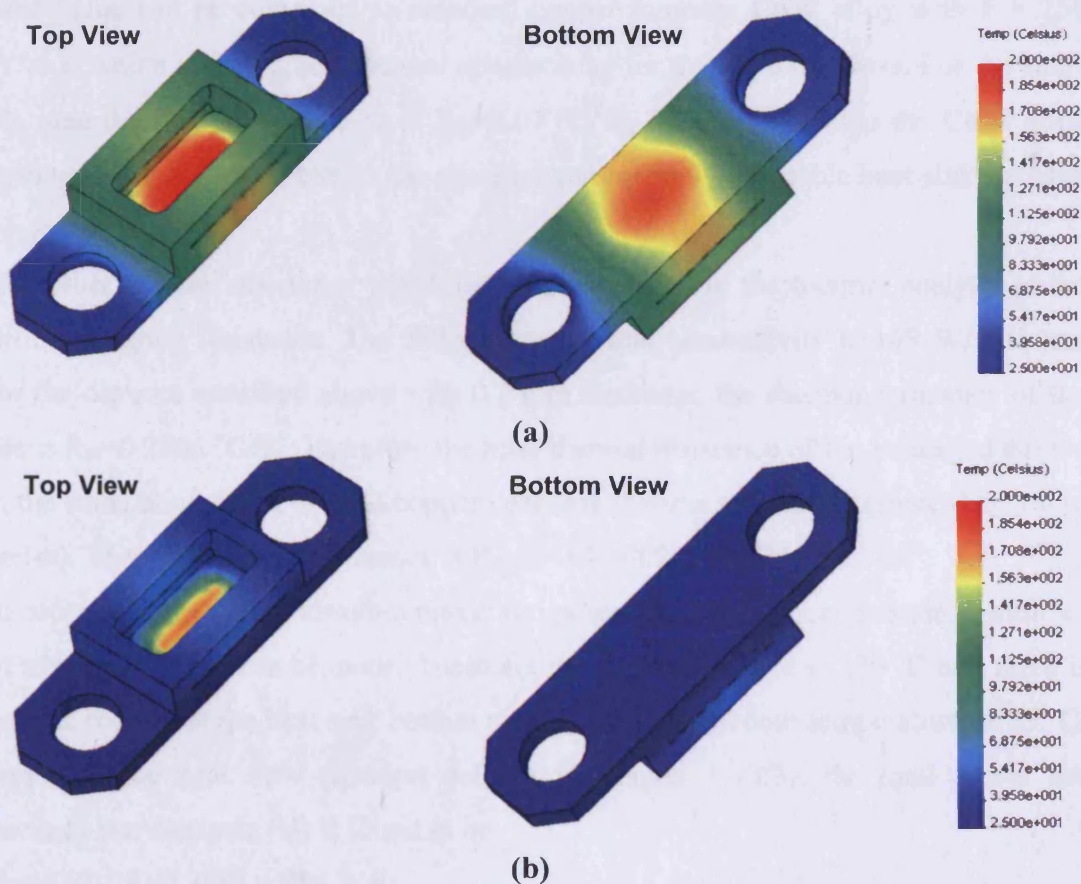


Fig. 5.3 High power package thermal simulation results **a)** no heat sink underneath the device, **b)** heat sink available under the whole package

It is clear from the figure above that for the case where there is no heat sink the temperature underneath the die and in the dielectric is easily high enough to cause copper and dielectric expansion. This is likely to create mechanical instability in the package structure. This can be avoided by providing a good heat sink underneath the die area. It can be seen in Fig. 5.3.b that the temperature drops significantly when the heat sink is included in the design; the temperature distribution across the package has also dropped significantly. Note that an ideal die to heat sink bonding is assumed, however non-ideal bonding will lead to temperature increase.

It is clear from the above simulation that the method of cooling can determine the heat flow rate across the heat sink. In order to predict the maximum power rating of the device which can be placed into the above package, then the following thermal calculation can be performed.

Using equation (3.4) [1], for the above package the copper heat sink has (1 mm) thickness, A is the die area (1.15x4.55 mm) and k is the copper thermal conductivity (390 W/m·K), which gives thermal resistance $R_{th} = 0.49 \text{ }^\circ\text{C/W}$.

This value can be compared to standard copper tungsten CuW alloy with $k = 250 \text{ W/m}\cdot\text{K}$ which is the highest thermal conductivity for this kind of alloys. For the same die area the thermal resistance is $R_{th} = 1.07 \text{ }^\circ\text{C/W}$, for this R_{th} value the CuW alloy thickness was 1.4 mm which is the standard commercially available heat sink for high power devices.

The other thermal resistance which has to be included in the thermal analysis is the Silicon thermal resistance. The Silicon has thermal conductivity $k = 149 \text{ W/m}\cdot\text{K}$ and for the die area specified above with 0.2 mm thickness, the thermal resistance of the die is $R_{th} = 0.2565 \text{ }^\circ\text{C/W}$. Therefore the total thermal resistance of the packaged device is the summation of the die and copper heat sink thermal resistances (since they are in series). The total thermal resistance is $R_{th-tot} = 0.49 + 0.2565 = 0.7465 \text{ }^\circ\text{C/W}$.

In order to calculate the absolute maximum power the package can sustain, a number of assumptions have to be made. These are the die temperature is $200 \text{ }^\circ\text{C}$ and there is perfect cooling at the heat sink bottom side to keep it at a room temperature of $25 \text{ }^\circ\text{C}$. Applying the heat flow equation defined in chapter 3 (3.3), the total power the package can dissipate (H) is found to be

$$H = (200 - 25) / 0.7465 = 234 \text{ Watt}$$

If the device is going to operate at its break down temperature, the device will not survive for any sustained period, so manufactures normally set an optimum die operating temperature. For LDMOS devices the operating temperature is normally specified to be 125 °C and the maximum ambient temperature for civil applications is 85°C. Applying these figures on the heat flow equation (3.3) reveal $H=(125-85)/0.7465=53.5$ Watt however this figure can decrease when non ideal die-to-heat sink and heat sink-to-mounting fixture attachments is involved.

Applying the last temperature boundary to the commercially available CuW alloy reveal $H=(125-85)/(1.07+0.2565)= 30.15$ Watt.

The above calculations show clearly that the newly developed package has nearly doubled the device power rating of the normal commercial choice of CuW alloy, allowing larger devices to be mounted within the package. which could be mounted inside the package. This is mainly due to the fact that the package heat sink is made of minimum thickness pure copper.

5.3 Package Realization and Measurement

The package shown in Fig. 5.1 has been manufactured by Labtech Ltd UK using RO3003 laminate with a lid made of FR4 material, the manufactured package is shown in Fig. 5.4 below,

In order to measure the performance of this package against an industrial standard package, two comparable 30 Watt LDMOS transistors made by Philips (PHILIPS ILSG4-4) were obtained. One of these devices was packaged by Philips (using a typical Alumina ceramic package) and the other identical device was acquired as an unpackaged die and was then mounted onto the Labtech laminate based high power package using silver epoxy.

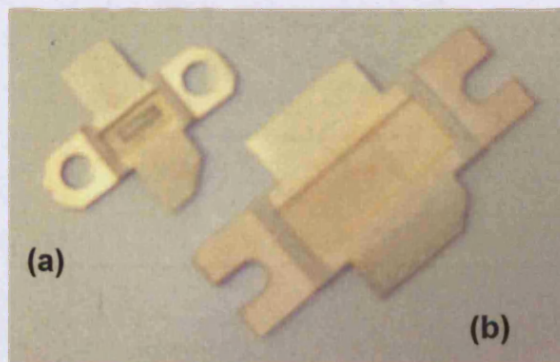


Fig. 5.4 High power laminate based packages, (a) 30Watt package with 30W device attached and (b) 100Watt package

This 30 Watt package had to be measured and therefore the measurement system described in the previous chapter was used. However the measurement system had to be equipped with two impedance transformers (tapers) and the whole system needed to be verified under different operating and calibration conditions. Therefore, the system was fully reconfigured and tested via the measurement of a known 100Watt LDMOS device as discussed in the previous chapter. The same system was also used to measure the above 30 Watt devices, but using different tapered transformers.

Having verified the load-pull measurement system, a new 50:9.5 Klopfenstein impedance transformer (70 mm in length) was realised using TMM4 board (D.K.=4.5, $\tan\delta=0.002$ and voltage breakdown=750 V/mil) with 68 μm copper cladding and 762 μm dielectric thickness. A ceramic based packaged 30W LDMOS transistor (PHILIPS ILSG4-4) was load-pulled at 1.8 GHz under class AB operation. The desire to compare measured performance to that given in the manufactures datasheet was unfortunately not possible since these transistors were found to be very fragile and kept breaking down when setting the V_{DS} bias voltage to values similar to the manufacturer datasheet setting which was 28 Volt. Therefore the device was biased at $V_{GS}=3.5\text{V}$ and $V_{DS}=25\text{V}$ instead during this study.

Following a comprehensive load-pull measurement and generation of contours of constant power, the optimum load was found to be $Z_{\text{opt}}=(1.74 - j3.25)\ \Omega$ at the DUT reference plane (Fig. 5.5) which shows good agreement with the optimum device impedance provided by the device data sheet $(1.31-j3.28)\ \Omega$.

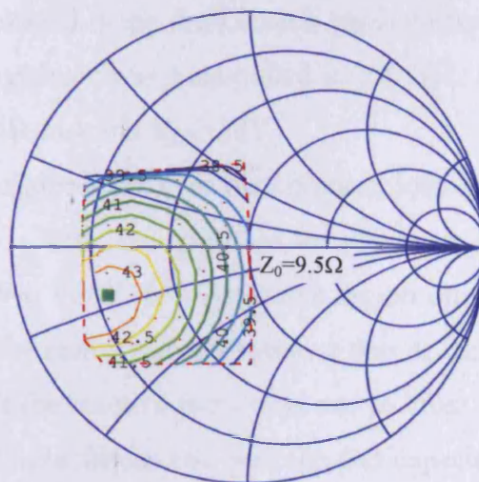


Fig. 5.5 Load-pull power contours in dBm for a 30W device (using ceramic package) with optimum impedance of $1.74-j3.25\ \Omega$

Whilst maintaining a constant optimum load, the input power was swept with resulting measurements shown in Fig. 5.6. The maximum output power is 23 Watt for which a load-pull power (P_{LP}) of only 32 Watt was required.

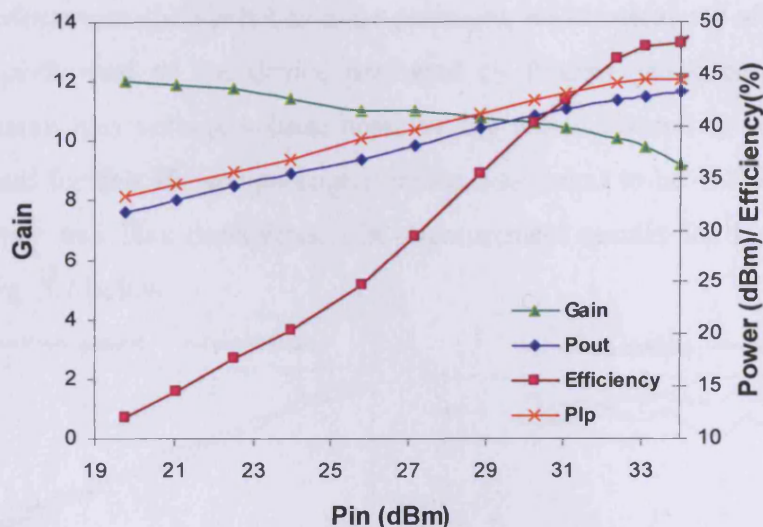


Fig. 5.6 Pin vs Pout, P_{LP} , Efficiency, and Gain for 30W LDMOS transistor

In order to make a valid comparison between Labtech and Philips packaged devices, both had to be measured using the same measurement setup. To measure the RF performance of these two packaged devices, the new load-pull measurement system described in detail in chapter 4 of this thesis was used [2].

As previously noted these Philips devices were found to be very fragile and kept breaking while increasing the V_{DS} voltage therefore they had to be biased at lower voltage levels that given in the datasheet. To start with, the 30 Watt Philips LDMOS device which was packaged using the Labtech laminate based package was mounted and measured. The transistor was load-pulled at 2.1 GHz under class AB operation with $V_{GS}=3.2V$, $I_{DS}=400mA$ and $V_{DS}=20V$.

Following a comprehensive search for the optimum load impedance, it was found to be $Z_{opt}=1.6-j4.7$ Ohm. Note, the specified manufacturer optimum load ($1.31-j3.28$ Ohm), at a different $V_{DS}=28V$, is in the same region on the Smith Chart. This still confirms good RF performance with the resistive part of the two packages being close to each other, however the reactive parts were not so close, and this can be attributed to different wire bond inductances and package pad capacitance to ground as well as that the device was biased at $V_{DS}=20V$ instead of 28V specified in the data sheet due to the reasons mentioned above.

Whilst maintaining the same optimum load impedance, an input power sweep (P_{in}) was performed while measuring the transistor output power, efficiency and gain. Since the device was biased at $V_{DS}=20V$ therefore in order to quantify the new package performance (Labtech Laminate package), an identical set of measurements were then performed on the device packaged by Philips (using ceramic package) under the same bias voltage values, however I_{DS} was measured to be 265mA. The optimum load for this Philips packaged device was found to be $1.479-j4.19$ Ohm at that frequency and bias conditions. The measurement results for both devices are shown in Fig. 5.7 below.

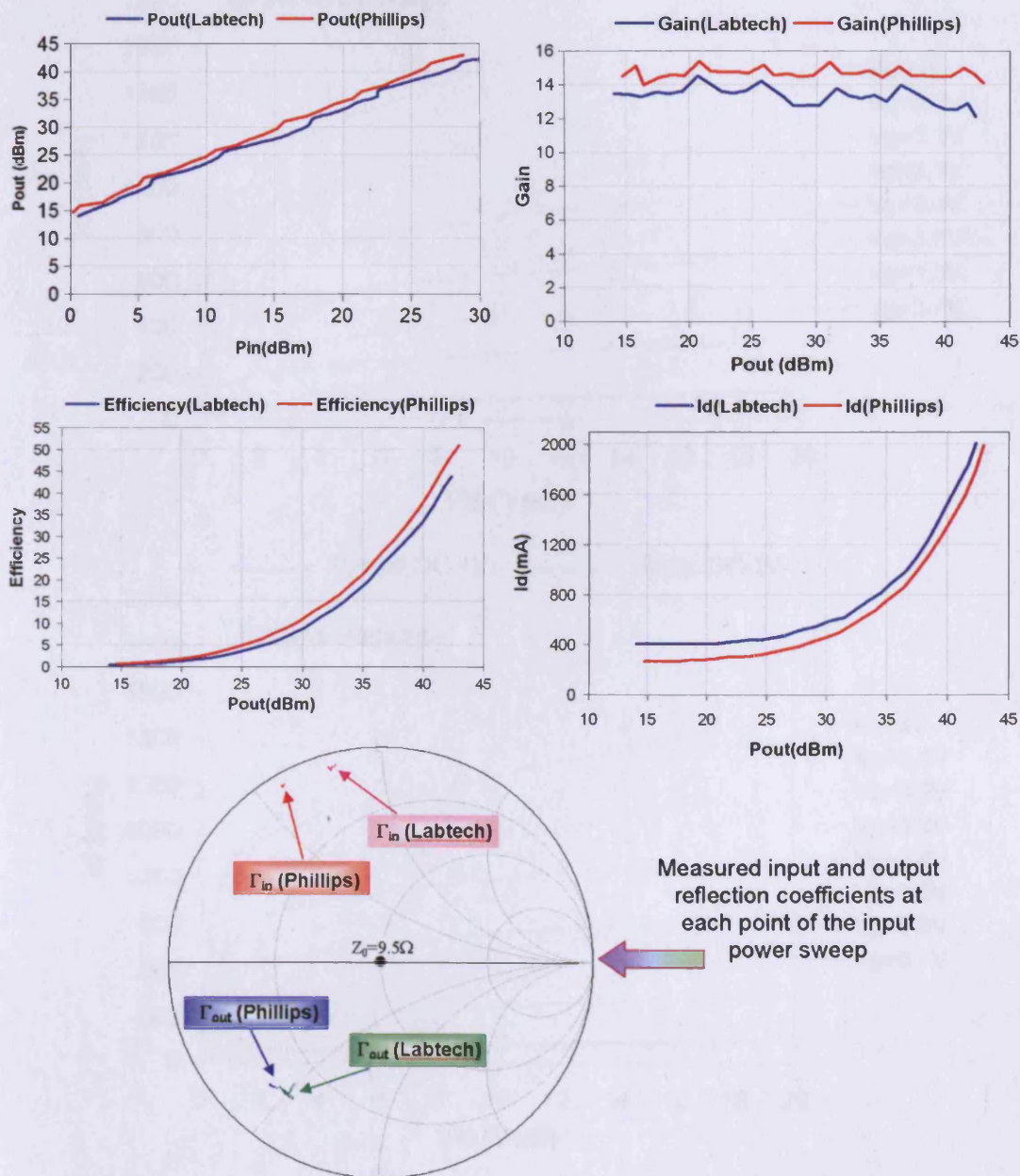


Fig. 5.7 Labtech packaged device measurement results compared to Philips packaged device response

The results of Fig. 5.7 above show that Philips and Labtech packages have similar RF performance. All measured parameters, such as output power (P_{out}), efficiency, and gain are very close. The small differences can be attributed to the differences in the drain currents which can be seen within the P_{out} versus I_d graph.

In order to confirm the origin of these differences, pulsed and static DC-IV measurements have been carried out for each device. The measurement results are shown in Fig. 5.8 below,

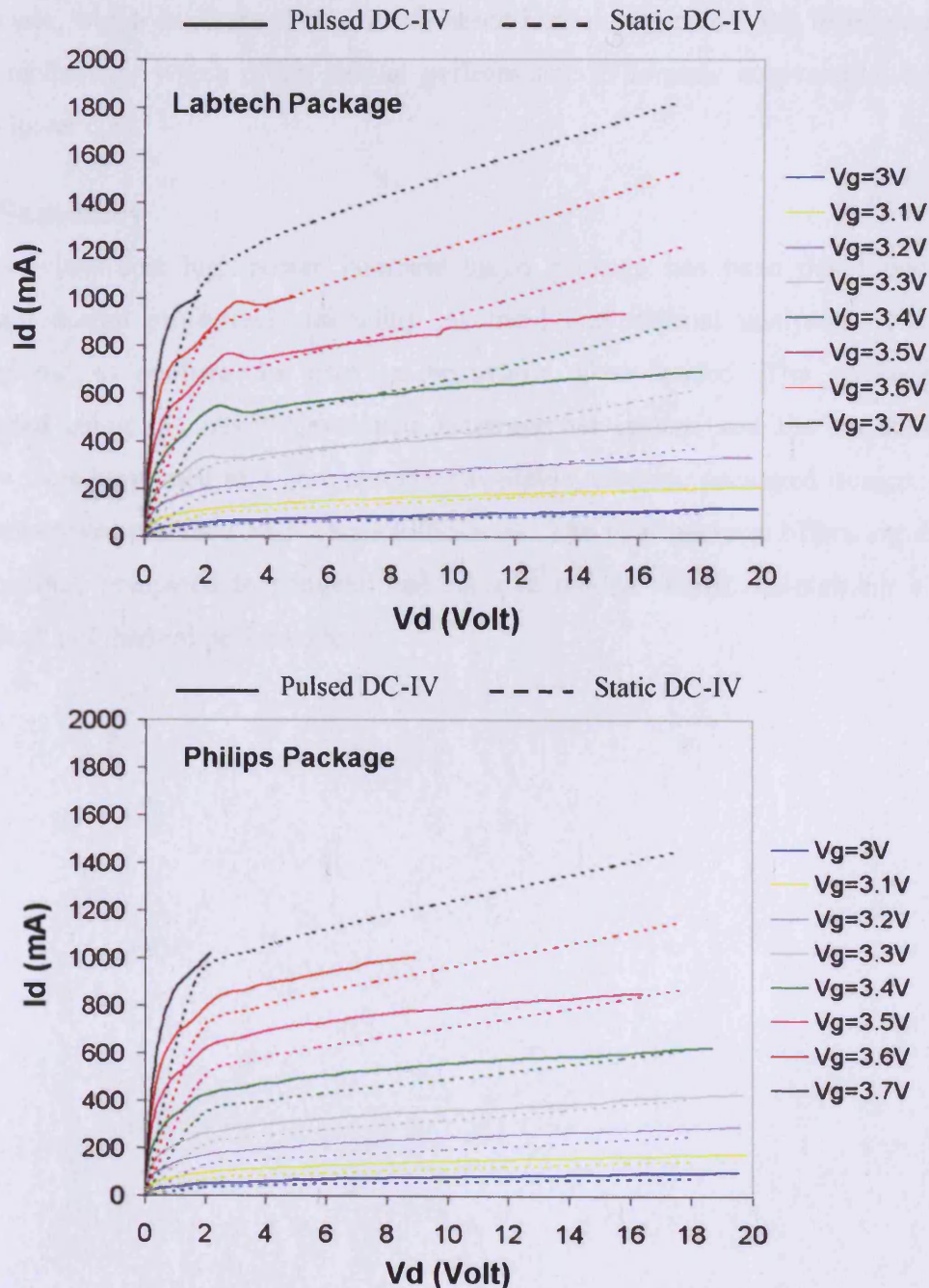


Fig. 5.8 Labtech and Philips packaged ILSG4-4 transistor pulsed and static DC-IV characteristics comparison

From the normal (static) DC-IV characteristics of Fig. 5.8, it is clear that the two devices are different regardless of the package make or shape. One of the reasons this difference can be attributed to is the fact that these two devices has come from two different wafers or batches and the time gap between obtaining the original Philips packaged device and the die on its own was around six months which indicate that new revision had been applied onto the die.

From RF point of view Labtech packaged device was able to deliver almost the same RF power, which confirms that laminate based high-power packaging technology is a valid technology which offers similar performance to ceramic equivalents, but at a much lower cost.

5.4 Summary

A novel low cost high-power laminate based package has been developed. The package design procedures, including electrical and thermal analysis, have been carried out to confirm the package behaviour when loaded. The package was measured using the newly developed measurement system and the measurement results were compared to a commercially available, ceramic packaged device. Good agreement was obtained with small differences. The new package offers significant cost savings compared to conventional ceramic models whilst maintaining a good electrical and thermal performance.

5.5 References:

- [1] Y. Freedman, *University Physics*: Addison Wesley, ISBN 0-321-20469-7.
- [2] Z. Aboush, J. Lees, J. Benedikt, and P. Tasker, "Active Harmonic Load-pull for Characterizing Highly Mismatched High Power Transistors," *IEEE MTT-S International Microwave Symposium Digest*, pp. 1311-1314, June 2005.

CHAPTER 6

CONCLUSION AND FUTURE WORK

6.1 Conclusion

The evolution of modern semiconductor technologies is generally driven by the continuous demand for reduced physical size, and increasing chip functionality. As a result, major challenges are being faced by semiconductor packaging technologies; these include increased bandwidth due to diverse integrated applications, and increased required power density per unit area. The most direct and significant impact of these emerging problems is increased package cost. This project targets the above technical problems and has resulted in optimised solutions, whilst reducing the overall package cost.

In terms of low-power devices (up to few Watts), this was achieved by replacing traditional yet expensive ceramic substrates with cutting-edge, low cost, Liquid Crystal Polymer (LCP) substrate. This new material offers competitive performance to ceramic at a much lower cost, with the only disadvantage of having a high-coefficient of thermal expansion in the z-direction. This material is therefore used for low power applications.

The design of the new, low power SMT package presented in this work was based on micro-via technology, which offers many advantages over the normal through-via. The first of these is the flexible control of the via's transition impedance (where the via connects the package top and bottom metallization layers). Impedance control was achieved using the methodology of systematically varying the via section's electrical parameters (inductance and capacitance), which can be achieved by varying the via's geometry. The outcome was a broadband DC-50 GHz transition with less than 0.3 dB insertion loss, and better than 15 dB return loss over the entire bandwidth. Any resonances due to the via transition section was suppressed, (or shifted up in frequency) by using thin LCP substrate, while offsetting the via's top and bottom pads from each other in order to reduce the coupling capacitance between parallel via pads. Furthermore, the launch from PCB board to package was analyzed, and designed in a systematic way to maintain 50 Ohm impedance. The resultant package maintained 50 Ohm impedance from the PCB-to-package launching point up to the DUT plane.

To measure the newly developed low power packages, a robust on-wafer probe based new measurement system was implemented which utilise a multi-tier calibration techniques, allowing measurement at various reference planes, all the way up to the DUT plane. This allowed the extraction of a full s-parameters based model of the package, which could be stored as a text file, and easily embedded into a CAD simulator to be used by the system designer, allowing the package effects to be taken into account.

Having demonstrated the advantages of using laminate-based substrates in low-power packaging application, the implementation of this technology was then extended to high-power packages. Laminate based substrates suitable for high-power applications were utilised to design high-power packages. The new high-power package was verified by mounting a 30 Watt LDMOS device die into the package, comparing non-linear measurement results to a similar commercial off-the-shelf device. Measurements of the new package show some discrepancy, the DC-IV curves comparison reveals that the devices used for comparison are in fact different and came from two different batches.

The measurement of the new high-power packaged device suggests that the laminate based, high-power packaging technology is a valid and promising technology which could be used to replace the ceramic based high-power packages, whilst maintaining good performance at a much lower cost.

Active load-pull measurement techniques were implemented to measure the high-power packages presented in this work. To enable the measurement of such high-power devices, a new active load-pull measurement system was developed to cope with these high power levels. The new measurement system was implemented based on the existing open-loop load-pull measurement system developed at Cardiff University prior to the start of this project. The new system was equipped with two, broadband impedance transformers and reconfigured through the use of multi-tier calibration techniques to enable the measurement of active devices of more than 100 Watt CW power. The impact of using impedance transformers in these systems, and their effects on reducing the voltage standing wave and the load-pull power requirements has been studied in great detail. Consequently, systematic design procedures were established in order to select the optimum transformation ratio. The major advantage of implementing the broadband impedance transformer approach was the ability to calibrate the system over wide frequency bandwidth (1-12 GHz),

and therefore enabled harmonic load-pull measurements which consequently enabled the waveforms to be extracted and observed at different calibrated reference planes, but most importantly at the DUT reference plane.

The weaknesses associated with this kind of measurement systems, specifically the non-perfect 50 Ohm measurement environment, has been examined and analyzed in detail. One outcome of this was the introduction of a hybrid load-pull measurement approach that exploits this non-ideality in order to maximize the system performance, by lowering the load-pull power requirements whilst at the same time, maintaining calibration and measurement accuracy. The analysis, design and implementation of this hybrid, load-pull measurement systems has been verified successfully through the measurements on a commercially available 100 Watt LDMOS device, where only 35 Watt of load-pull power was necessary in order to load-pull the device and to locate its optimum impedance.

6.2 Future Work

The work presented in this thesis has established a basis for developing low-cost, high-performance Surface Mount Technology (SMT) packages. Further work is required to investigate the effect of wire-bonds on package performance, and wire-bond compensation techniques. This usually involves adding capacitive elements in order to resonate-out parasitic inductive effects. The wire-bond compensating circuitry can be embedded into the laminate itself. In terms of wire-bond characterization, the developed measurement system used to characterize the low power packages in conjunction with the multi-tier calibration techniques can be utilised to do this job efficiently.

For the low-power packages presented in this thesis, conductor backed coplanar transmission lines were used in order to launch the package. Practically, microstrip lines can also be used to route power within microwave circuits, therefore further work can be carried-out, looking at how to launch into the package using this approach. For this, a special impedance environment transformation circuit may become essential in order to maintain a clear transmission path. Also, a full s -parameter model for the mounted package will be useful, extracted using the same procedures as for the un-mounted package.

Furthermore, low power package verification can involve placing an active device inside the package and measuring the packaged device performance. For these types of measurements, the measurement system developed to characterize the high-power packages can be utilised to do that.

For the developed high power package, further optimisation of the die-attach techniques is necessary to maintain good thermal path. This could be achieved by using eutectic bonding instead of silver epoxy. Thermal measurement might also be useful to generate a thermal model for the package, and this can be achieved by placing thermal sensors on top of the package lid, inside the package, on die sensor and a sensor inside the heat sink just below the package. This technique can give a very robust thermal model for the package which can be used by the system designer to optimise the thermal dissipation rate from the package to the neighbour environment.

Matching circuits can also be embedded into the laminate to replace the external matching network, which will contribute in reducing the overall module cost. Similar electrical models generated for the low power packages can be extracted for the high power packages using the same techniques as those used for the low-power packages.

APPENDICES

Appendix A

TWO-PORT CALIBRATION USING THRU, REFLECT AND LINE (TRL)

A.1 TRL Calibration Algorithm

To perform this kind of calibration [1, 2], the known calibration standards have to be created using similar structure to the one used for the actual measurement. Firstly, the ‘Thru’ standard is created, which can be either a short length of transmission line with specific impedance (e.g. 50 Ohm) or of zero length; the centre of this standard represents the calibration reference plane. The ‘Reflect’ standard is a line with either an open or short termination with same characteristic impedance as the Thru standard. This standard should be placed at the desired calibration reference plane, which is normally set by the Thru standard. An offset-open or offset-short could also be used as the Reflect standard, provided the calibration procedure can account for the additional delay. Finally, the ‘Line’ standard is a line with different lengths which cover suitable frequency range depending on the phase of the lower and upper frequency band, again the impedance of this line should be the same as the Thru standard impedance. Furthermore, the line must be longer than the Thru standard. The derivation presented below assumes a zero length Thru and Reflect standards, and a non-zero length Line standard. The typical equivalent-error model for a two port measurement system is shown in Fig. A.1 below.

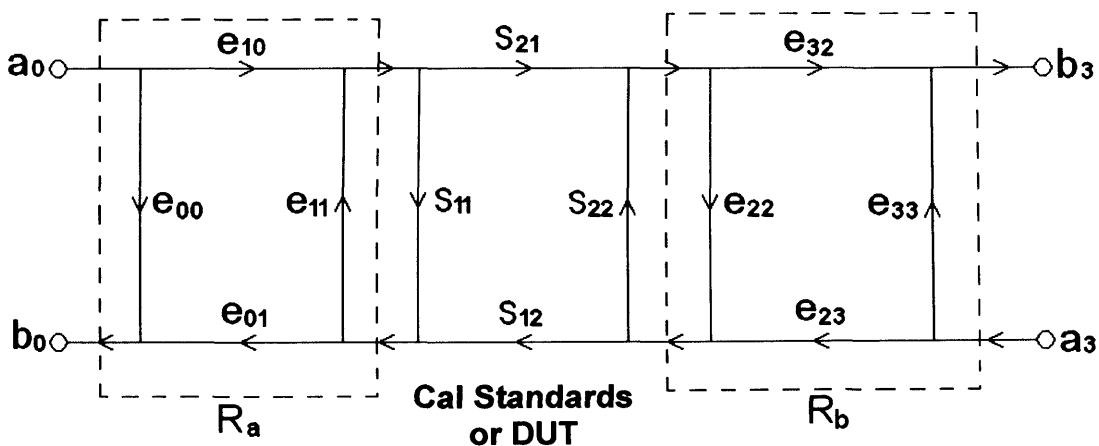


Fig. A.1 Equivalent error model for a two port measurement system

Using the S-to-T-Parameters conversion relations found in section A.2 of this document, let R_a and R_b be the transmission matrices of the two port error adaptors, then

$$R_a = \begin{bmatrix} ra_{11} & ra_{12} \\ ra_{21} & ra_{22} \end{bmatrix} = \frac{1}{e_{10}} \begin{bmatrix} -\Delta_a & e_{00} \\ -e_{11} & 1 \end{bmatrix} \quad (\text{A.1})$$

$$R_b = \begin{bmatrix} rb_{11} & rb_{12} \\ rb_{21} & rb_{22} \end{bmatrix} = \frac{1}{e_{32}} \begin{bmatrix} -\Delta_b & e_{22} \\ -e_{33} & 1 \end{bmatrix} \quad (\text{A.2})$$

where

$$\Delta_a = e_{00} e_{11} - e_{01} e_{10} \quad \text{and} \quad \Delta_b = e_{22} e_{33} - e_{23} e_{32}$$

The transmission matrices associated with the measured (R_M) and the DUT (R_D) s-parameters are given by

$$R_M = \frac{1}{S_{21M}} \begin{bmatrix} -\Delta_M & S_{11M} \\ -S_{22M} & 1 \end{bmatrix} \quad (\text{A.3})$$

$$R_D = \begin{bmatrix} r_{11D} & r_{12D} \\ r_{21D} & r_{22D} \end{bmatrix} = \frac{1}{S_{21D}} \begin{bmatrix} -\Delta_D & S_{11D} \\ -S_{22D} & 1 \end{bmatrix} \quad (\text{A.4})$$

where

$$\Delta_M = (S_{11M} S_{22M} - S_{12M} S_{21M})$$

$$\Delta_D = (S_{11D} S_{22D} - S_{12D} S_{21D})$$

Using matrix (A.4), the R_D matrices for an ideal Thru and a Line of length “L” and characteristics impedance Z_0 are

$$R_{DT} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \quad (\text{A.5.a})$$

and

$$R_{DL} = \begin{bmatrix} e^{-\gamma L} & 0 \\ 0 & e^{+\gamma L} \end{bmatrix} \quad (\text{A.5.b})$$

The measured s-parameters are related to the adaptors, and DUT s-parameters as shown

$$R_M = R_a R_D R_b \quad (\text{A.6})$$

The measured s-parameters when the Thru standard is connected are

$$R_{MT} = R_a R_{DT} R_b = R_a R_b \quad (\text{A.7})$$

The measured s-parameters when the Line standard is connected are

$$R_{ML} = R_a R_{DL} R_b \quad (\text{A.8})$$

Solving equation (A.7) for the R_b matrix yields

$$R_b = R_a^{-1} R_{MT} \quad (\text{A.9})$$

Substituting equation (A.9) into (A.8) yields

$$R_{ML} = R_a R_{DL} R_a^{-1} R_{MT}$$

Rearranging the above equation yields

$$R_{ML} R_{MT}^{-1} R_a = R_a R_{DL}$$

$$\therefore M R_a = R_a R_{DL} \quad (\text{A.10})$$

Where

$$M = R_{ML} R_{MT}^{-1} = \begin{bmatrix} m_{11} & m_{12} \\ m_{21} & m_{22} \end{bmatrix}$$

Substituting equations (A.1) and (A.6) into (A.10) yields

$$\begin{bmatrix} m_{11} & m_{12} \\ m_{21} & m_{22} \end{bmatrix} \begin{bmatrix} ra_{11} & ra_{12} \\ ra_{21} & ra_{22} \end{bmatrix} = \begin{bmatrix} ra_{11} & ra_{12} \\ ra_{21} & ra_{22} \end{bmatrix} \begin{bmatrix} e^{-\gamma L} & 0 \\ 0 & e^{+\gamma L} \end{bmatrix} \quad (\text{A.11})$$

By expanding the matrices in (A.11) in both sides, the following set of equations can be obtained:

$$m_{11} ra_{11} + m_{12} ra_{21} = ra_{11} e^{-\gamma L} \quad (\text{A.12.a})$$

$$m_{21} ra_{11} + m_{22} ra_{21} = ra_{21} e^{-\gamma L} \quad (\text{A.12.b})$$

$$m_{11} ra_{12} + m_{12} ra_{22} = ra_{12} e^{+\gamma L} \quad (\text{A.12.c})$$

$$m_{21} ra_{12} + m_{22} ra_{22} = ra_{22} e^{+\gamma L} \quad (\text{A.12.d})$$

Dividing equation (A.12.a) by (A.12.b), and (A.12.c) by (A.12.d), and rearrange the equations will result in two quadratic equations with the same constant terms.

$$m_{21} \left(\frac{ra_{11}}{ra_{21}} \right)^2 + (m_{22} - m_{11}) \left(\frac{ra_{11}}{ra_{21}} \right) - m_{12} = 0 \quad (\text{A.13.a})$$

$$m_{21} \left(\frac{ra_{12}}{ra_{22}} \right)^2 + (m_{22} - m_{11}) \left(\frac{ra_{12}}{ra_{22}} \right) - m_{12} = 0 \quad (\text{A.13.b})$$

Let $a = \frac{ra_{11}}{ra_{21}}$ and $b = \frac{ra_{12}}{ra_{22}}$ Consequently

$$a = \frac{ra_{11}}{ra_{21}} = e_{00} - \frac{e_{01} e_{10}}{e_{11}} \quad (\text{A.14.a})$$

$$b = \frac{ra_{12}}{ra_{22}} = e_{00} \quad \text{where } |a| > |b| \quad (\text{A.14.b})$$

Hence

$$e_{00} = b \quad (\text{A.15.a})$$

$$\frac{e_{01} e_{10}}{e_{11}} = b - a \quad (\text{A.15.b})$$

Similarly equation (A.7) can be solved for the R_a matrix, which yields

$$R_a = R_{MT} R_b^{-1} \quad (\text{A.16})$$

Substituting equation A.16 into A.8 yields

$$R_{ML} = R_{MT} R_b^{-1} R_{DL} R_b$$

Rearranging the above equation yields

$$R_b R_{MT}^{-1} R_{ML} = R_{DL} R_b$$

$$\therefore R_b N = R_{DL} R_b \quad (\text{A.17})$$

Where

$$N = R_{MT}^{-1} R_{ML} = \begin{pmatrix} n_{11} & n_{12} \\ n_{21} & n_{22} \end{pmatrix}$$

Substituting equations (A.2) and (A.6) into (A.17) yields

$$\begin{pmatrix} rb_{11} & rb_{12} \\ rb_{21} & rb_{22} \end{pmatrix} \begin{pmatrix} n_{11} & n_{12} \\ n_{21} & n_{22} \end{pmatrix} = \begin{pmatrix} e^{-\gamma L} & 0 \\ 0 & e^{+\gamma L} \end{pmatrix} \begin{pmatrix} rb_{11} & rb_{12} \\ rb_{21} & rb_{22} \end{pmatrix} \quad (\text{A.18})$$

By expanding both sides of the matrices in (A.18), the following set of equations can be obtained:

$$rb_{11} n_{11} + rb_{21} n_{12} = rb_{11} e^{-\gamma L} \quad (\text{A.19.a})$$

$$rb_{11} n_{12} + rb_{12} n_{22} = rb_{12} e^{-\gamma L} \quad (\text{A.19.b})$$

$$rb_{21} n_{11} + rb_{22} n_{21} = rb_{21} e^{+\gamma L} \quad (\text{A.19.c})$$

$$rb_{21} n_{12} + rb_{22} n_{22} = rb_{22} e^{+\gamma L} \quad (\text{A.19.d})$$

Dividing equation (A.19.a) by (A.19.b), and (A.19.c) by (A.19.d), and rearrange the equations result in two quadratic equations, with the same constant terms.

$$n_{12} \left(\frac{rb_{11}}{rb_{12}} \right)^2 + (n_{22} - n_{11}) \left(\frac{rb_{11}}{rb_{12}} \right) - n_{21} = 0 \quad (\text{A.20.a})$$

$$n_{12} \left(\frac{rb_{21}}{rb_{22}} \right)^2 + (n_{22} - n_{11}) \left(\frac{rb_{21}}{rb_{22}} \right) - n_{21} = 0 \quad (\text{A.20.b})$$

Let $c = \frac{rb_{11}}{rb_{12}}$ and $d = \frac{rb_{21}}{rb_{22}}$ Consequently

$$c = \frac{rb_{11}}{rb_{12}} = -e_{33} + \frac{e_{23} e_{32}}{e_{22}} \quad (\text{A.21.a})$$

$$d = \frac{rb_{21}}{rb_{22}} = -e_{33} \quad \text{where } |c| > |d| \quad (\text{A.21.b})$$

Hence

$$\frac{e_{23} e_{32}}{e_{22}} = c - d \quad (\text{A.22.a})$$

$$e_{33} = -d \quad (\text{A.22.b})$$

Reflection Standard

By applying a high reflection standard (open or short) at the calibration reference planes, the reflection on the “ R_a ” adaptor can be measured to be Γ_{Ma} with Γ_a being the actual standard reflectance. The one port equation can be written as

$$\Gamma_{Ma} = e_{00} + \frac{e_{01} e_{10} \Gamma_a}{1 - e_{11} \Gamma_a} \quad (\text{A.23})$$

Solving (A.23) for the actual reflection coefficient Γ_a yields

$$\Gamma_{Ma} - e_{00} = \Gamma_a e_{11} \left(\frac{e_{01} e_{10}}{e_{11}} - e_{00} + \Gamma_{Ma} \right) \quad (\text{A.24})$$

Using a & b expressions in equation (A.14) into equation (A.24) yields

$$\begin{aligned} \Gamma_{Ma} - b &= \Gamma_a e_{11} (-a + \Gamma_{Ma}) \\ \therefore \Gamma_a &= \frac{1}{e_{11}} \frac{b - \Gamma_{Ma}}{a - \Gamma_{Ma}} \end{aligned} \quad (\text{A.25})$$

Similarly the above procedures performed on adaptor “ R_b ” with Γ_{Mb} to be the measured input reflection and Γ_b being the actual reflection coefficient of the standard, it follows that

$$\Gamma_{Mb} = e_{33} + \frac{e_{23} e_{32} \Gamma_b}{1 - e_{22} \Gamma_b} \quad (\text{A.26})$$

Solving (A.26) for the actual reflection coefficient of the reflect standard Γ_b yields

$$\Gamma_{Mb} - e_{33} = \Gamma_b e_{22} \left(\frac{e_{23} e_{32}}{e_{22}} - e_{33} + \Gamma_{Mb} \right) \quad (\text{A.27})$$

Using c & d expressions in equation (A.21) into equation (A.27) yields

$$\begin{aligned} \Gamma_{Mb} + d &= \Gamma_b e_{22} (c + \Gamma_{Mb}) \\ \therefore \Gamma_b &= \frac{1}{e_{22}} \frac{d + \Gamma_{Mb}}{c + \Gamma_{Mb}} \end{aligned} \quad (\text{A.28})$$

By using the same type of reflection standard on both sides of the adaptors, then assuming $\Gamma_a \approx \Gamma_b$. Hence equating equations (A.25) and (A.28) yields

$$\frac{1}{e_{22}} = \frac{1}{e_{11}} \left(\frac{b - \Gamma_{Ma}}{a - \Gamma_{Ma}} \right) \left(\frac{c + \Gamma_{Mb}}{d + \Gamma_{Mb}} \right) \quad (\text{A.29})$$

A second equation is required to solve for e_{11} and e_{22} in equation (A.29). Therefore, we can make use of the measured input reflection coefficient S_{11MT} obtained when the thru standard is connected.

$$S_{11MT} = e_{00} + \frac{e_{01} e_{10} e_{22}}{1 - e_{11} e_{22}} \quad (\text{A.30})$$

Solving equation (A.30) for e_{11} yields

$$\therefore e_{11} = \frac{1}{e_{22}} \frac{b - S_{11MT}}{a - S_{11MT}} \quad (\text{A.31})$$

Substituting equation (A.29) into (A.31) and solving for e_{11} yields

$$\therefore e_{11}^2 = \left(\frac{b - \Gamma_{Ma}}{a - \Gamma_{Ma}} \right) \left(\frac{c + \Gamma_{Mb}}{d + \Gamma_{Mb}} \right) \left(\frac{b - S_{11MT}}{a - S_{11MT}} \right) \quad (\text{A.32})$$

The sign of e_{11} can be chosen based on the type of the used reflect calibration standard (open or short). Once e_{11} value is found equation (A.31) can be used to solve for e_{22}

$$e_{22} = \frac{1}{e_{11}} \frac{b - S_{11MT}}{a - S_{11MT}} \quad (\text{A.33})$$

Using equations (A.15.b, A.22.b, A.32, and A.33) will give the following products

$$e_{01} e_{10} = (b - a) e_{11} \quad (\text{A.34})$$

$$e_{23} e_{32} = (c - d) e_{22} \quad (\text{A.35})$$

Once these products are known, the propagation constant γ can be found using equation (A.12.a)

$$e^{-\gamma L} = m_{11} + m_{12} \frac{ra_{21}}{ra_{11}} = m_{11} + \frac{m_{12}}{a} \quad (\text{A.36})$$

It is important to find equations which relate the products $(e_{10} e_{32})$ and $(e_{01} e_{23})$. These products will be used in equation (A.6) and other relevant equations in order to find the final DUT parameters.

During the Thru measurement, the forward and reverse transmission coefficients can be written as

$$S_{21MT} = \frac{e_{10} e_{32}}{1 - e_{11} e_{22}} \quad (\text{A.37})$$

$$S_{12MT} = \frac{e_{01} e_{23}}{1 - e_{11} e_{22}} \quad (\text{A.38})$$

Solving equations (A.37) and (A.38) for the products $(e_{10} e_{32})$ and $(e_{01} e_{23})$ yields

$$e_{10} e_{32} = S_{21MT} (1 - e_{11} e_{22}) \quad (\text{A.39})$$

$$e_{01} e_{23} = S_{12MT} (1 - e_{11} e_{22}) \quad (\text{A.40})$$

These products are now ready to be used to find the final DUT s-parameters represented in equation (A.6) above. Therefore using equation (A.6) and replacing R_a and R_b with their equivalents in equations (A.1) and (A.2) to obtain:

$$R_M = \frac{1}{e_{10}} \begin{bmatrix} -\Delta_a & e_{00} \\ -e_{11} & 1 \end{bmatrix} R_D \frac{1}{e_{32}} \begin{bmatrix} -\Delta_b & e_{22} \\ -e_{33} & 1 \end{bmatrix}$$

Where

$$\Delta_a = e_{00} e_{11} - e_{01} e_{10} \quad \text{and} \quad \Delta_b = e_{22} e_{33} - e_{23} e_{32}$$

Replacing the error coefficients in the above equations with the equivalents in equations (A.14.a, A.14.b, A.21.a, A.21.b) yields

$$R_M = \frac{1}{e_{10} e_{32}} \begin{bmatrix} -\Delta_a & b \\ -e_{11} & 1 \end{bmatrix} R_D \begin{bmatrix} -\Delta_b & e_{22} \\ d & 1 \end{bmatrix} \quad (\text{A.41})$$

Where

$$\Delta_a = b e_{11} - (b - a) e_{11} = a e_{11} \quad \text{and} \quad \Delta_b = -d e_{22} - (c - d) e_{22} = -c e_{22}$$

R_M in equation (A.41) is the measured s-parameters for the system including the DUT. In order to extract the DUT s-parameters, the R_D matrix has to be solved. Note that the product $e_{01} e_{23}$ can be replaced by using equation (A.40) above; consequently,

$$R_D = e_{10} e_{32} \begin{bmatrix} -\Delta_a & b \\ -e_{11} & 1 \end{bmatrix}^{-1} R_M \begin{bmatrix} -\Delta_b & d \\ -e_{33} & 1 \end{bmatrix}^{-1} \quad (\text{A.42})$$

A.2 S to T Parameters Conversion [1]

When two port circuits are cascaded, it is often convenient to organize the signal parameters so that the input (port-1) signal parameters (a_1 and b_1) and output (port-2) parameters (a_2 and b_2) are grouped together. Consider the s-parameter error model shown in Fig. A.2 below.

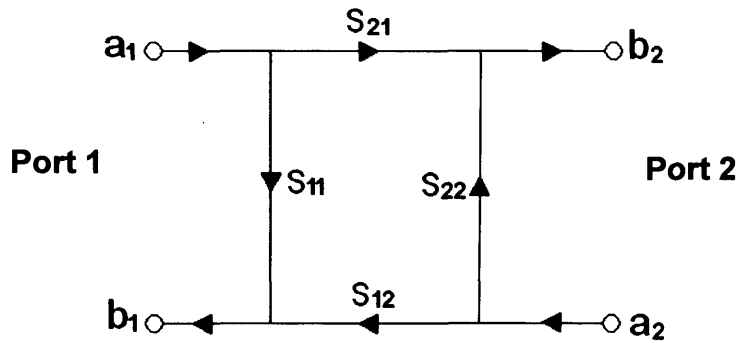


Fig. A.2 Two port network error flow graph

The reflected wave amplitudes b_1 and b_2 at ports 1 and 2 respectively are related to the incident waves a_1 and a_2 by the well known scattering equations:

$$b_1 = S_{11} a_1 + S_{12} a_2 \quad (\text{A.43})$$

$$b_2 = S_{21} a_1 + S_{22} a_2 \quad (\text{A.44})$$

Equations (A.43) and (A.44) can be represented in matrix form:

$$\begin{bmatrix} b_1 \\ b_2 \end{bmatrix} = \begin{bmatrix} S_{11} & S_{12} \\ S_{21} & S_{22} \end{bmatrix} \begin{bmatrix} a_1 \\ a_2 \end{bmatrix} \quad (\text{A.45})$$

Matrix equation (A.45) deals with the reflected wave forms as a function of the incident waveforms, which is not relevant in cascaded combinations. Hence this matrix needs to be converted to an equivalent T-parameter matrix, as shown in the matrix below:

$$\begin{bmatrix} b_1 \\ a_1 \end{bmatrix} = \begin{bmatrix} T_{11} & T_{12} \\ T_{21} & T_{22} \end{bmatrix} \begin{bmatrix} a_2 \\ b_2 \end{bmatrix} \quad (\text{A.46})$$

In order to convert matrix equation (A.45) to (A.46), equation (A.44) has to be substituted into equation (A.43) to eliminate a_1 , and then rearranging; this is shown in the following steps:

Rearrange equation (A.44):

$$a_1 = \frac{b_2 - S_{22} a_2}{S_{21}} \quad (\text{A.47})$$

Substitute equation (A.47) into (A.43):

$$b_1 = -\frac{\Delta}{S_{21}} a_2 + \frac{S_{11}}{S_{21}} b_2 \quad (\text{A.48})$$

Where $\Delta = (S_{11} S_{22} - S_{12} S_{21})$

Rearranging equation (A.47) for a_1 yields:

$$a_1 = -\frac{S_{22}}{S_{21}} a_2 + \frac{1}{S_{21}} b_2 \quad (\text{A.49})$$

Now Equation (A.48) and (A.49) can be combined to form Transmission matrix:

$$\begin{bmatrix} b_1 \\ a_1 \end{bmatrix} = \frac{1}{S_{21}} \begin{bmatrix} -\Delta & S_{11} \\ -S_{22} & 1 \end{bmatrix} \begin{bmatrix} a_2 \\ b_2 \end{bmatrix} \quad (\text{A.50})$$

Matrix equation (A.50) can now be related to matrix equation (A.45) and used in cascade with any other system.

A.3 T to S Parameters Conversion [1]

Matrix equation (A.50) can be expanded to the following two equations:

$$b_1 = T_{11} a_2 + T_{12} b_2 \quad (\text{A.51})$$

$$a_1 = T_{21} a_2 + T_{22} b_2 \quad (\text{A.52})$$

Rearranging equation (A.52) yields:

$$b_2 = \frac{1}{T_{22}} (a_1 - T_{21} a_2) \quad (\text{A.53})$$

Substituting equation (A.53) into (A.51) yields:

$$b_1 = T_{11} a_2 + \frac{T_{12}}{T_{22}} (a_1 - T_{21} a_2) \quad (\text{A.54})$$

Hence

$$b_1 = \frac{T_{12}}{T_{22}} a_1 + \left(\frac{T_{11} T_{22} - T_{12} T_{21}}{T_{22}} \right) a_2 \quad (\text{A.55})$$

Matrix equation (A.45) can be expanded to:

$$b_1 = S_{11} a_1 + S_{12} a_2 \quad (\text{A.56})$$

$$b_2 = S_{21} a_1 + S_{22} a_2 \quad (\text{A.57})$$

Comparing equation (A.56) to equation (A.55) and comparing equation (A.53) to equation (A.57) to obtain:

$$S_{11} = \frac{T_{12}}{T_{22}} \quad (\text{A.58})$$

$$S_{12} = T_{11} - \frac{T_{12} T_{21}}{T_{22}} \quad (\text{A.59})$$

$$S_{21} = \frac{1}{T_{22}} \quad (\text{A.60})$$

$$S_{22} = -\frac{T_{21}}{T_{22}} \quad (\text{A.61})$$

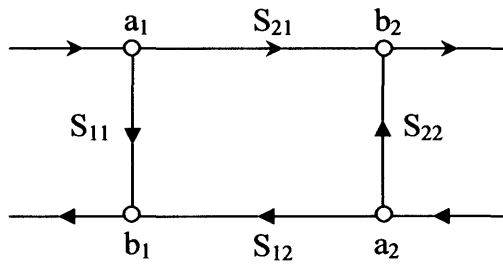
References:

- [1] G. F. Engen and C. A. Hoer, "“Thru-Reflect-Line:” An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer," *IEEE Transactions on Microwave Theory and Techniques*, vol. 27, pp. 987-993, December 1979.
- [2] D. Rytting, "Appendix to an analysis of vector measurement accuracy enhancement techniques," *Hewlett-Packard RF Microwave Symposium Digest*, pp. 1-42, March 1982.

Appendix B

LOSSLESS RECIPROCAL NETWORK ANALYSIS

The [S] matrix for a lossless reciprocal network are symmetrical [1]. To prove this, the s- parameters can be presented in a flow graph configuration as shown in Fig. B.1.



Where:

$$S_{11} = |S_{11}| e^{j\alpha}$$

$$S_{21} = |S_{21}| e^{j\gamma}$$

$$S_{12} = |S_{12}| e^{j\beta}$$

$$S_{22} = |S_{22}| e^{j\delta}$$

Fig. B.1 Flow graph for 2-port s-parameters

The following relations describe the properties of the lossless reciprocal network [1],

$$\sum_{k=1}^N S_{ki} S_{kj}^* = \delta_{ij} \quad \text{Where, } \delta_{ij} = \begin{cases} 1 & \text{if } i = j \\ 0 & \text{if } i \neq j \end{cases} \quad (\text{B.1})$$

Equation (B.1) implies the following four useful relations,

$$|S_{11}|^2 + |S_{21}|^2 = 1 \quad (\text{B.2})$$

$$|S_{12}|^2 + |S_{22}|^2 = 1 \quad (\text{B.3})$$

$$S_{11}S_{12}^* + S_{21}S_{22}^* = 0 \quad (\text{B.4})$$

$$S_{12}S_{11}^* + S_{22}S_{21}^* = 0 \quad (\text{B.5})$$

Proof 1: $|S_{11}| = |S_{22}|$ and $|S_{21}| = |S_{12}|$

Re-arranging equation (B.4) to obtain:

$$S_{21} = \frac{-S_{11}S_{12}^*}{S_{22}^*} \quad (\text{B.6})$$

Substituting equation (B.6) into (B.2) yields:

$$|S_{11}|^2 + \left| \frac{S_{11}S_{12}^*}{S_{22}^*} \right|^2 = 1 \quad (\text{B.7})$$

Multiplying equation (B.7) by $|S_{22}|^2$ yields:

$$|S_{11}|^2 |S_{22}|^2 + |S_{11}S_{12}|^2 = |S_{22}|^2 \quad (\text{B.8})$$

Note that the complex conjugate has disappeared due to the magnitude effect.

Rearranging equation (B.8) yields:

$$|S_{11}|^2 (|S_{22}|^2 + |S_{12}|^2) = |S_{22}|^2 \quad (\text{B.9})$$

Substituting equation (B.3) into (B.9) yields:

$$|S_{11}|^2 = |S_{22}|^2$$

Hence,

$$|S_{11}| = |S_{22}| \quad (\text{B.10})$$

Now to prove $|S_{21}| = |S_{12}|$ we need to equate equation (B.2) to (B.3),

$$|S_{11}|^2 + |S_{21}|^2 = |S_{12}|^2 + |S_{22}|^2 \quad (\text{B.11})$$

Substituting equation (B.10) into (B.11) yields

$$|S_{21}|^2 = |S_{12}|^2$$

Hence,

$$|S_{21}| = |S_{12}| \quad (\text{B.12})$$

Proof 2: Determine the phase relation between the four s-parameters,

Using the properties of equations (B.10) and (B.12); and re-arranging equation (B.2):

$$|S_{21}| = \sqrt{1 - |S_{11}|^2} = |S_{12}| \quad (\text{B.13})$$

Substitute equations (B.13) with (B.10) and (B.12) into equation (B.4) yields:

$$|S_{11}| e^{j\alpha} \sqrt{1 - |S_{11}|^2} e^{-j\beta} + \sqrt{1 - |S_{11}|^2} e^{j\gamma} |S_{11}| e^{-j\delta} = 0 \quad (\text{B.14})$$

Simplifying equation (B.14),

$$e^{j(\alpha-\beta)} + e^{j(\gamma-\delta)} = 0$$

$$\frac{e^{j(\alpha-\beta)}}{e^{j(\gamma-\delta)}} + 1 = 0$$

$$e^{j(\alpha-\beta-\gamma+\delta)} = -1 = e^{\pm jn\pi}, \quad \text{where } n=\text{odd number}$$

$$e^{j(\alpha-\beta-\gamma+\delta \mp n\pi)} = 1 = e^{j0} \quad (\text{B.15})$$

Equating the phase of the two sides of equation (B.15) yields:

$$\alpha - \beta - \gamma + \delta \mp n\pi = 0 \quad (\text{B.16})$$

For a passive reciprocal network ($\gamma = \beta$), substituting that into equation (B.16) and solving for δ yields,

$$\delta = 2\gamma - \alpha \pm n\pi \quad (\text{B.17})$$

Therefore the four s-parameters for a lossless reciprocal network could be written as following:

$$[S] = \begin{bmatrix} |S_{11}|e^{j\alpha} & \sqrt{1-|S_{11}|^2}e^{j\gamma} \\ \sqrt{1-|S_{11}|^2}e^{j\gamma} & -|S_{11}|e^{j(2\gamma-\alpha\pm n\pi)} \end{bmatrix} \quad (\text{B.18})$$

References:

- [1] D. M. Pozar, *Microwave Engineering*: John Wiley, ISBN 0-471-17096-8.

Appendix C

STANDING WAVE ANALYSIS IN LOAD-PULL MEASUREMENT SYSTEMS

In any load-pull system (passive or active), once a non-50 Ohm impedance is provided to an active device, this will immediately create voltage and current standing waves in the measurement system. In this appendix, for a given system characteristic impedance, the voltage standing wave produced and its relation to the device maximum available power and the synthesised load-pull reflection coefficient will be derived in full.

The analysis can be initiated by considering the signal flow graph shown in Fig. C.1 below,

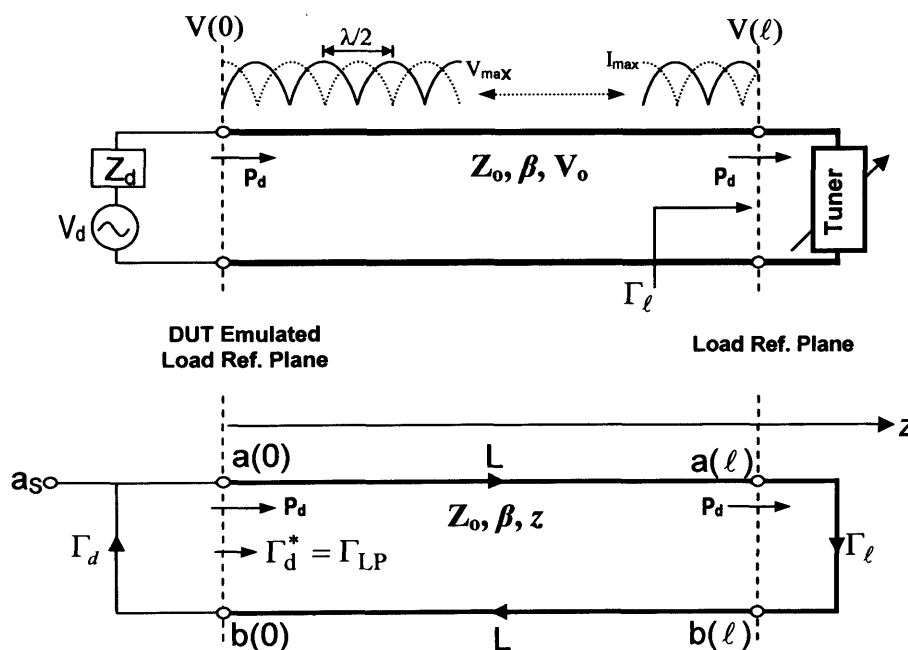


Fig. C.1 Passive load-pull measurement system methodology and its equivalent flow graph

Where a_s is the power wave generated by the DUT, Γ_d is the DUT reflection coefficient, Γ_{LP} is the load-pull reflection coefficient, Γ_ℓ is the load reflection coefficient and L is the transmission line delay.

The maximum available power delivered by the device under the conjugate match condition can be written as

$$P_{av} = \frac{a_s^2}{1 - |\Gamma_d|^2} \quad (C.1)$$

The maximum voltage at the DUT plane can be written in terms of the incident and reflected travelling waves as,

$$V(0) = \sqrt{2} \cdot (a(0) + b(0)) \cdot \sqrt{Z_o} = a(0)(1 + \Gamma_d^*) \cdot \sqrt{2 \cdot Z_o} \quad (C.2)$$

Where,

$$a(0) = a_s + b(0) \cdot \Gamma_d \quad (C.3)$$

$$b(0) = a(0) \cdot \Gamma_d^* \quad (C.4)$$

Substituting (C.4) into (C.3) yields,

$$a(0) = \frac{a_s}{1 - |\Gamma_d|^2} \quad (C.5)$$

Substituting (C.5) into (C.2) yield,

$$V(0) = \left(\frac{a_s}{1 - |\Gamma_d|^2} (1 + \Gamma_d^*) \right) \sqrt{2 \cdot Z_o} \quad (C.6)$$

The maximum voltage at the load reference plane can be written as,

$$V(\ell) = \sqrt{2} \cdot (a(\ell) + b(\ell)) \cdot \sqrt{Z_o} = a(\ell)(1 + \Gamma_\ell) \cdot \sqrt{2 \cdot Z_o} \quad (C.7)$$

The load reflection coefficient is related to the DUT reflection coefficient by

$$\Gamma_\ell \cdot L^2 = \Gamma_d^* \quad (C.8)$$

and when the DUT is conjugately matched then

$$|\Gamma_{LP}| = |\Gamma_d^*| \quad (C.9)$$

Hence the maximum voltage along the transmission path up to the load reference plane can be written as,

$$V(z) = \sqrt{2} \cdot a(\ell)(1 + \Gamma_\ell) \cdot \sqrt{Z_o} = a(0) \cdot L \left(1 + \frac{\Gamma_d^*}{L^2} \right) \cdot \sqrt{2 \cdot Z_o} \quad (C.10)$$

Substituting (C.5) into (C.10) yield,

$$V(z) = \frac{a_s}{1 - |\Gamma_d|^2} \cdot L \left(1 + \frac{\Gamma_d^*}{L^2} \right) \cdot \sqrt{2 \cdot Z_o} \quad (C.11)$$

Substituting (C.1) into (C.11) yield,

$$V(z) = \sqrt{2P_{av} \cdot Z_o \cdot (1 - |\Gamma_d|^2)} \cdot \frac{L}{1 - |\Gamma_d|^2} \cdot \left(1 + \frac{\Gamma_d^*}{L^2}\right) \quad (C.12)$$

Simplifying (C.12),

$$V(z) = \sqrt{\frac{2P_{av} \cdot Z_o}{1 - |\Gamma_d|^2}} \cdot L \cdot \left(1 + \frac{\Gamma_d^*}{L^2}\right) \quad (C.13)$$

Taking the magnitude of (C.13) yield,

$$V(z) = \sqrt{\frac{2P_{av} \cdot Z_o}{1 - |\Gamma_d|^2}} \cdot \left(1 + \frac{\Gamma_d^*}{L^2}\right) = \sqrt{\frac{2P_{av} \cdot Z_o}{1 - |\Gamma_d|^2}} \cdot \left(1 + \frac{\Gamma_{LP}}{L^2}\right) \quad (C.14)$$

Substituting $L = e^{j\beta z}$ into (C.14) yield

$$V(z) = \sqrt{\frac{2P_{av} \cdot Z_o}{1 - |\Gamma_d|^2}} \cdot \left(1 + \Gamma_{LP} \cdot e^{-2j\beta z}\right) \quad (C.15)$$

The maximum available delivered power P_{av} can be related to the actual delivered power P_d . In order for the DUT to deliver its maximum rated power, it needs to see its conjugately matched load. Based on the flow graph of Fig. C.1, the power delivered to the load P_d can be written as

$$P_d = a(0) \cdot a(0)^* - b(0) \cdot b(0)^* = a(0) \cdot a(0)^* (1 - |\Gamma_{LP}|^2) = |a(0)|^2 (1 - |\Gamma_{LP}|^2) \quad (C.16)$$

Also,

$$a(0) = a_s + \Gamma_d \cdot b(0) = a_s + \Gamma_d \cdot \Gamma_{LP} \cdot a(0)$$

Hence,

$$a(0) = \frac{a_s}{1 - \Gamma_d \cdot \Gamma_{LP}} \quad (C.17)$$

Substituting (C.17) into (C.16) yields

$$P_d = \frac{a_s^2}{|1 - \Gamma_d \cdot \Gamma_{LP}|^2} (1 - |\Gamma_{LP}|^2) \quad (C.18)$$

Substituting (C.1) into (C.18) yield

$$P_d = P_{av} \frac{(1 - |\Gamma_{lp}|^2)(1 - |\Gamma_d|^2)}{|1 - \Gamma_{lp}\Gamma_d|^2} \quad (C.19)$$

When the device is conjugately matched then $|\Gamma_{lp}| = |\Gamma_d|$ and (C.19) reduces to,

$$P_d = P_{av} \quad (C.20)$$

Substituting (C.20) into (C.15) for the conjugate match condition yield,

$$V(z) = \sqrt{\frac{2P_d \cdot Z_o}{1 - |\Gamma_{LP}|^2}} \cdot (1 + \Gamma_{LP} \cdot e^{-2j\beta z}) \quad (C.21)$$

Appendix D

LOAD-PULL POWER ANALYSIS FOR NON 50 OHM MEASUREMENT SYSTEMS

Consider the full signal flow graph model of Fig. D.1, where the active load-pull measurement system presented in chapter 4 of this thesis is connected to the DUT via an impedance transformer with reflection coefficient Γ . An equivalent reflection coefficient Γ_L is also included in the model to account for a non-matched measurement system.

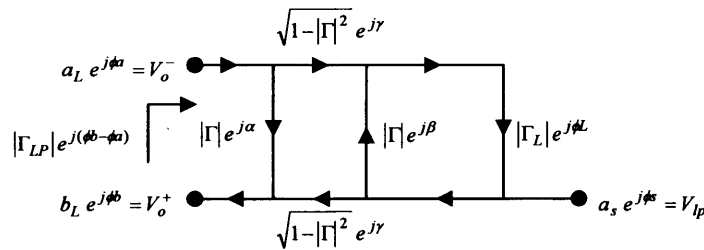


Fig. D.1 Error flow graph for the impedance transformer connected to a non-50 Ohm measurement system

The above model is also valid for a normal system without impedance transformer. This could be achieved by setting the transformer reflection coefficient Γ to zero. The impedance transformer signal flow graph of Fig. D.1 is assumed to be lossless therefore it obeys the lossless reciprocal network rules (Appendix B), which implies

$$\beta = 2\gamma - \alpha \pm n\pi \quad , n=\text{odd number} \quad (\text{D.1})$$

The load-pull reflection coefficient seen by the device can be defined as (equation 4.4)

$$\Gamma_{lp} = \frac{V_o^+}{V_o^-} = \frac{b_L e^{j\phi_b}}{a_L e^{j\phi_a}} = |\Gamma_{LP}| e^{j(\phi_b - \phi_a)} \quad (\text{D.2})$$

Also one can write (Fig. D1),

$$b_L e^{j\phi_b} = \Gamma_{in} a_L e^{j\phi_a} + \Gamma_T a_S e^{j\phi_s} \quad (\text{D.3})$$

Where

$$\Gamma_{in} = |\Gamma|e^{j\alpha} + \frac{(1-|\Gamma|^2)e^{j2\gamma}|\Gamma_L|e^{j\phi_L}}{1-|\Gamma|e^{j\beta}|\Gamma_L|e^{j\phi_L}}, \quad \text{and} \quad \Gamma_T = \frac{\sqrt{1-|\Gamma|^2}e^{j\gamma}}{1-|\Gamma_L||\Gamma|e^{j(\beta+\phi_L)}}$$

Since the active load-pull process deals with the relative phase between ϕ_a and ϕ_s , therefore ϕ_a could be set to zero to simplify the problem. Solving (D.3) for a_L and taking its magnitude squared yields,

$$|a_L|^2 = \frac{\left| \frac{\sqrt{1-|\Gamma|^2}e^{j\gamma}}{1-|\Gamma_L||\Gamma|e^{j(\beta+\phi_L)}} a_S e^{j\phi_s} \right|^2}{\left| \frac{|\Gamma_{LP}|e^{j\phi_b} - \frac{|\Gamma|e^{j\alpha} + |\Gamma_L|e^{j(2\gamma+\phi_L)}}{1-|\Gamma_L||\Gamma|e^{j(\beta+\phi_L)}}}{1-|\Gamma_L||\Gamma|e^{j(\beta+\phi_L)}} \right|^2} \quad (D.4)$$

Where $P_{LP} = |a_S|^2$

The net power delivered by the device is written as,

$$P_d = |a_L|^2 - |b_L|^2 \quad (D.5)$$

Substituting (D.2) into (D.5) and rearranging yields

$$P_d = |a_L|^2 - |\Gamma_{LP} a_L e^{j\phi_b}|^2 = |a_L|^2 (1 - |\Gamma_{LP}|^2) \quad (D.6)$$

Substituting (D.4) into (D.6) and simplifying yields

$$\begin{aligned} P_{LP} = P_d [& |\Gamma_{LP}|^2 + |\Gamma|^2 + |\Gamma_L|^2 + |\Gamma_{LP}|^2 |\Gamma|^2 |\Gamma_L|^2 - 2|\Gamma_L| \cdot |\Gamma| \cdot (1 + |\Gamma_{LP}|^2) \cdot \cos(\beta + \phi_L) \\ & - 2|\Gamma_{LP}| \cdot |\Gamma| \cdot (1 + |\Gamma_L|^2) \cdot \cos(\phi_b - \alpha) + 2|\Gamma_{LP}| \cdot |\Gamma_L| \cdot |\Gamma|^2 \cdot \cos(\beta + \phi_L + \phi_b - \alpha) \\ & - 2|\Gamma_{LP}| \cdot |\Gamma_L| \cdot \cos(\phi_b - 2\gamma - \phi_L)] / (1 - |\Gamma|^2) (1 - |\Gamma_{LP}|^2) \end{aligned} \quad (D.7)$$

Appendix E

KLOPFENSTEIN TAPER DESIGN

The Klopfenstein impedance transformer has the advantage of being the shortest (in length) impedance transformer for a given pass-band reflection coefficient [1]. The Klopfenstein taper is derived from a Chebyshev stepped impedance transformer, but where the number of sections increases to infinity.

The transformer design assumes a lossless system, and since this kind of transformers can only works on transforming real impedances this produces a purely imaginary propagation constant γ which is proportional to the frequency. The procedures presented here avoid detailed theory but summarizes the taper design procedures.

The design starts by specifying the desired transformer impedances which then can be used to calculate the transformer reflection coefficient at zero frequency [2],

$$\Gamma_0 = \frac{Z_L - Z_0}{Z_L + Z_0} \approx \frac{1}{2} \ln \left(\frac{Z_L}{Z_0} \right) \quad (\text{E.1})$$

The transformer resulting input reflection coefficient with a specified pass-band reflection coefficient can be found using the following equations [2].

$$\Gamma(\theta) = \Gamma_0 e^{-j\beta\ell} \frac{\cos \sqrt{(\beta\ell)^2 - A^2}}{\cosh(A)} \quad (\beta\ell)^2 \geq A^2 \quad (\text{E.2})$$

$$\Gamma(\theta) = \Gamma_0 e^{-j\beta\ell} \frac{\cos \sqrt{A^2 - (\beta\ell)^2}}{\cosh(A)} \quad A^2 \geq (\beta\ell)^2 \quad (\text{E.3})$$

where Γ_m is the passband ripple which is used to determine the variable ($\cosh A$)

$$\cosh(A) = \frac{\Gamma_0}{\Gamma_m} \quad (\text{E.4})$$

$$\text{Hence, } A = \cosh^{-1} \left(\frac{\Gamma_0}{\Gamma_m} \right) \quad (\text{E.5})$$

And ℓ is the taper length and; β is the propagation constant defined as;

$$\beta = \frac{2\pi}{\lambda} = \frac{2\pi \cdot f \cdot \sqrt{\epsilon_e}}{c} \quad (\text{E.6})$$

The Klopfenstein taper's pass-band region starts when $(\beta\ell) \geq A$ with "A" being the point at which the maximum reflection coefficient occurs in the passband. This then allows for the determination of the length of the taper required for a specified frequency by using the following equation.

$$\beta\ell = A \quad (E.7)$$

Having determined the taper length, the logarithmic characteristic impedance variation for Klopfenstein taper as a function of taper length can be used (equation E.8 below) to calculate the impedance at each impedance step [2]:

$$\ln(Z(z)) = \frac{1}{2} \ln(Z_0 Z_L) + \frac{\Gamma_0}{\cosh(A)} A^2 \phi\left(\frac{2z}{\ell} - 1, A\right), \quad \text{where } 0 \leq z \leq \ell \quad (E.8)$$

Where the function $\phi(x, A)$ is defined as,

$$\phi(x, A) = -\phi(-x, A) = \int_0^x \frac{I_1\left(A\sqrt{1-y^2}\right)}{A\sqrt{1-y^2}} dy, \quad \text{for } |x| \leq 1 \quad (E.9)$$

Where $I_1(x)$ is the modified Bessel function, equation (E.9) should be calculated numerically, alternatively a simple program for doing this is available in [3] which has been used in the transformer design used in this thesis.

Its worth mentioning that Klopfenstein taper experience discontinuous change in characteristic impedance at each end of the taper, this is due to the approximation made to the differential equation used to derive the taper formula [1]. Using equation

(E.1) in the format $\Gamma_0 = \frac{1}{2} \ln\left(\frac{Z_L}{Z_0}\right)$ ensure minimum discontinuity [1].

A program has been written which calculate the transformer impedance as a function of transformer length; this is shown in following procedures.

Specify first impedance $z1 := 7$
 Specify second impedance $z2 := 50$
 Speed transformer length in meter Length := 0.081
 Specify transformer reflection coefficient $gm := 0.01$

ϕ Function Evaluation

```
phi(z, A) :=
  ak ← 1
  bk ← 0.5 · z
  ck ← bk
  phi ← bk
  for k ∈ 1..1000
    fk ← k
    ck ← ck · (1 - z2)
    bk ← (ck + 2 · fk · bk) / (2 · fk + 1)
    ak ← (A2 · ak) / (4 · fk · (fk + 1))
    phi ← phi + ak · bk
```

Specify number of steps and calculate the impedance for each step

```
z0(z1, z2, gm, steps, Length) :=
  g0 ← 0.5 · ln(z2/z1)
  coshA ← g0 / gm
  A ← acosh(coshA)
  for zs ∈ 0..steps
    z ← zs / steps
    zin ← e0.5 · ln(z1 · z2) + (g0 / coshA) · A2 · phi(z, A)
    zout ← e0.5 · ln(z1 · z2) - (g0 / coshA) · A2 · phi(z, A)
    hsteps + zs, 1 ← zin
    hsteps - zs, 1 ← zout
    hzs, 0 ← (z / 2) · Length · 1000
    hzs + steps, 0 ← ((z / 2) + 0.5) · Length · 1000
  h
```

Evaluate the above function

```
v := z0(z1, z2, gm, 30, Length)
```

Write the matrix to a text file

```
WRITEPRN("c:\Transformer.dat") := v
```

References:

- [1] R. W. Klopfenstein, "A transmission line taper of improved design," *Proceedings IRE.*, vol. 44, pp. 31-35, January 1956.
- [2] D. M. Pozar, *Microwave Engineering*: John Wiley, ISBN 0-471-17096-8.
- [3] M. A. Grossberg, "Extremely rapid computation of the Klopfenstein impedance taper," *Proceedings of the IEEE*, vol. 56, pp. 1629 - 1630, September 1968.

Appendix F

IMPEDANCE TRANSFORMER CHARACTERISTIC IMPEDANCE MEASUREMENTS

Measuring the characteristic impedance of transmission lines with wide geometry can become a problem due to the large discontinuity that can exist between the measured line and the launching structure, which is normally a 50 Ohm structure. In this appendix, an attempt has been made to measure the impedance of the taper's (presented in chapter 4 of this thesis) low-impedance side.

Two methods have been adopted to determine the impedance transformer's characteristic impedance. The first uses a number of transmission line sections with different characteristic impedances, starting with 50 Ohm and ending with a line which has the same dimension as the taper's low-impedance side. Therefore the discontinuity effect between the 50 Ohm line and the taper's low-impedance side can be minimised. The second measurement method involved attaching a number of 50 Ohm terminations via SMA connectors to the transformer lower impedance side, and perform one-port measurement to extract the impedance. Both methods are discussed in details below.

F.1 Stepped Impedance Method

With the impedance transformer designed and fabricated, it was important to verify whether the impedances at both ends of the transformer were in agreement with the EM simulations. The authenticity of the impedances would confirm that the transformer was fabricated correctly and when it came to testing, allow for accurate characterisation of the transistor where all the measurement results are normalised to the impedance transformer's characteristic impedance. One of the methods adopted for extracting the impedance involved fabricating stepped impedances of the transformer. The stepped transmission lines can be fabricated to mimic the impedance changes along the taper as shown in Fig. F.1 below.

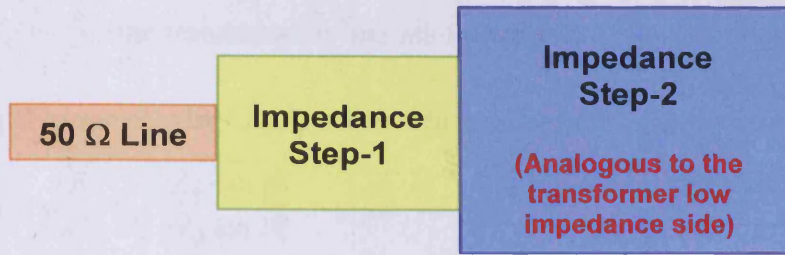


Fig. F.1 Stepped impedance methodology to aid measure the impedance of the transformer low impedance side

The high impedance (50Ω) side of the transformer was measured by simply fabricating a 10mm long transmission line with 1.325mm in width (the measured width at the transformer 50Ω side) using the same transformer board (TMM4) specified in this thesis.

All transmission line measurements have been conducted using the Anritsu Test Fixture (Fig. F.2) and HP 8510 Vector Network Analyser (VNA), the measurement system was calibrated using Anritsu in-fixture calibration standards. The transmission line's s-parameters are then measured and stored as a CITI file format, readable by Agilent Advanced Design System (ADS).



Fig. F.2 Anritsu universal test fixture

For a given length of transmission line, four s-parameters can be measured, from which the line characteristic impedance can be calculated. Firstly, the measured s-parameters are converted to ABCD parameters. Where for a transmission line of length ℓ , characteristic Impedance Z_0 and propagation constant β the transmission line ABCD matrix can be written as [1]:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos \beta \ell & jZ_0 \sin \beta \ell \\ jY_0 \sin \beta \ell & \cos \beta \ell \end{bmatrix} \quad (\text{F.1})$$

Where $Y_0 = \frac{1}{Z_0}$ (the transmission line admittance)

Dividing B-parameter by C-parameter while taking the square root yield:

$$Z_0 = \sqrt{\frac{B}{C}} = \sqrt{\frac{jZ_0 \sin \beta\ell}{jY_0 \sin \beta\ell}} = \sqrt{Z_0^2} \quad (\text{F.2})$$

Using the above-described method, the measured transmission line's s-parameters can be loaded into ADS and then used to calculate the line's characteristic impedance. The first measured transmission line was the 10 mm (50 Ω) which was measured up to 6 GHz. The line extracted impedance is shown in Fig. F.3 below.

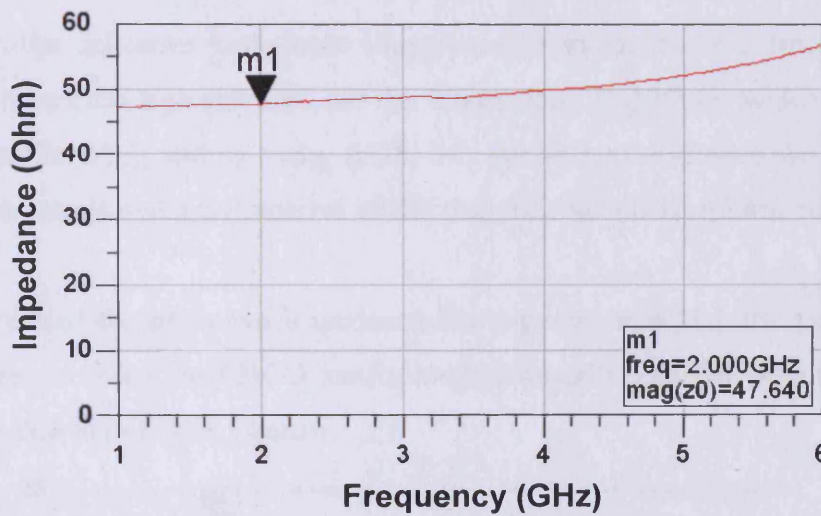


Fig. F.3 50 Ω line impedance plot as a function of frequency.

The results above shows that this line impedance is 47.64 Ω at 2GHz which represent the taper high impedance side.

The next step was to extract the characteristic impedance at the low-impedance end of the transformer. Since realising a 50 Ω to the 7 Ω transmission line is difficult due to a high level of mismatch (discontinuities). Therefore an intermediate stage (Impedance step-1 in Fig. F.1) was introduced to reduce this mismatch.

The stepped transmission line fabricated to do this is shown in Fig. F.4. It consists of a 10mm long 50 Ω line (47.64 Ω measured) of width 1.325mm that steps to a 10mm line length of width 4.6mm (of unknown impedance) and then back down to a 10mm line of width 1.325mm.

The stepped transmission lines combination of Fig. F.4 s-parameters were measured using the HP 8510 VNA. In order to extract the unknown impedance, (i.e. the line of width 4.6mm), the ABCD matrix method presented above was used.

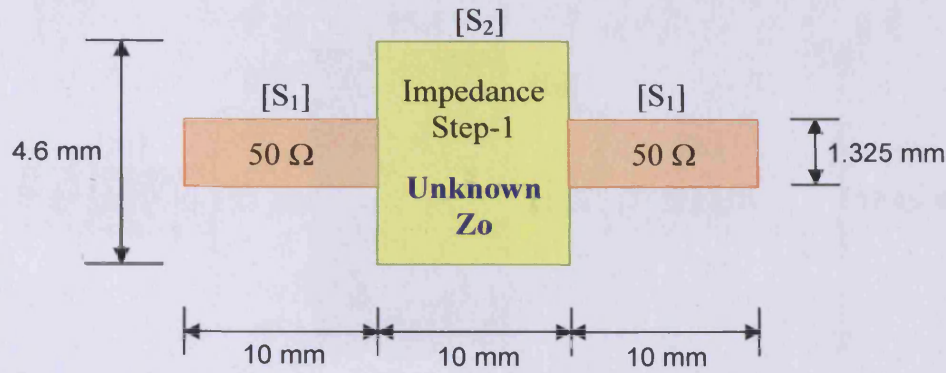


Fig. F.4 Illustration of the stepped transmission lines fabricated to extract the unknown impedance (Impedance step-1 of Fig. F.1)

To do that, the unknown impedance line s-parameters has to be extracted first $[S_2]$. Using the measured s-parameters for the 10mm long (1.325mm wide) transmission measured earlier $[S_1]$; and by using ADS, it is possible to de-embed the s-parameters $[S_1]$ from the measured s-parameters of the stepped transmission lines combination of Fig. F.4.

Having extracted the unknown impedance line s-parameters $[S_2]$, the line impedance can be extracted using the ABCD matrix method described earlier which revealed the impedance shown in Fig. F.5 below.

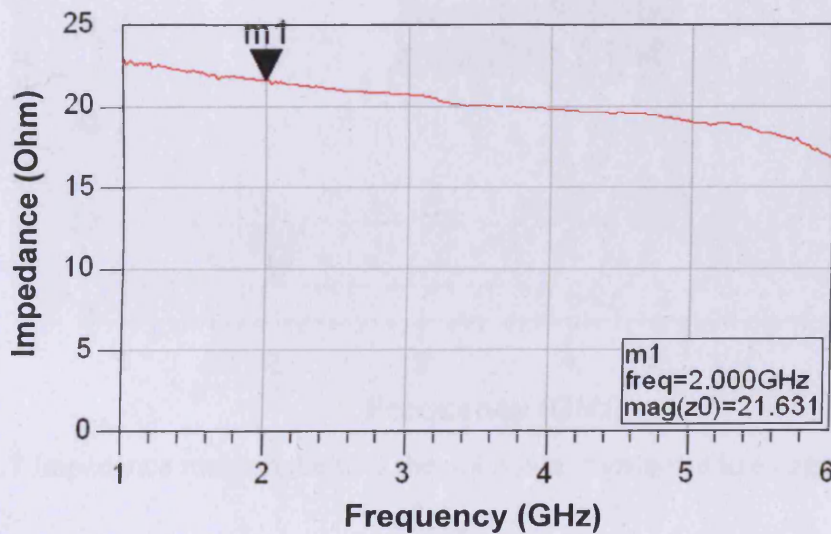


Fig. F.5 Impedance measurement of the unknown impedance line (Impedance step-1) of Fig. F.4

Another step is required to obtain the impedance at the transformer low impedance side. Therefore the stepped transmission lines combination of Fig. F.6. was fabricated.

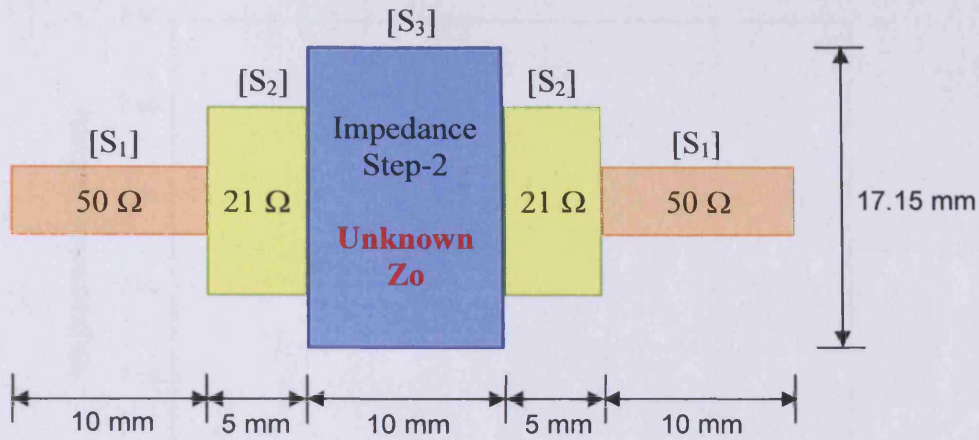


Fig. F.6 Stepped impedance transmission lines combination fabricated to extract the transformer low impedance side (Impedance step-2 of Fig. F.1)

Similar procedures used to extract the unknown impedance step-1 of Fig. F.4 were used to extract the impedance step-2. Using the stepped transmission lines combination of Fig. F.6 and by using the de-embedding techniques using ADS as done previously it was possible to extract the s-parameters $[S_3]$ for the impedance step-2 line of Fig. F.6 from which the line impedance was extracted (Fig. F.7).

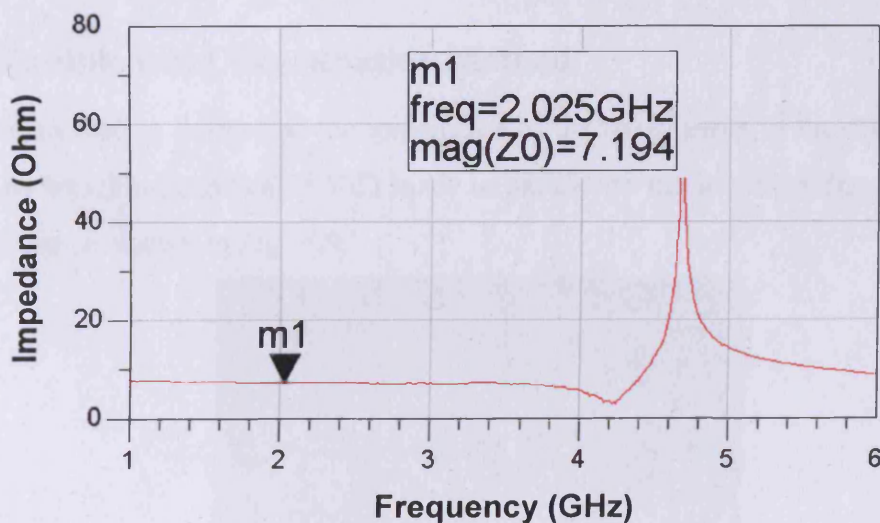


Fig. F.7 Impedance measurement of the unknown impedance line (impedance step-2 of Fig. F.6)

Putting the impedance step-2 geometry into ADS-LineCalc reveal the impedance of this line to be 7.13Ω at 2 GHz, which is in a very good agreement with the measured value. The above impedance value can be compared with that of the HFSS simulations used for the design of the transformer as shown in Fig. F.8 below.

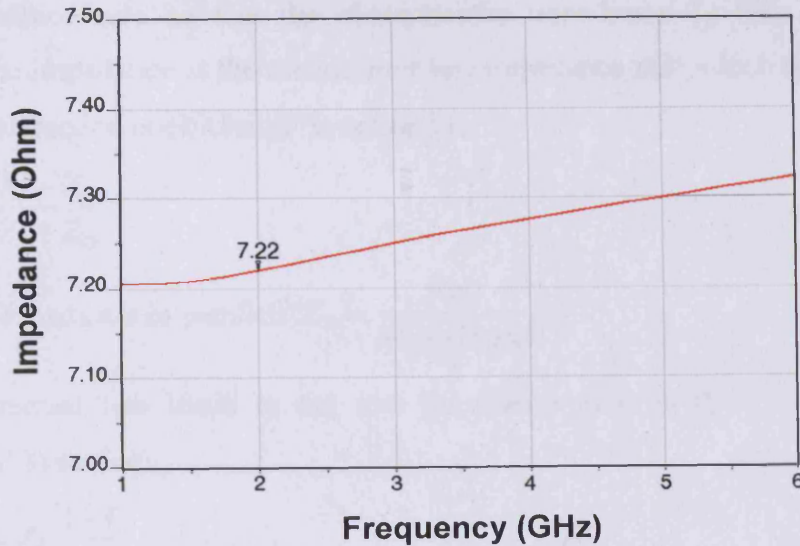


Fig. F.8 HFSS impedance simulation results at the transformer low impedance side

Both the simulated values (7.17Ω using HFSS and 7.13Ω using ADS-LineCalc) and the measured value of 7.19Ω are very close. This result further confirms that the ABCD matrix method used for extracting the impedance from the stepped line is reasonably good for such complex stepped lines combination (Fig. F.1).

F.2 Multiple Load Termination Method

Another method to determine the impedance of the transformer at the low impedance end is by attaching a series of 50Ω loads in parallel to the low impedance side of the transformer as shown in Fig. F.9.

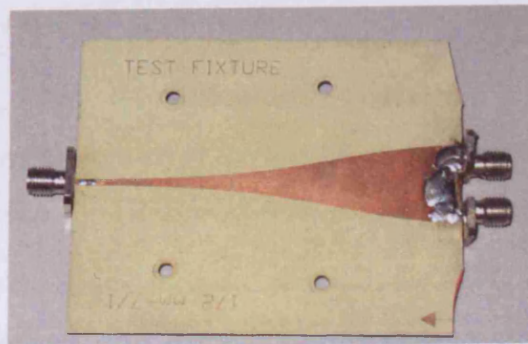


Fig. F.9 A broadband impedance transformer terminated with two 50Ω SMA launchers on the low impedance side

By terminating the low impedance side into two 50Ω loads which is equivalent to 25Ω broadband termination (assuming that the terminations are exactly 50Ω) this automatically transforms the load(s) attached to the transformer to the transformer

high impedance side so that the characteristic impedance Z_0 seen by the VNA becomes the impedance at the transformer low impedance side which is thought to be (7Ω). The reflection coefficient Γ is defined as:

$$\Gamma = \frac{Z_l - Z_0}{Z_l + Z_0} \quad (\text{F.3})$$

As the 50Ω loads are in parallel: $Z_l = \frac{50\Omega}{\text{No. of loads}}$

Having attached two loads to the low impedance side so $Z_l = 25\Omega$. Re-arrange equation (F.3) so that:

$$Z_0 = Z_l \frac{1 - \Gamma}{1 + \Gamma} \quad (\text{F.4})$$

Using calibrated HP 8510 VNA, a one port measurement was performed to measure the transformer reflection coefficient (Γ). ADS was used to calculate Z_0 (Fig. F.10) using equation (F.4) for a frequency range of (1-6GHz).

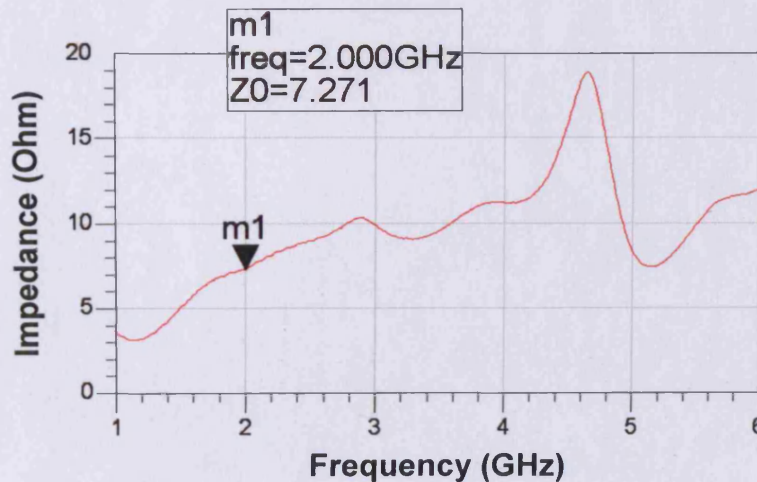


Fig. F.10 Impedance measurement of the low impedance side of the transformer for a frequency range 1-6 GHz using multiple load termination method

From the above figure the impedance was found to be 7.27Ω at 2 GHz. This value is similar to the value obtained using the stepped impedance method, ADS-LineCalc and HFSS simulations. The results of Fig. F.10 above shows how the method begins to produce discontinuities at higher frequencies; the method can be improved by attaching a number of precision loads to the transformer low-impedance side.

The similarity in the values obtained using the multiple load and stepped impedance methods suggests that both measurement methods are reasonably adequate in extracting the impedance at the transformer low impedance side.

Further improvement can be performed on the stepped impedance method is by measuring more lines with different lengths and different combinations. The measured results can then be averaged to obtain more accurate impedance measurement over wider bandwidth.

References:

- [1] D. M. Pozar, *Microwave Engineering*: John Wiley, ISBN 0-471-17096-8.

PUBLICATIONS

DC-50 GHz Low Loss Thermally Enhanced Low Cost LCP Package Process Utilizing Micro Via Technology

Z. Aboush¹, J. Benedikt¹, J. Priday² and P. J. Tasker¹

¹Cardiff University, School of Engineering, Cardiff CF24 3TF, UK – AboushZ@cf.ac.uk

²Labtech Limited, Broadaxe Business Park, Presteigne, Powys, LD8 2UH – J.Priday@labtech.ltd.uk

Abstract — This paper describes the design, simulation and measurements of a novel 5X5mm² surface mount Liquid Crystal Polymer (LCP) package which uses micro vias as a means of signal transition. The new package offers excellent thermal dissipation due to a cavity for device mounting, hence, eliminating the need for thermal vias. For the package design a novel matching technique was developed to match the micro via to 50Ω transmission line. The novel design allowed for a broadband response with 0.3dB of insertion loss and 20dB return loss up to 50GHz. The package achieved 40dB of isolation (after bonding) for a 1.2mm MMIC gap. To obtain accurate package s-parameter measurements a 2-tier calibration procedure was deployed to rapidly extract the package response. Further developments utilizing the good thermal conductivity of the new package technology for high-power LDMOS devices are presented

Index Terms — Broadband Communication, Calibration, Ceramics, Laser Machining, Microstrip, MMICs, Packaging.

I. INTRODUCTION

Miniaturization, power and increasing functionality are main drivers for future wireless communication systems. Also broadband wireless applications such as computer network equipment and multiband RF/microwave modules are placing RF packaging technology under continuous pressure to fulfill these requirements whilst maintaining low cost.

Since RF components are normally packaged, RF performance can be strongly affected. Substrate materials such as LTCC have been widely employed in package manufacturing [1] which can provide an excellent RF performance but yet are still rather expensive. Plastic SMT packages have been reported [2] which can reduce the cost however at the expense of RF performance. New organic liquid crystal polymer substrates [3][4] on the other hand have shown their abilities to provide a very good alternative to LTCC material by providing excellent performance while significantly driving down the costs [5].

A further important characteristic for MMIC packages is their thermal conductivity as MMIC devices generate a lot of heat at high frequencies. In particular, GaAs devices are subject to this problem because of the poor thermal conductivity of GaAs. Previously reported packages [5] address this problem by incorporating thermal vias directly underneath the MMIC device. This approach has its limitation however since only a finite number of vias can be placed between the mounting board and the device. The package proposed in this paper provides excellent heat dissipation by

placing the die inside a cavity in the dielectric thus eliminating the need for thermal vias, consequently reducing the cost even further. However in order to be able to miniaturize the package and allowing for hermeticity, micro vias [6] were introduced. In contrast to conventional through vias [7] the micro via results in better control of the impedance of the via transition section. A positive outcome was that no changes in the geometry of the feed lines were necessary to compensate for the via effect, giving a broadband performance of the manufactured packages.

II. PACKAGE DESCRIPTION

The package consists of two layers of metallization (Fig.1). The bottom plane contains a short section of transmission line connected to a coplanar waveguide with 50 Ohm characteristic impedance. On the top plane a 50 Ohm microstrip line is connected to the bottom plane using a micro via. The micro via is terminated into a cylinder base to provide the necessary capacitance to ground. Unlike previous package technologies, this package has a 2 mm cavity for the direct mounting of MMICs onto the solid bottom gold plated copper layer. The advantage of using the cavity is to provide excellent thermal dissipation which eliminates the need for thermal vias.

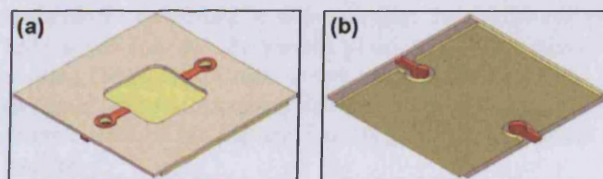


Fig. 1 Proposed Thermally and Electrically Enhanced LCP Package Layout (a) Top View, (b) Bottom View.

III. PACKAGE DESIGN AND OPTIMIZATION

The motivation behind this work is to design a package with an all-pass filter characteristic with very low losses whilst introducing minimum interruption in the signal flow within the transition between the package and the structure onto which the package will be mounted. In almost all cases the mounting structure consists of transmission lines connecting the LCP package with a circuit board. To achieve the all-pass filter characteristic of the LCP package and its smooth integration with the mounting board, it was decided to design

a package which has an equivalent circuit model similar to that of a transmission line. The models of a transmission line consist of either a series of T- or π -section networks of capacitances and inductances producing an all-pass filter. The series of networks can be extended through additional similar T- or π -sections without decreasing the bandwidth of the resulting new network. Thus, matching the equivalent circuit model of the package to the one of the transmission line should ensure a minimal effect on the signal flow.

To achieve this, a small signal circuit model was derived for the package based on the package structure and is shown in detail in Fig. 2. The floating transmission line (T_1) at the bottom plane represents the launching point from a coplanar mounting structure. The section with no coplanar mounting structure underneath is referred to as the transmission line T_2 , which is connected through a via structure to 50 Ohm microstrip line T_3 on the top layer.

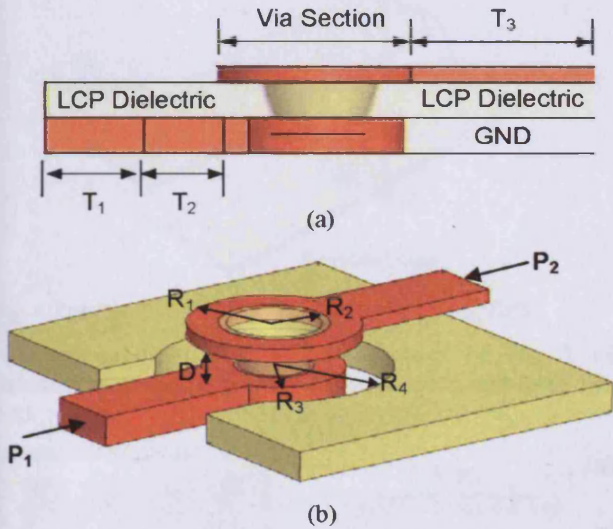


Fig.2 One Side of the LCP Package Shown in 2D Representation (a) and 3D Representation (b).

Based on the package geometry shown in Fig. 2, a simple equivalent circuit can be derived (Fig. 3),

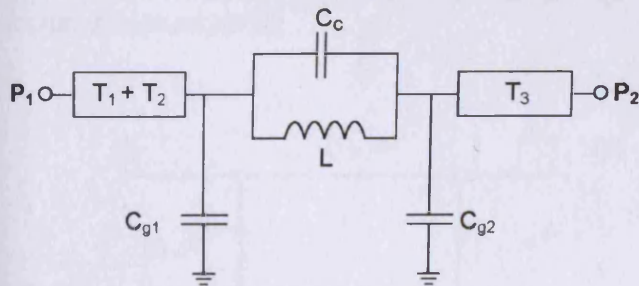


Fig. 3 Package Equivalent Electrical Circuit.

In this model the via was modeled as an inductance in parallel with capacitance, the inductance L comes from the

via's self inductance, whilst the coupling capacitance C_C comes from the coupling between the top and bottom pads around the via. The capacitances to ground C_{g1} and C_{g2} represent the coupling of the top and bottom via pads to the ground plane.

Within the resulting model, the parallel combination of L and C_C forms bandstop filter which will resonate at $f_o = 1/2\pi\sqrt{LC_C}$. This characteristic is contrary to the required broadband behavior of an all-pass filter. However, the section consisting of the inductance L and the capacitances C_{g1} and C_{g2} resembles the π -section of the equivalent circuit model of a transmission line. To increase the similarity further it is important to reduce or even eliminate the capacitance C_C . This can be accomplished by two methods, i.e. either by reducing the dielectric thickness D which will lead to an increase in the capacitance's even mode and therefore reduce the odd mode, or by misaligning the via top and bottom pads. The disadvantage of the first method is that it will give rise to the capacitance C_{g2} . The second method can be achieved rather readily through the use of micro via where the top via radius is increased relatively to the bottom via radius. Applying both methods on the coupling capacitance C_C it was possible to dramatically decrease its value, thus virtually eliminating it from the equivalent electrical model – at least as a first approximation. As a result the simple π -section similar to the one of a transmission line is obtained. However, the two capacitances values at both ends of the via, without any optimization, yield a low-pass filter characteristic.

To further approximate the package characteristics to that of a transmission line it is important that an arrangement where $C_{g1} = C_{g2} = C_g$ is attained. The capacitances C_{g1} and C_{g2} were formed by the introduction of two additional features within the LCP package; firstly is the ground plane at the bottom layer and secondly the pads at the bottom and top layer connecting the micro via to the transmission lines T_2 and T_3 . Both can be controlled by either varying the gap between the bottom via pad and the ground plane ($R_4 - R_3$) and/or by varying the effective mean geometric distance of the top via pad from the bottom ground. To balance out both capacitances at both sides of the via the following relationship could be realized

$$R_4 - R_3 \approx \sqrt{D^2 + (R_4 - R_1)^2} \tag{1}$$

With the right hand side of (1) relating to the effective mean geometric distance between the top via pad and the bottom ground.

Conclusively, the introduction of the micro via with pads on the bottom and top layer as well as the ground plane allow a 50 Ohm environment to be maintained across the via section ($Z_o = \sqrt{L/C_g}$) over a large bandwidth. To further optimize the broadband behavior of the new package the radius of the via has been kept large. This maximizes the available surface for the conduction of the signal, hence, minimizes the surface impedance effect due to the decreasing skin depth with an increasing frequency.

It is interesting to note that the above introduced structure and its flexibility can be readily utilized to take into account the effect of bonding wires. For instance, the capacitance to ground C_{g2} could be tuned to provide the conjugate matching for the bonding wire inductance.

IV. PACKAGE SIMULATION, REALIZATION AND MEASUREMENT

A liquid crystal polymer laminate Rogers R/flex3000 (D.K. 2.9) was chosen as a package substrate. The dielectric thickness was $100 \mu\text{m}$ with $50 \mu\text{m}$ and $100 \mu\text{m}$ gold plated copper cladding on the package top and bottom surfaces respectively. Based on the discussion presented in the previous section, the package has been designed and its s-parameters have been simulated using Ansoft HFSS. The simulation was performed for only one side of the package as shown in Fig. 4

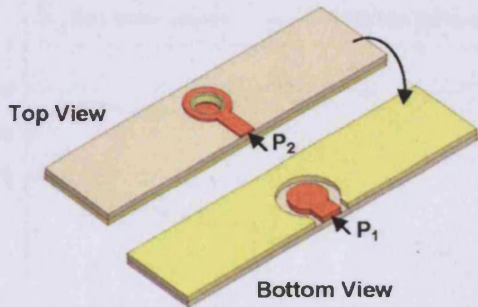


Fig. 4 One Side LCP Package Representations Using HFSS.

Following the simulations, the package of Fig. 1 was manufactured with a set of TRL calibration standards (Fig. 5.a).

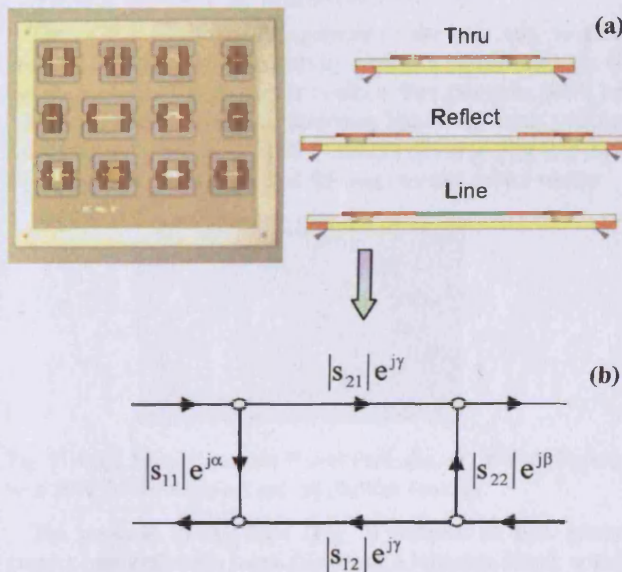


Fig. 5 (a) In Package TRL Calibration Standards, (b) One Package Side Error Flow Graph (S-Parameters).

These calibration standards consist of the package itself for the open standard and packages with a modified geometry to realize the thru and line standards. The measurement process included a 2-tier calibration process. First the measurement system, consisting of an Agilent 8510 VNA, was calibrated up to its on-wafer probes using an on-wafer TRM calibration. In the second step a second tier [8] calibration was carried out using the TRL calibration standards described above.

From the TRL cal (2nd tier) step a complete error model for the package was obtained, representing the actual package s-parameters (Fig. 5.b). One draw back of this method of characterization is the fact that the actual insertion loss of the package is not available as independent parameter, but always as the product $|s_{21}||s_{12}|e^{j2\gamma}$ (Transmission Tracking Coefficient) of s_{21} and s_{12} parameters.

In order to extract the insertion loss of the package the square root of the transmission tracking coefficient should be taken to obtain $\pm|s_{21}|e^{j\gamma}$. The resulting sign ambiguity can be resolved using the lossless reciprocal networks properties [9].

$$S_{11}S_{12}^* + S_{21}S_{22}^* = 0 \tag{2}$$

Once the phase is decided then the package s-parameters are available and can be readily imported into a CAD program (e.g. ADS) as a measurement based model, hence, allowing its use within the design process of the MMIC.

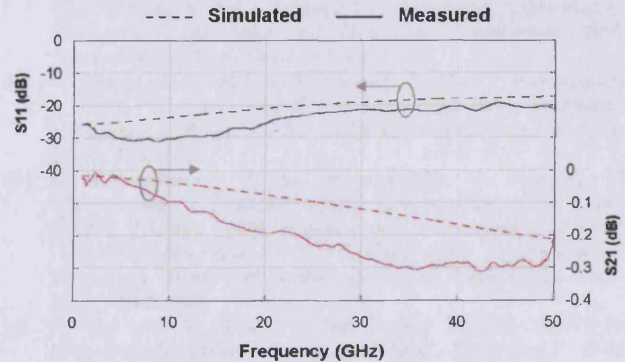


Fig. 6 Measured and Simulated S-Parameters for the Package of Fig.5

Having done the above procedures, the actual s-parameters for one side of the package were measured and compared to the simulation results (Fig. 6)

From these measurement results (Fig.6) it can be seen that the package has sustained 20 dB of return loss and 0.3 dB insertion loss up to 50 GHz. Comparing the measured results to the corresponding simulated data shows a good agreement.

To investigate the effect of bond wires on the isolation performance of the package, a basic measurement has been carried out. For this measurement the package feed lines on the top layer (P2 in Fig.4) were bonded to the cavity ground on both sides leaving 1.2mm gap between the two bonding wires. The resulting package isolation was found to be better than -40 dB (Fig. 7) over the entire bandwidth.

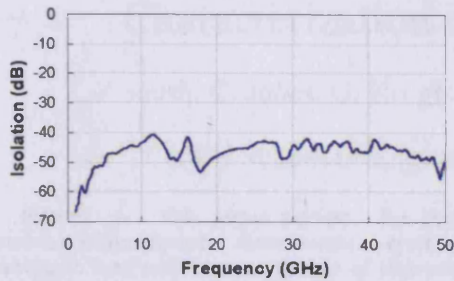


Fig. 7 Package Isolation measured with bond wires to ground.

To identify the effect of the lid on the package performance, further measurement was carried out on a $5 \times 5 \text{ mm}^2$ package (with 2mm thru line in the middle) with and without the lid. Again, the measurement results revealed that the package lid had a minimum effect (Fig. 8).

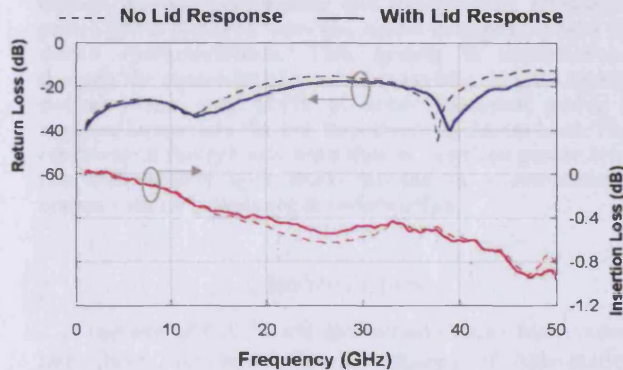


Fig. 8 Package Performance With and Without the Lid.

V. FURTHER DEVELOPMENTS

The LCP laminate process presented above is very versatile and its high thermal conductivity makes it highly suitable for the packaging of high power devices. For example, 30W and 100W packages based on laminates have also been realized. Initial measurements of 30W LDMOS devices (Fig 9.a) have confirmed the good predicted RF and thermal performance.



Fig. 9 High Power Laminate Based Packages, (a) 30Watt Package with 30W Device Attached and (b) 100Watt Package.

The package in this case (Fig 9) consists of gold plated copper heat sink with 1 mm thickness, a laminate frame which has been cut using laser technology to form the input/output conductor wings and the laminate ring which isolates the input and output leads from the electrically conductive heat sink.

The laminate structure is bonded to the heat sink using FR4 film. Finally the package is capped with a lid made of the same laminate material. At present measurement are under way to evaluate the performance of these high-power laminate based packages.

VI. CONCLUSION

A novel, low-loss thermally enhanced LCP package has been presented. The low manufacturing costs make the package suitable for a large range of RF and high-frequency applications. The optimized micro via design coupled with good characteristics of the LCP materials result in a very good package performance suitable for frequencies up to at least 50 GHz. Furthermore, the flexibility of the presented novel packaging process has been demonstrated by presenting high-power packages optimized for basestation transistors for the telecommunication industry.

ACKNOWLEDGEMENT

The authors would like to thank Labtech Ltd UK for funding this activity and manufacturing the presented package components.

REFERENCES

- [1] K. Yoshida, T. Shirasaki, S. Matsuzono and C. Makihara, "50 GHz Broadband SMT Package for Microwave Applications," *Electronic Components and Technology Conference*, 2001. Proceedings, 51st, pp. 744 - 749, June 2001.
- [2] H. Huang, A. Ezzeddine, A. Darwish, B. Hsu, J. Williams and S. Peak, "Ku-Band MMIC's in Low Cost SMT Compatible Packages," *IEEE MTT-S Int. Microwave Symp. Dig.*, vol.1, pp. 27-30, June 2002.
- [3] D. Thompson, O. Tantot, H. Jallageas, G. Ponchak, M. Tentzeris and J. Papapolymerou, "Characterization of Liquid Crystal Polymer (LCP) Material and Transmission Lines on LCP Substrates From 30 to 110 GHz," *IEEE Transactions on Microwave Theory and Techniques*, vol.52, Issue 4, pp. 1343 - 1352, April 2004.
- [4] Z. Wei and A. Pham, "Liquid Crystal Polymer (LCP) for Microwave/Millimeter Wave Multilayer Packaging," *IEEE MTT-S Int. Microwave Symp. Dig.*, vol.3, pp. 2273 - 2276, June 2003.
- [5] H. Kanno, H. Ogura and K. Takahashi, "Surface Mountable Liquid Crystal Polymer Package with Vertical Via Transition Compensating Wire Inductance up to V-band" *IEEE MTT-S Int. Microwave Symp. Dig.*, vol.2, pp. 1159 - 1162, June 2003.
- [6] R. Abhari and T.E. van Deventer, "Analysis of Microvia Interconnects," *IEEE MTT-S Int. Microwave Symp. Dig.*, vol.3, pp. 1925 - 1928, June 1998.
- [7] W. Simon, R. Kulke, A. Wien, M. Rittweger, I. Wolff, A. Girard and J.P. Bertinet, "Interconnects and Transitions in Multilayer LTCC Multichip Modules for 24 GHz ISM-Band Applications," *IEEE MTT-S Int. Microwave Symp. Dig.*, vol.2, pp. 1047 - 1050, June 2000.
- [8] G.F. Engen and C.A. Hoer, "Thru-Reflect-Line": An Improved Technique for Calibrating the Dual Six-Port Automatic Network Analyzer," *IEEE Transactions on Microwave Theory and Techniques*, vol.27, Issue 12, pp. 987 - 993, December 1979.
- [9] David M. Pozar, "Microwave Engineering," Wiley, ISBN 0-471-17096-8.

High Power Active Harmonic Load-Pull System for Characterization of High Power 100Watt Transistors

Z. Aboush, C. Jones, G. Knight, A. Sheikh, H. Lee, J. Lees, J. Benedikt and P. J. Tasker

Cardiff School of Engineering, Cardiff University, Cardiff, CF24 0YF, UK

Abstract — This paper presents, for the first time, a waveform/time-domain measurement system with active harmonic load pull that is capable of characterising 100W LDMOS devices. In order to achieve the required high-power capability the measurement system employs a new bias-tee design [1] coupled with broadband impedance transformers [2]. The unique characteristics of the high-power bias-tee increases the performance of the measurement system up to 12GHz, 100W CW for the RF channel, and 100V, 10A for the DC channel. The broadband impedance transformers are embedded within the time-domain measurement system and dramatically reduce the power levels required from the active load-pull system for device characterization. This system is demonstrated through the successful characterisation of a 100W LDMOS device, where only 120W of active load-pull power is required to emulate the low impedance optimum load. This represents a remarkable reduction in required power from the impractically high 688W needed in a conventional system with no impedance transformation.

I. INTRODUCTION

A number of CAD tools and measurement instruments have been developed for the design of base-station amplifiers. However, the CAD tools are completely dependent on the availability of accurate large-signal models and hence large-signal data, i.e. current and voltage waveforms. Instrumentation for the characterisation of devices at higher power levels is generally limited to passive load pull systems [3][4]. One disadvantage of the passive approach is the time required to perform a complete load-pull characterisation of a device. This becomes particularly noticeable when devices are optimised for harmonic as well as fundamental loads, in which case the device performance has to be measured for many combinations of the harmonic impedances. For example, an optimisation over three harmonics with a grid containing 100 points at each frequency would lead to 100^3 measurements. Furthermore, sweeping impedances at the device output plane provides only limited understanding of the device mode of operation, which becomes an important point when analysing the device or amplifier performance. The ability to measure and control the relative phase of all harmonics is critical when characterising more complex, multiple-device structures such as the Doherty amplifier.

These disadvantages, i.e. the extensive measurement times and lack of information can be overcome by a time domain/waveform measurement systems in combination with an active load-pull allowing for device optimisation through waveform engineering [5].

Until now, there has been no active harmonic load-pull measurement system that can accommodate device power levels in excess of 30W. This is a limitation that can be

attributed to two significant factors: Firstly, the difficulty in achieving the required power handling capability of all critical system components such as bias-tee's, and secondly, the rapidly increasing load-pull power required due to increasing differences between the measurement system characteristic impedance (50Ω) and the DUT optimum impedance (sub 2Ω).

The impedance differential can also result in high standing wave ratios in excess of 25 that can cause very large voltage and current peaks along the transmission path. These can easily damage fragile system components.

In this paper a novel system capable of measuring high power devices in excess of 100W is presented. It is constructed by combining an active harmonic load-pull measurement system [1][5], with high power bias-tees¹ [1] which uses a novel design involving the connection of two 90° hybrid couplers back to back. Broadband impedance transformers [2][6] have been designed and are inserted between the DUT and the measurement system in order to reduce the measurement system characteristic impedance at the device plane to a level much closer to the device impedance. As the transformers are resonance free over a wide bandwidth (1-12 GHz), the system can be fully calibrated using standard TRL calibration techniques, thus allowing active harmonic load-pull measurements.

II. MEASUREMENT SYSTEM DESCRIPTION AND LIMITATIONS

A measurement system (Fig.1) combining time domain waveform and active load-pull entities has been developed at Cardiff University [1][5].

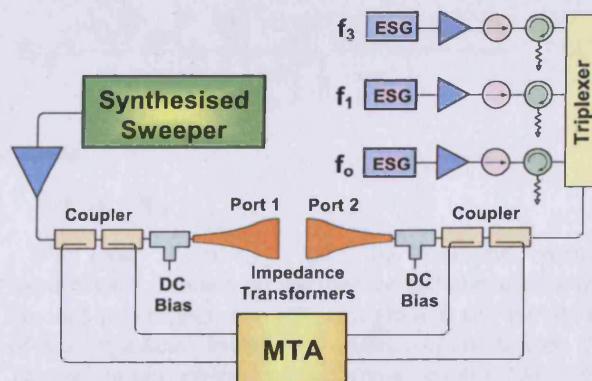


Fig. 1. Active load-pull measurement system including the impedance transformer

¹ Supplied by MPower Microwave Ltd, Cardiff, UK

Fig. 1 illustrates the block diagram of this system, which essentially measures the absolute incident and reflected waveforms at the calibrated reference plane, and is based around the two channel Microwave Transition Analyser (MTA). The synthesized sweeper is used as a source signal generator, while the active load-pull system comprises a set of phase coherent signal generators and amplifiers (with 200 Watt fundamental drive amplifier) that are responsible for presenting the desired fundamental and harmonic impedances. With the exception of the DUT, the characteristic impedance of the system is 50 Ohm.

Fig. 2 represents a 100 Watt device inserted into the measurement system of Fig. 1, the device has been modeled as a simple voltage source (V_d) in series with an impedance (Z_d).

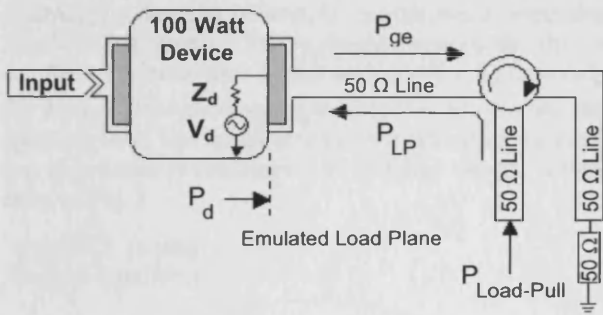


Fig. 2. Impedance Mismatch Representation for the Active Load Pull System

The large relative difference (Fig. 2) between the system and DUT impedances limits the capability of conventional load-pull systems when measuring the low impedance associated with many high power devices, therefore the system has been modified to accommodate impedance transformers at the DUT input and output ports which bring the system characteristic impedance down to a level that allows high power devices to be load-pulled quite easily.

II. BROADBAND IMPEDANCE TRANSFORMER ANALYSIS

To analyze the impedance transformer effect, consider the model of Fig. 3 where a 100 Watt device is connected to the load-pull measurement system via two impedance transformers (Klopfenstein Taper).

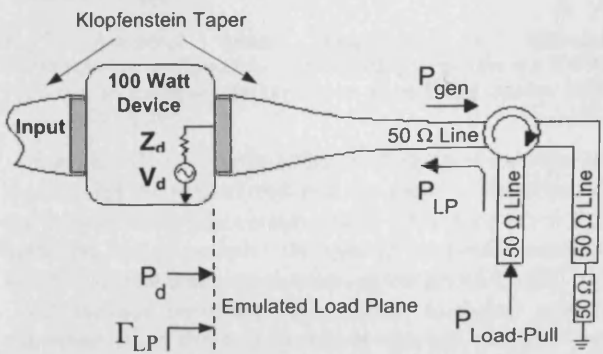


Fig. 3. Impedance Transformation Representation for the active Load-Pull System

The power delivered into the emulated load at the device reference plane is limited by three important factors; the load-pull power amplifier capacity, the difference between the device optimum impedance and the characteristic impedance of the measurement system, and finally the power rating of the device itself.

The process of active load-pull involves injecting a phase coherent RF signal from the load-pull source (P_{LP}) in order to balance the RF power generated by the device (P_{gen}) such that the required load is presented. The difference $P_{gen} - P_{LP}$ will give the net power delivered (P_d) to the emulated load at the device reference plane.

The transformer effect on the load-pull power levels could be modeled and derived using the simple signal flow graph (SFG) of Fig. 4 below,

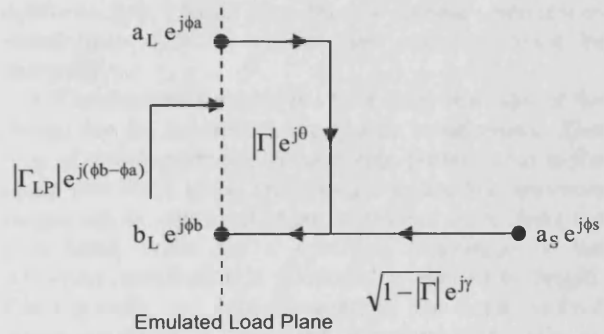


Fig. 4. Lossless Impedance Transformer Signal Flow Graph (SFG) Representation on the Measurement System Load Side.

Where $a_S e^{j\phi_s}$ represents the injected complex signal to the transformer from the load-pull source, $|\Gamma|$ is the impedance transformer reflection coefficient which is basically a measure of the transformation ratio, while $|\Gamma_{LP}| e^{j(\phi_b - \phi_a)}$ is the load-pull reflection coefficient seen by the device at the DUT plane (emulated load plane).

A formula [7] which relates the load pull power (P_{LP}) to the impedance transformer reflection coefficient ($|\Gamma| e^{j\theta}$) and the load-pull reflection coefficient ($|\Gamma_{LP}| e^{j\phi}$) has been modified to include the load-pull reflection coefficient phase and the impedance transformer reflection coefficient phase,

$$P_{LP} = \frac{P_d \left(|\Gamma_{LP}|^2 + |\Gamma|^2 - 2|\Gamma_{LP}||\Gamma| \cos(\phi - \theta) \right)}{\left(1 - |\Gamma_{LP}|^2 \right) \left(1 - |\Gamma|^2 \right)} \quad (1)$$

Where,

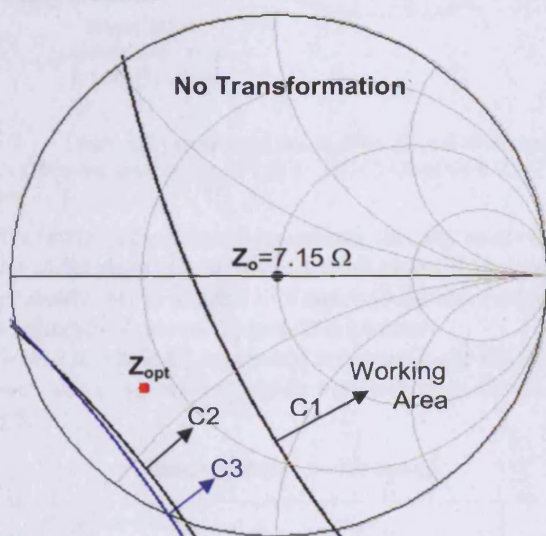
$$\phi = \phi_b - \phi_a$$

It's clear from (1) that the load-pull power requirements depends on the relative difference between the load-pull reflection coefficient phase ϕ and the phase of the impedance transformer reflection coefficient θ . The minimum power occurs when $\phi - \theta = 0$ and the cosine term goes to 1.

Therefore in order to minimize the load-pull power requirement it is essential to have $\theta = \phi$, which can be achieved by adding a length of the low impedance line or line-stretcher (the effect of this extra line could be removed using conventional TRL cal procedure). If this is not the case, the load-pull power requirement will increase as the angle ϕ departs from θ with the resultant load-pull power being obtained from (1).

To demonstrate the advantage of using the tapered impedance transformer, as quantified by (1), consider a 100 W device with ideal optimum impedance $Z_{opt} = (1.7 - j2.55)$ Ohm. Without transformation, the required load-pull power needed to emulate the optimum load is 688W, and a high VSWR (>25). By incorporating a broadband impedance transformer with a ratio 50:7.15 and without using any line extension, the load-pull power requirement dramatically drops to 75 watt. If, in addition, a correcting length of transmission line is placed between the device and the impedance transformer such that $\theta = \phi$, then only 61 Watt of load-pull power is required to emulate the optimum load. The limitations and the advantage of using the impedance transformer are clarified on the Smith chart of Fig. 5.

C2: 50→7.15 With
No Line Extension



C3: 50→7.15 With
Line Extension

Fig.5. Load-pull power constraints for different transformation configuration. Each contour represent the 200W P_{LP} limit, as computed by (1) for an ideal 100W device with $Z_{opt} = 1.7 - j2.55$ Ohm

Note that C1 contour is offset from the real axis due to the fact that the system load-pull contours are function of the device load-pull contours itself. Therefore when the optimum load is complex the system load-pull contours will follow that complex position on the Smith Chart.

C2 contour represents the system load-pull power constraint when the transformer is inserted between the DUT and the 50 Ohm system. Again this contour has been rotated due to the complex optimum load.

Finally C3 contour represents the system power constraints after inserting a length of transmission line

between the DUT and the low impedance side of the impedance transformer. In this particular case, since $\phi - \theta$ is only 2.3° (see Fig. 7), the addition of the line extension only has a minor effect.

Selecting the impedance transformation ratio is rather critical. A high transformation ratio requires the transformer to be physically very long and thus possess significant transmission losses. Also for a device with unknown optimum impedance, going for high transformation ratio can reduce the area of Smith chart which could be scanned using the available load-pull power. Therefore an optimisation process is necessary to find the optimum transformation ratio. One solution is to do a coarse scan around Smith chart with no impedance transformer present to identify in which quarter the optimum lay, based on that a proper impedance transformer with or without line stretcher could be designed.

A Klopfenstein taper [6] has been used as a basis of the design for the broadband impedance transformers. This type of transformer delivers optimum performance in the sense that for a given taper length it has the minimum magnitude of input reflection coefficient throughout the pass band, while for a specified magnitude of the reflection coefficient it produces a minimum length. Consequently, an impedance taper has been realised which produces a measured transformation ratio of 50:7.15 over a 1-12 GHz bandwidth. Roger TMM4 board with 0.762 mm dielectric thickness has been used and the resulting taper length is 81 mm. The realised set-up consisting of the 100W device between two Klopfenstein tapers and the high-power bias-tee, attached to the output side, are depicted in Fig. 6.

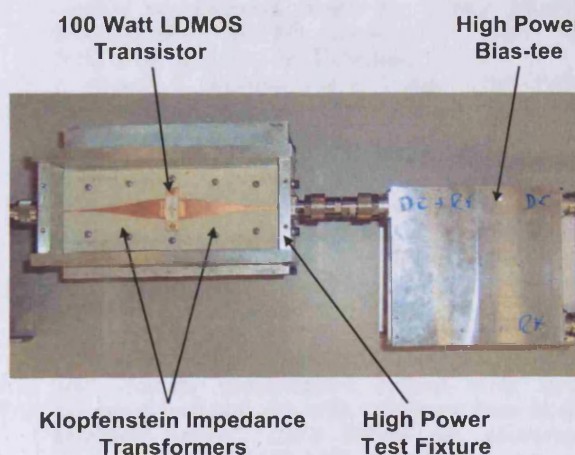


Fig.6. High power test fixture suitable for measuring high power devices (>100 Watt)

IV. EXPERIMENTAL RESULTS

Using a fundamental frequency of 2.135 GHz, the system as shown in Fig. 1 was calibrated using a two-tier approach [8]. This involved firstly a calibration up to the coaxial reference plane of the system, and then additional TRL calibration to move the reference plane up to the DUT plane. Utilising the transformer, a 100W Motorola

(Freescale) LDMOS device (Fig. 6) was biased at $V_{GS}=3.85V$ and $V_{DS}=28V$ ($I_{dq}=1A$).

Following a comprehensive load-pull measurement and generation of contours of constant powers, (Fig.7), the optimum load was found to be $(1.643-j3.562) \Omega$ at the DUT reference plane which shows good agreement with the optimum device impedance provided by the device data sheet $(1.7-j2.55)\Omega$.

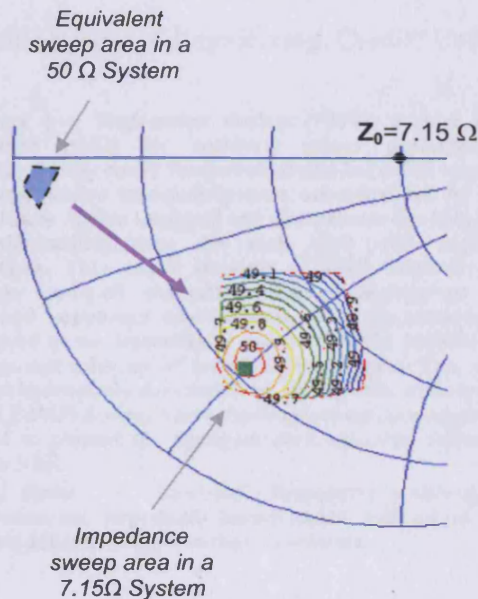


Fig.7. Load-pull power contours in dBm for a 100W device with Optimum impedance of $1.643 - j3.562$ Ohm with $Z_0=7.15$ ohms

The measured optimum impedance and the data sheet value differ slightly in terms of a small phase shift, which is probably due to a small difference (0.44mm) between the reference planes of the test-fixtures used.

Whilst maintaining a constant optimum load, the input power was swept with resulting measurements shown in Fig.8.

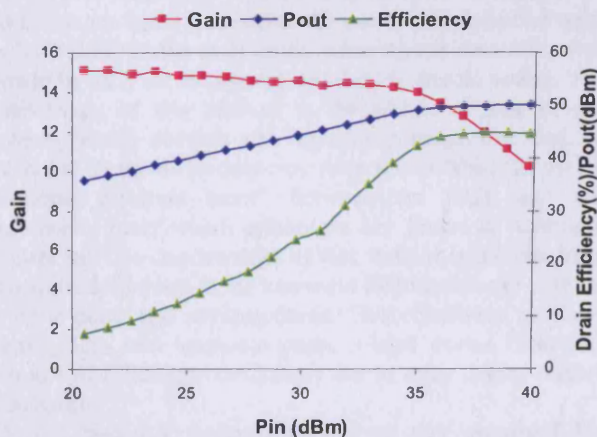


Fig.8. Measured Pout, Efficiency and Gain vs Pin when load-pull to its optimum load thus delivering over 100Watts

The system was able to load-pull the device at the optimum impedance, up to a maximum device output

power of 101.45W. By incorporation of the taper into the measurement system only a load-pull source output power of 120.22 Watt, hence VSWR <10, was required to generate the necessary optimum low impedance $(1.643 - j3.562$ Ohms). This includes the constraint that in order to emulate the optimum load the active load-pull system had to also overcome a 1.2 dB of loss between the DUT and the load-pull amplifier.

V. CONCLUSION

A novel, high-power, active harmonic waveform/time-domain measurement system, incorporating harmonic load pull is presented, allowing for the first time comprehensive device characterisations and optimisations at the high power levels relevant to base-station PA applications. This system has been successfully characterised a 100W LDMOS device whilst using only 120 W of load-pull power. The nature of the measurement system enables multiple harmonic load-pull and consequently accurate measurement of the voltage and current waveforms at the device plane

ACKNOWLEDGEMENT

The authors would like to thank Labtech Ltd for funding this activity. Atlantic Microwave Ltd for supplying components and MPower Microwave Ltd for supplying the bias-tees.

REFERENCES

- [1] J. Benedikt, and P. Tasker, "High power time-domain measurement bench for power amplifier development", *ARFTG Conference Digest, Fall 2002*, 60th, pp.107-110, December 2002.
- [2] Z. Aboush, J. Benedikt, and P. Tasker, "High Power Harmonic Active Load-Pull Using Broadband Impedance Transformers", *High Frequency Postgraduate Student Colloquium*, pp. 145-150, Sept. 2004.
- [3] Maury Microwave Corporation, "Device Characterization with Harmonic Source and Load Pull", *Application Note 5C-044*, December 2000.
- [4] Focus Microwave, "Load Pull Measurements on Transistors with Harmonic Impedance Control", *Technical Note*, Aug. 1999
- [5] J. Benedikt, R. Gaddi and P. J. Tasker, "High power time domain measurement system with active harmonic load-pull for high efficiency base station amplifier design", *IEEE MTT-S Int. Microwave Symp. Digest*, pp. 1459-1462, June 2000.
- [6] R. W. Klopfenstein, "A Transmission line taper of improved design" *Proc. IRE*, vol. 44, pp. 31-15, January 1956.
- [7] Z. Aboush, J. Lees, J. Benedikt, P. Tasker, "Active Harmonic Load-pull for Characterizing Highly Mismatched High Power Transistors", *IEEE MTT-S Int. Microwave Symp. Digest*, June 2005.
- [8] J. F. Sevic, "A Sub 1Ω Load-pull Quarter-wave Pre-matching Network Based on a Two-tier TRL Calibration", *ARFTG Conference Digest, Computer-Aided Design and Test for High-Speed Electronics*, 52nd, pp. 73-81, December 1998.

Active Harmonic Load-Pull System for Characterizing Highly Mismatched High Power Transistors

Zaid Aboush, Jonathan Lees, Johannes Benedikt and Paul Tasker

Cardiff School of Engineering, Cardiff University, Cardiff, CF24 0YF, UK. E-mail: AboushZ@cf.ac.uk

Abstract — High-power devices (>30W) require low load impedances (<5Ω) for optimum power performance. In presenting the necessary fundamental and harmonic impedances, traditional passive load-pull systems are restricted by inherent system losses. Active load-pull can compensate for this problem, but unfortunately does not scale well with high power applications. This paper presents a novel solution allowing harmonic load-pull characterization of high-power devices. Broadband impedance transformers allow the necessary load-pull power to be dramatically reduced whilst maintaining the accuracy and integrity of measured waveforms. This approach has been successfully demonstrated through the measurement of a 30W LDMOS device, where the required active load-pull power required to present the optimum load has been reduced from 270W to 50W.

Index Terms — Load-pull, impedance matching, device characterization, impedance transformers, microwave and RF power amplifiers, voltage/current waveforms.

I. INTRODUCTION

Traditionally, mechanical tuners are used to identify optimum loads for efficiency, linearity, and output power. These passive systems suffer from one major problem however; any losses introduced between the Device Under Test (DUT) and the load-pull system will reduce the range of load impedances that can be realized. This is especially true for highly reflective loads, and is exacerbated when extending the passive load-pull concept to harmonic frequencies. For this reason, it is important that the load-pull tuners are placed as close to the DUT as possible.

Harmonic tuning can be accomplished in a number of ways: One method [1] involves the use of a triplexer between the DUT and fundamental tuner, allowing the remaining two ports to be used for the second and third harmonic tuning. The disadvantage of this method is the additional loss of the triplexer, which reduces the impedance range that can be realized at harmonic frequencies. A second method [2] uses a “harmonic rejection tuner” between the DUT and the fundamental tuner which minimizes any losses at harmonic frequencies. The disadvantage of this method is the resulting reflection coefficients at the harmonic frequencies can only be varied in phase and not magnitude. This effectively prevents investigations into harmonic phase related device behavior, such as low reflection coefficients due to lossy device output capacitance.

Active load-pull systems, similar to that proposed by Takayama[3], avoid this limitation by actively compensating

for any losses introduced between the DUT and the load-pull system, allowing any Smith chart impedance to be realized. There is however a fundamental problem associated with the implementation of the active load-pull systems: Due to the large impedance differential between the device optimum impedance (typically <5Ω) and the characteristic impedance of the measurement systems (50Ω), active load-pull systems do not scale well to high power levels.

This paper presents a simple yet novel solution that overcomes these limitations through the use of broadband impedance transformers. The transformation of “relevant” harmonic frequencies to lower impedances maintains the overall shape and integrity of the voltage and current waveforms that exist at the device plane. The transformers are resonance free and can be fully calibrated using standard TRL calibration.

II. IMPEDANCE MISMATCH CONSIDERATION

To analyze the mismatch problem, a 100W device had been chosen to help highlight the underlying problem. Consider the scenario shown in Fig.1 where a 100W DUT is modeled as a simple 20 V rms voltage source in series with a 1 Ohm resistor.

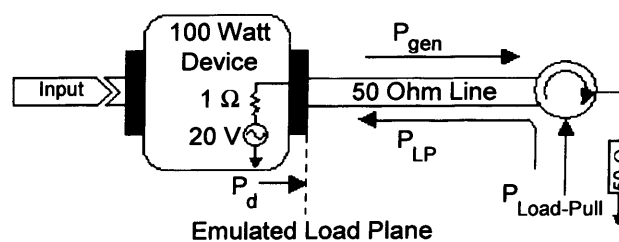


Fig.1. Impedance Mismatch Representation for the Active Load Pull System

The power delivered into the emulated load depends on three constraints; the maximum power delivered by the load-pull amplifiers; the difference between the device optimum impedance and the characteristic impedance of the measurement system, and finally the output power rating of the device itself.

Whilst performing the load-pull actively on the power transistor, a phase coherent RF signal has to be injected from

the load-pull source (P_{LP}), to balance the RF power wave generated by the device (P_{gen}). The ratio of these power waves relates to the load-pull reflection coefficient, while the difference determines the power delivered by the device to the emulated load (P_d)[5].

$$P_{LP} = \frac{P_d |\Gamma_{LP}|^2}{1 - |\Gamma_{LP}|^2} \quad (1)$$

In order to emulate 1 Ohm impedance at the device reference plane the load pull source has to deliver 1200W to the device (1). This level of power is prohibitively large and can create a large VSWR that can damage the system. Hence an alternative solution is required to bring the load pull power level down to a reasonable level.

III. BROADBAND IMPEDANCE TRANSFORMER SOLUTION

The solution to this problem is to reduce the impedance difference, which can be achieved either by reducing the impedance environment of the entire measurement system, i.e. using couplers, bias tee, etc. with a non 50 ohm characteristic impedance, or by inserting impedance transforming networks between the DUT and the measurement system. For the first solution, working with 10 Ohm system would be preferred, however the design of the couplers, bias tee, etc to meet the increasing current demands is very challenging. Therefore the utilization of the impedance transformer just before the DUT is the more practical solution.

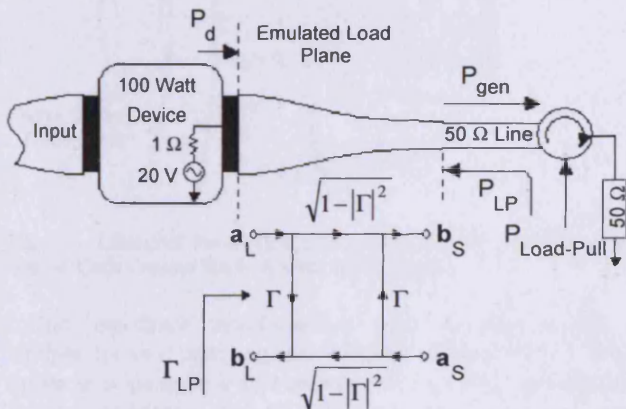


Fig. 2. Impedance Transformation Representation for the active Load-Pull System

To realize the impact of the impedance transformer consider the model shown in Fig. 2 above, here the device is connected to the measurement system via the broadband impedance transformer. Based on the model above, the effect of introducing the impedance transformer can be modeled with the simple signal flow graph shown, consequently the load-pull behavior of the system is modified as follows

$$P_d = a_L^2 - b_L^2 \quad (2)$$

$$b_L = \Gamma a_L + \sqrt{1 - |\Gamma|^2} a_S \quad (3)$$

Also

$$\Gamma_{LP} = \frac{b_L}{a_L} \quad (4)$$

Solving for (2,3,4) it is very easy to show that the Load-Pull power is defined as

$$P_{LP} = a_S^2 = \frac{P_d |\Gamma_{LP} - \Gamma|^2}{(1 - |\Gamma_{LP}|^2)(1 - |\Gamma|^2)} \quad (5)$$

It is clear from (5) that the effect of the impedance transformer is much stronger on the numerator than the denominator which leads to a reduced load-pull power requirement. It's important to mention that optimum power requires $\phi(\Gamma_{opt}) = \phi(\Gamma)$ which could be achieved by simply adding a length of the low impedance line.

For a 100 watt device with 1 Ohm optimum impedance (5) could be used to plot the load-pull power requirement against the load-pull reflection coefficient for various impedance transformation ratios this is shown in Fig. 3.

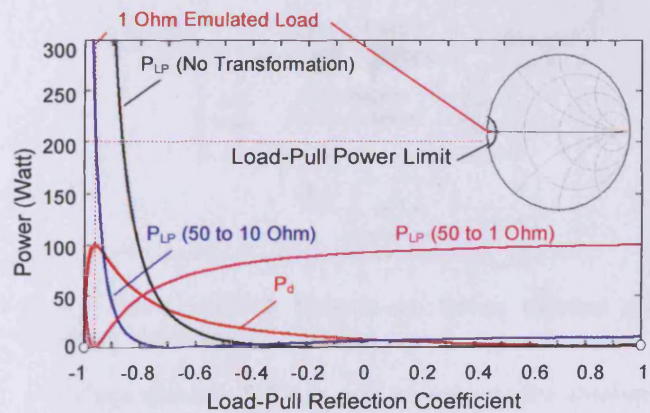


Fig. 3. Load-Pull Power vs. Load-Pull reflection Coefficient for Different Impedance Transformation Ratios along the Loci of Γ_{opt} Which in This Case the Real Axis

Note that the load-pull reflection coefficient extremes of Fig.3 are not defined by (5) as the ratio 0/0 can only be solved by considering the voltages and currents at these points.

For the same device another curve which relates the required load-pull power to the impedance transformation ratio at a fixed load-pull reflection coefficient is shown in Fig. 4.

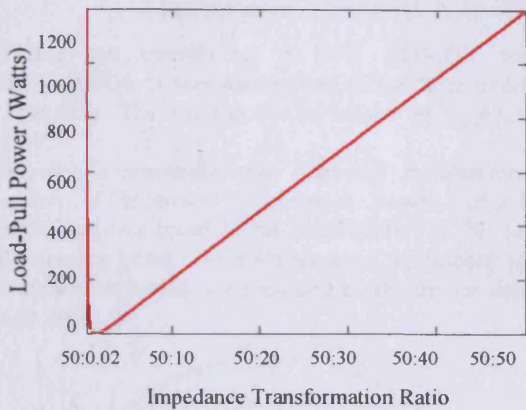


Fig.4 Load-Pull Power Requirement vs. Impedance Transformation Ratio for a 100W 10Ohm Optimum Impedance Device

This in turn could be plotted on a smith chart to showing how big an area can be covered for a given transformation ratio assuming for the maximum power delivered by the load-pull amplifiers $P_{LP}=200W$, as shown in Fig.5.

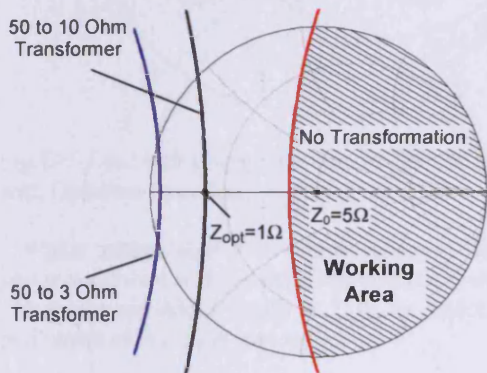


Fig.5. Load-Pull Power Constraints for Different Transformation Ratios, Each Contour Represent the 200W Limit

The impedance transformation ratio decision is not a straight forward task, e.g. for a 100W device with 1 Ohm optimum impedance a 50:1 transformer might be possible but impractical because then the transformer has to be very long which lead to increase the transmission losses by the time the signal reaches the device reference plane it can loose up to -3 dB of its strength. Therefore an optimisation process is necessary to find the optimum transformation ratio.

Another important issue, due to the fact that the impedance transformer works only on transforming real impedances then if the device optimum impedance does not lay on the real axis of the smith chart (typically it won't) then the load-pull power requirement will increase by the amount the optimum point depart from the real axis.

During the design of the broadband impedance transformer the Klopfenstein taper [6] has shown the optimum performance in the sense that for a given taper length it has the minimum magnitude of input reflection coefficient throughout the pass band. Additionally, for a specified tolerance for the magnitude of the reflection coefficient the taper has shown to produce a minimum length. Consequently, a Klopfenstein impedance taper has been realised on site producing a measured transformation ratio of 50:9.47 over a 1-12 GHz bandwidth. For the realisation a Roger TMM4 board with 0.762 mm thickness has been used. The resulting taper length is 77 mm.

IV. MEASUREMENT SYSTEM SETUP

Fig. 6 illustrates the block diagram of a measurement system combining time domain waveform measurements and active load-pull developed over the past few years at Cardiff University[7,8], modified to incorporate the impedance transformers.

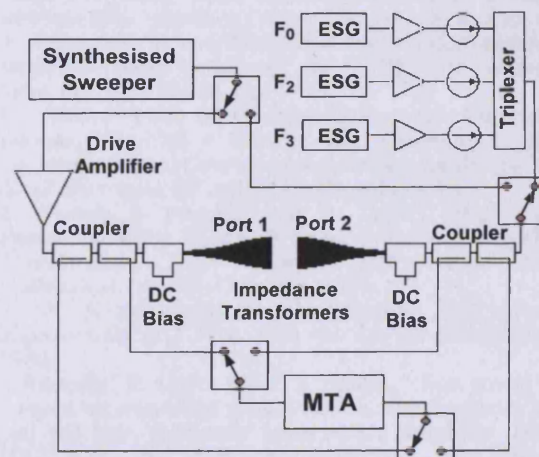


Fig. 6. Active Load-Pull Measurement System Including the Impedance Transformer

The two channels MTA is used to measure the absolute incident and reflected waveforms on the device input and output ports, the synthesized sweeper is used as a signal generator, while the active load-pull system comprises a set of signal generators at multiple frequencies which could be set using a CAD program. To perform load-pull measurements at high power levels a 200 W power amplifier is used to drive the fundamental path. Apart from the DUT, the characteristic impedance of the system is 50 Ohm.

The system was calibrated (1.8-11 GHz) in 2 steps. First a calibration had been performed up to the coaxial reference of the system. In the second step a TRL calibration has been performed to move the reference plane up to the DUT.

V. EXPERIMENTAL RESULTS

Utilising the transformer a 30W LDMOS transistor (PHILIPS ILSG4-4) was load-pulled at 1.8 GHz under class AB operation. The transistor was biased at $V_{GS}=3.5V$ and $V_{DS}=25V$.

Following a comprehensive load-pull measurement and generation of contours of constant power, (Fig.7), the optimum load was found to be $Z_{opt}=(1.74 - j3.25) \Omega$ at the DUT reference plane which shows good agreement with the optimum device impedance provided by the device data sheet $(1.31-j3.28) \Omega$.

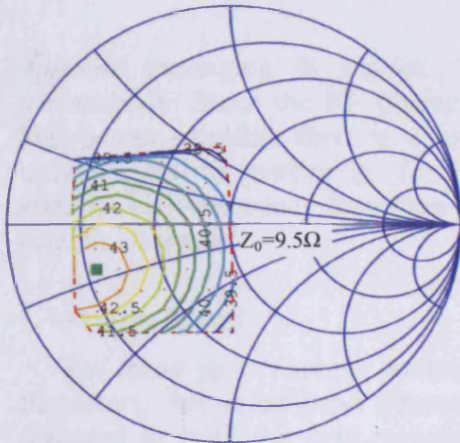


Fig.7. Load-pull Power Contours in dBm for a 30W Device with Optimum Impedance of 1.74-j3.25 Ohm

Whilst maintaining a constant optimum load, the input power was swept with resulting measurements shown in Fig.8. The maximum output power is 23W for which only a load-pull power of $P_{LP}=32W$ was sufficient.

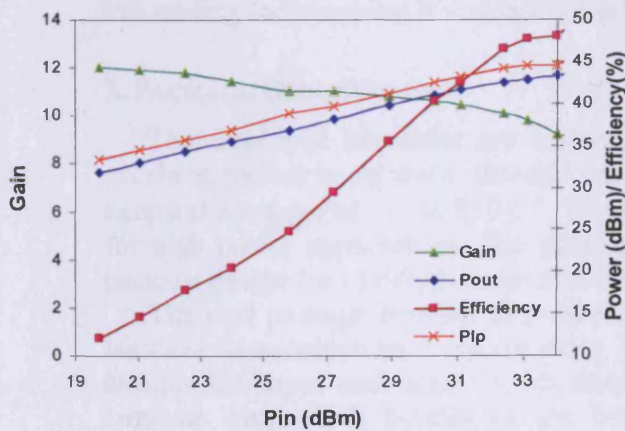


Fig.8. Pin vs Pout, P_{LP} , Efficiency, and Gain.

VI. CONCLUSION

The novel active load-pull system presented in this paper has shown the ability to reduce the load-pull power requirement significantly; utilizing the broadband impedance transformer allowing to synthesize any impedance at any frequency at the DUT plane with an acceptable active load-pull power requirement. The resulting reduction in the required maximum power delivered by the load-pull ($P_{LP,max}$) has clearly demonstrated on a 30W LDMOS device.

ACKNOWLEDGEMENT

The authors would like to thank Labtech Ltd for funding this activity.

REFERENCES

- [1] Maury Microwave Corporation, "Device Characterization with Harmonic Source and Load Pull," *Application Note 5C-044*, December 2000.
- [2] Focus Microwave, "Load Pull Measurements on Transistors with Harmonic Impedance Control," *Technical Note*, Aug. 1999
- [3] Y. Takayama, "A new load-pull characterization method for microwave power transistors," *IEEE MTT-S Int. Microwave Symp. Dig.*, pp. 218-220, June 1967.
- [4] J. F. Sevic, "A Sub 1Ω Load-pull Quarter-wave Pre-matching Network Based on a Two-tier TRL Calibration," *ARFTG Conference Digest, Computer-Aided Design and Test for High-Speed Electronics, 52nd*, pp. 73-81, December 1998.
- [5] Z. Aboush, J. Benedikt, and P. Tasker, "High Power Harmonic Active Load-Pull Using Broadband Impedance Transformers," *High Frequency Postgraduate Student Colloquium*, pp. 145-150, Sept. 2004.
- [6] R. W. Klopfenstein, "A Transmission line taper of improved design," *Proc. IRE*, vol. 44, pp. 31-15, January 1956.
- [7] J. Benedikt, R. Gaddi and P. J. Tasker, "High power time domain measurement system with active harmonic load-pull for high efficiency base station amplifier design" *IEEE MTT-S Int. Microwave Symp. Dig.*, June 2000, pp. 1459-1462
- [8] J. Benedikt, and P. Tasker, "High power time-domain measurement bench for power amplifier development," *ARFTG Conference Digest, 60th*, pp.107-110, 5-6 Dec. 2002.
- [9] P. Bouysse, J. Nedus, J. Coupat, and J. Villotte, "A novel accurate load-pull setup allowing the characterization of highly mismatched power transistors," *IEEE Transaction on Microwave Theory and Techniques*, vol. 42 No. 2, February 1994.

Novel Cost-efficient Packaging Technology for High-Power LDMOS Devices

Zaid Aboush, Johannes Benedikt, John Priday* and Paul Tasker

Cardiff University, School of Engineering, Cardiff CF24 3TF Wales

Tel: +44 (0)2920879095: AboushZ@cf.ac.uk

*Labtech Limited, Broadaxe Business Park, Presteigne, Powys, LD8 2UH, UK

Tel: +44 (0)1544 260093, Fax: +44 (0)1544 260310, j.priday@labtech.ltd.uk

Abstract: Packaging is crucial factor in maximizing the RF power transistors performance. Since the RF power device is the most expensive component within a high-power amplifier there is a substantial market pressure to reduce the cost of the transistor and its packaging. This paper presents a novel packaging technology which uses the high-frequency laminates as a base material replacing the currently dominant ceramic packages.

1. INTRODUCTION

For many years ceramic packages [1], [2] have been used to house the RF power transistors, due to its good thermal and electrical performance this kind of packages managed to fulfil the performance and reliability demands on RF power transistors. However, the resulting costs per package comprise a significant part of the overall price of the high-power transistor, hence, numerous developments have been undertaken in the past to develop more cost-effective packaging.

This paper presents a novel packaging technology suitable for high power applications (>30 Watts). The new package is based on high-frequency laminates, allowing for parallel simultaneous processing of several hundreds of packages, hence reducing the price per package. In addition, the employed printing board technology has low tooling costs making it viable for smaller markets.

2. PACKAGE DESCRIPTION

The employed laminates are ceramic-filled PTFE composites, which provide an excellent dielectric constant, thermal expansion and mechanical stability over a wide temperature range of -55 to 250 C°. These specifications make this board very suitable for high power applications. The package technology is demonstrated on a 30 Watt package design for LDMOS devices and is shown in Fig. 1.

The new package consists of gold plated copper heat sink with 1 mm thickness, a laminate frame which has been cut using laser technology to form a laminate ring which isolates the input and output leads from the electrically conductive heat sink. The laminate structure is bonded to the heat sink using FR4 film. For environmental protection, the package is capped with a lid made of the same laminate material (or any other suitable material) which in turn glued to the laminate ring and the input and output leads. The gold plated copper leads thickness is 100 µm, based on the die thickness the laminate thickness could be chosen to mate the die accordingly to reduce the required bond wire length.

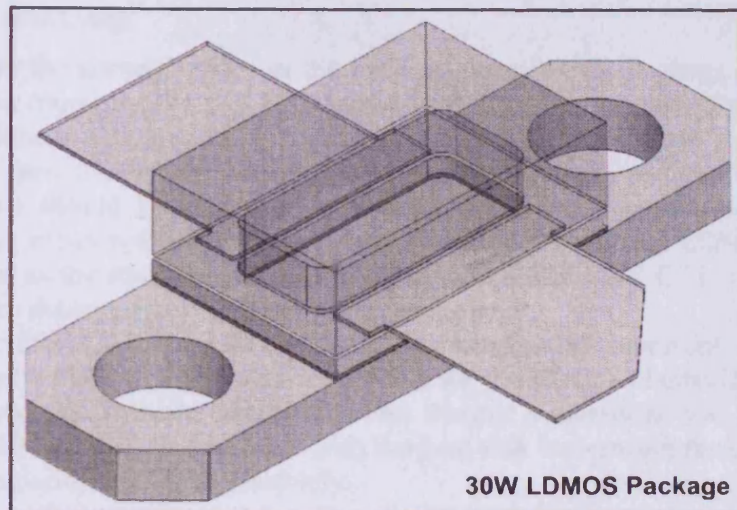


Fig. 1: HFSS Representation for 30 Watt LDMOS Package Structure.

3. EM SIMULATION

For the first evaluation of the novel package, EM simulations have been carried out. To examine the package electrical performance, a small section of the package of Fig.1 has been selected which represents either I/O ports of the package, this package section is shown in Fig.2 below. HFSS simulator was used to simulate the package RF behaviour, the package port response is shown in Fig.2 below,

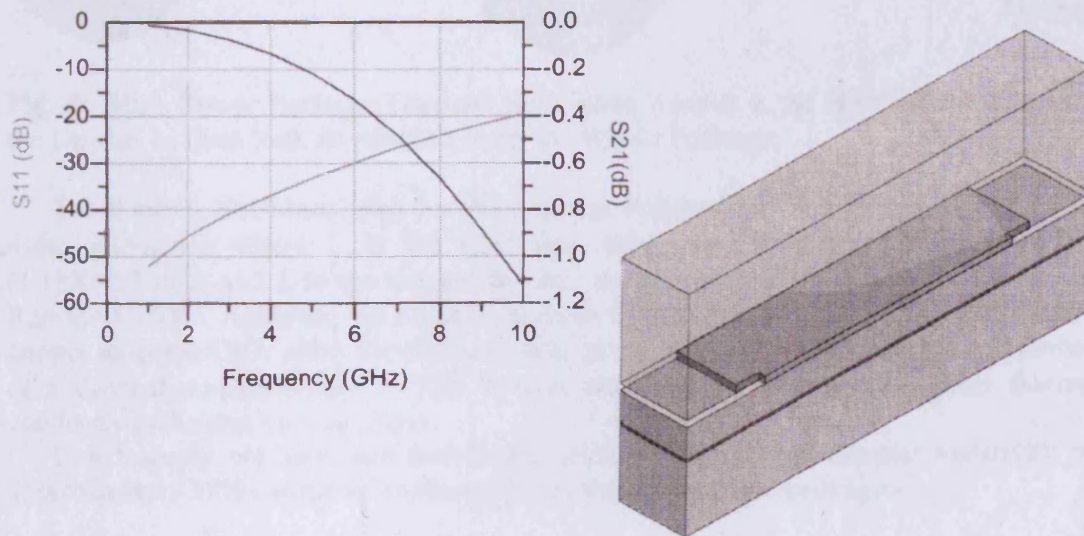


Fig. 2: HFSS Simulation on One Port Package Using RO3003 (635 μm) Laminate.

At 2.1 GHz the package EM simulation shows -45 dB return loss and -0.1 dB insertion loss normalised to 15 Ohm I/O port characteristic impedance, this response makes it a very effective package suitable for the next generation UMTS systems.

To improve the electrical performance beyond 5 GHz different laminate materials and dielectric thicknesses could be used to extend the electrical performance to higher frequency ranges.

4. THERMAL ANALYSIS

To analyze the thermal effect in the package consider the package of Fig.1, where the high power transistor die will be attached to the copper heat sink directly but due to the fact that the die temperature is concentrated on the die top surface therefore some of the heat will flow inside the package including the laminate and the lid. Therefore a good heat sink should be provided underneath the package to dissipate as much as possible of the excessive heat generated by the active device. For LDMOS device 125 C° is specified as the transistor operating temperature while 200 C° is considered to be the limit where the transistor junction will breakdown.

Therefore 200 C° has been chosen for simulation to represent the worse case scenario. The model of Fig.1 was simulated for its thermal behaviour, in order to observe the package thermal capabilities two thermal simulations had been performed one without the heat sink and another with the heat sink underneath the device. Fig.3a ,b shows the simulation results respectively.

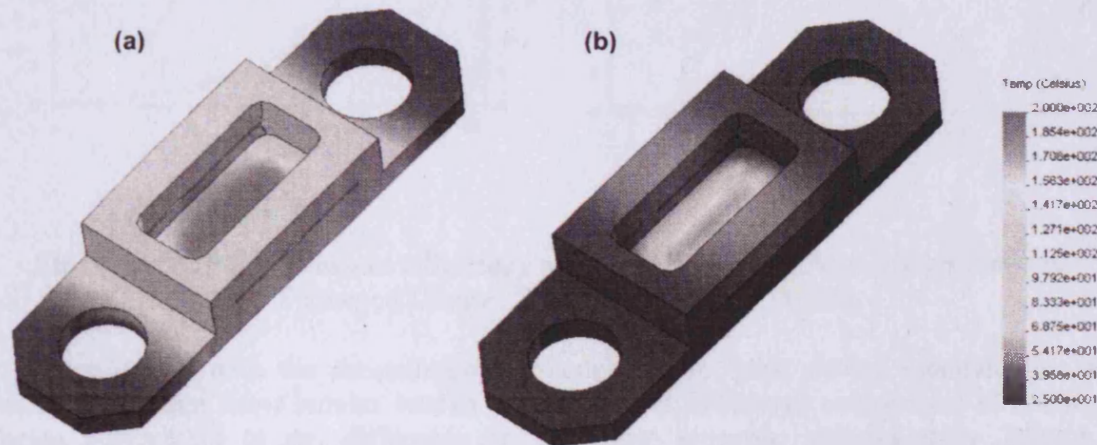


Fig. 3: High Power Package Thermal Simulation Results **a.** no Heat Sink Underneath the Device, **b.** Heat Sink Available Under the Whole Package.

The thermal resistance (R_{th}) for the package copper heat sink can be estimated [3] using $R_{th}=L/A \cdot k$ where L is the heat sink thickness (1 mm), A is the die area (1.15X4.55 mm) and k is the copper thermal conductivity (390 W/m.K), which gives $R_{th}= 0.49$ °C/W. Applying the same formula to a typical ceramic package, which uses a copper tungsten CuW alloy for the heat sink, gives $R_{th}=0.77$ °C/W. For this calculation of a thermal conductivity $k = 250$ W/m.K was used, which is the highest thermal conductivity for this kind of alloys.

Conclusively, the new laminate-based package reduces the thermal resistivity by approximately 35% compared to the currently utilised ceramic packages.

5. MEASUREMENT RESULTS

The package shown in Fig.1 has been manufactured by Labtech Ltd UK using RO3003 laminate and the lid was made of FR4 material, a 30 Watt Philips LDMOS device (PHILIPS ILSG4-4) was then mounted and measured. The transistor was load-pulled [4] at 2.1 GHz under class AB operation with $V_{GS}=3.2V$ and $V_{DS}=20V$.

Following a comprehensive search for the optimum load impedance, it's found to be $Z_{opt}=1.6-j4.7$ Ohm which is very close to the specified manufacturer optimum load (1.31-j3.28 Ohm), hence confirming the good RF performance obtained from the EM

simulations. While maintaining the same optimum load impedance an input power sweep had been performed while measuring the transistor output power, efficiency and gain, the results are shown in Fig.5.a below. The same measurement procedures applied on the same device packaged using Alumina Philips package (Fig. 3.b); the optimum load for this packaged device was found to be $1.479-j4.19$ Ohm.

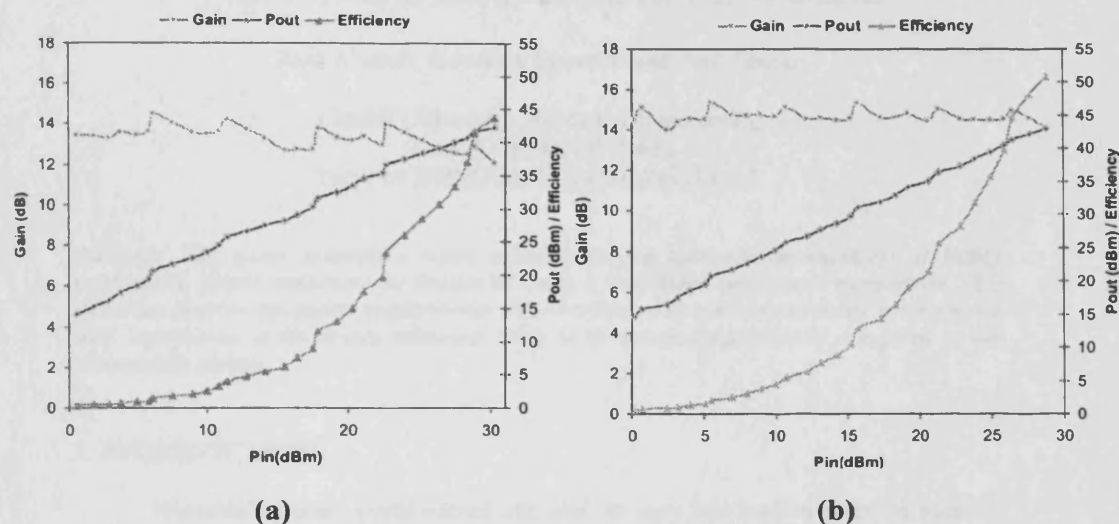


Fig 5. Pin Vs Pout, Gain and Efficiency at $V_{GS}=3.2V$, $V_{DS}=20V$, **a.** Novel Labtech Packaged Device, **b.** Philips Packaged Device.

Comparison with the measurements obtained from same device mounted into a ceramic package show similar results with the small difference in gain and efficiency being attributable to the difference in DC drain currents, approximately 200mA, between the measurements.

6. CONCLUSION

A novel low cost high power package design, simulation and measurement are presented in this paper. The new package offers significant cost savings compared to conventional ceramic models while maintaining an excellent electrical and thermal performance.

ACKNOWLEDGEMENT

The authors of this paper would like to thank Labtech Ltd UK for manufacturing the high power packages.

REFERENCES

- [1] Kyocera Wireless Corporation, "LDMOS Packages High-Power Amplifiers, Push-pull Devices," Product Information Sheet.
- [2] Philips Semiconductor, "SOT540A Package Outline," Ceramic Package Data Sheet, January 2000.
- [3] Young & Freedman, "University Physics," Addison Wesley, ISBN 0-321-20469-7.
- [4] Z. Aboush, J. Lees, J. Benedikt, P. Tasker, "Active Harmonic Load-pull for Characterizing Highly Mismatched High Power Transistors", *IEEE MTT-S Int. Microwave Symp. Digest*, June 2005.

HIGH POWER HARMONIC ACTIVE LOAD-PULL USING BROADBAND IMPEDANCE TRANSFORMERS

Zaid Aboush, Johannes Benedikt and Paul Tasker

Cardiff University, School of Engineering
Cardiff CF24 3TF Wales
Tel: +44 2920879095: AboushZ@cf.ac.uk

Abstract: This paper presents a novel solution for the load-pull measurement of highly mismatched power transistors by means of using a broadband impedance transformer. This technique enables the power requirements of active load-pull systems necessary to synthesize load impedances at the device reference plane to be reduced significantly compared to the mismatched system.

1. INTRODUCTION

Historically, mechanical tuners are used to vary the load in order to identify values for optimum efficiency, linearity, and output power. However these systems suffer a major problem: any losses introduced between the device under test (DUT) and the load-pull system reduce the range of load impedances that can be synthesized especially at highly reflective loads. Active load-pull systems, similar to that proposed by Takayama^[1], avoid this limitation by actively compensating for any losses introduced between the DUT and the load-pull system, therefore any impedance could be set on the smith chart.

A fundamental problem associated with the implementation of the active load-pull systems is that they don't scale well to higher power levels. This is due to the large impedance difference between the optimum impedance required by high power devices (sub 10 Ohms) and the characteristic impedance of the measurement systems (50 Ohms). In order to overcome the above limitations, we propose a solution, which uses a broadband impedance transformer to cover several harmonics present in UMTS systems, which operate at 2.1 GHz. The integration of this transformer into active load-pull measurement systems enables the characterisation of higher power devices, from 30 W up to 100 W devices, into highly reflective loads.

As illustrated in this paper, the impedance transformer can reduce drastically the power levels required from the active load-pull system, furthermore injecting power through the impedance transformer can reduce the risk of damaging the device due to the poor phase control in the high power mismatched system.

2. EXPLANATION OF PROBLEM

To analyze the mismatch problem, it is important to realize that the power delivered into a load depends on three limitations; the maximum power delivered by the load-pull amplifiers, the difference between the device optimum impedance and the characteristic impedance of the measurement system, and the output power rating of the device itself. While performing the load-pull actively on the power transistor, an RF

signal has to be injected from the load-pull source (P_{LP}), at the same time an apparent RF signal is generated by the device (P_{gen}), the ratio of these powers relate to the load-pull reflection coefficient, while the difference determines the power delivered to the load (P_d). This implies

$$P_d = P_{gen} - P_{LP} \quad \text{But,} \quad |\Gamma_{LP}|^2 = \frac{P_{LP}}{P_{gen}}$$

Hence

$$P_{LP} = \frac{P_d |\Gamma_{LP}|^2}{1 - |\Gamma_{LP}|^2} \quad (1)$$

Rearranging

$$|\Gamma_{LP}|^2 = \frac{P_{LP}}{P_d + P_{LP}} \quad (2)$$

In order to visualize the problem, the scenario shown in Fig. 1 has been investigated, in which the device under test is a 20 V(rms) voltage source in series with a 1 Ohm resistor –this is a simple representation of a 100 W transistor with an optimum load impedance of 1 Ohm. The 50 Ohm characteristic impedance of the system, represented by a 50 Ohm line, creates a highly mismatched standing wave.

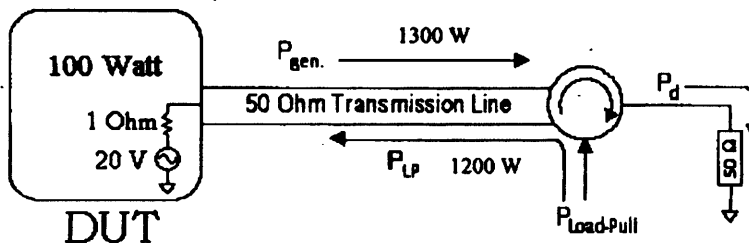


Fig.1 Impedance Mismatch Representation for the Active Load Pull System

This has also been implemented in ADS. The ADS simulation is then used to calculate the active load-pull power required to achieve different reflection coefficient. The simulation results in Fig. 2.a represent the active load-pull requirements (P_{LP}) in the form of constant power contours. (Note: the variation of the power delivered to the load (P_d) as a function of Γ_{LP} is directly taken into account), Fig 2.b illustrates the required load-pull power as a function of the load-pull reflection coefficient along the real axis.

As it can be observed only 2 watts are required to emulate an open (high impedance). However, to present 1 Ohm impedance at the device reference plane the load pull system has to deliver 1200 Watts. Hence the apparent generated power required when delivering 100W power to the load is 1300W. Hence it can be seen that the power requirement on the load pull system in this configuration are significant.

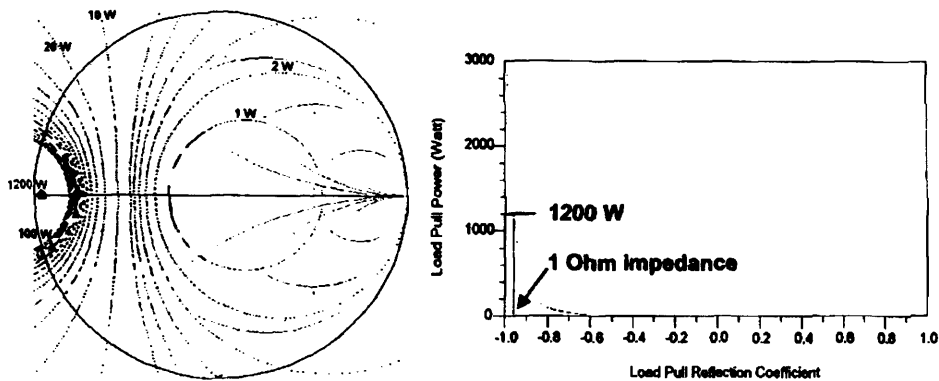


Fig. 2 a. Active Load-Pull Power Requirement Contours for a 100 W, 1 Ohm source in a 50 Ohm Environment, b. Load-Pull Power as a Function of the Load-Pull Reflection Coefficient

3. BROADBAND IMPEDANCE EFFECT

Clearly, the power levels required from an active load-pull within a highly mismatched system can become prohibitive. The solution to this problem is to reduce the impedance difference, which can be achieved either by reducing the impedance environment of the entire measurement system, i.e. using couplers, bias tee, etc. with a non 50 Ohm characteristic impedance, or by inserting impedance transforming network between the DUT and the measurement system. For the first solution (i.e. for a non 50 Ohm system), working with 10 Ohm system would be preferred, however, the design of the couplers, bias tee, etc. to meet the increasing current demands is very challenging. Therefore the utilization of the impedance transformer just before the DUT is more practical.

However, this impedance transformer needs to match the whole bandwidth of the measurement system to allow for calibration (in fact the broadband impedance will provide a resonance free environment which make the calibration possible at the whole bandwidth). TRL calibration could be used to calibrate the system at the device reference plane.

For a 100 Watt rated power device, 1 Ohm optimum load impedance is quite normal. Practically to transform 50 Ohm impedance into 1 Ohm with a good input reflection coefficient, the transformer will then become long and wide, therefore a compromise is necessary. Depending on the application and for the purpose of illustration an ideal 10 to 50 Ohm impedance transformer is introduced in this paper in combination with a 100 Watt, 1 Ohm device.

Again, the layout of Fig. 3 has then been modelled using ADS (the same DUT as in Fig. 1), the simulations revealed a significant improvement in the amount of power required to load-pull this 1 Ohm device. Loci of the required active load-pull power in the form of constant power contours are shown in Fig. 4.

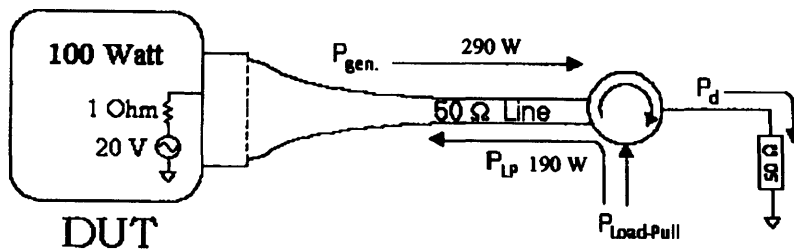


Fig. 3 Impedance Transformation representation for the Active Load-Pull System

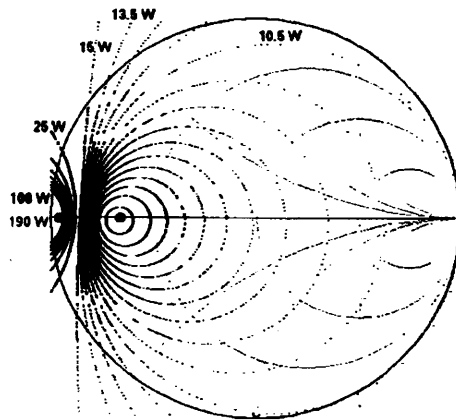


Fig. 4 Load-pull power contours for a 1 Ohm device after using impedance transformer

Notice the impedance transformer has lowered the load-pull power requirement to obtain 1 Ohm load from 1200 Watts to only 190 Watts (i.e. 84% power reduction). On the other hand the load-pull power required to achieve an open (high impedance) has increased from only 2 Watts to 10.5 Watts (which what we expect).

4. BROADBAND IMPEDANCE TRANSFORMER

To realize the experiment practically, Klopfenstein taper impedance transformer which is based on Fourier transform analysis has been designed^[4]. Among the various methods of designing broadband impedance transformer using tapered lines the Klopfenstein taper has shown to have the optimum performance in the sense that for a given taper length it has the minimum magnitude of the input reflection coefficient throughout the pass band, on the other hand for a specified tolerance of reflection coefficient magnitude the taper has the minimum length. The taper final shape is shown in Fig 5 below

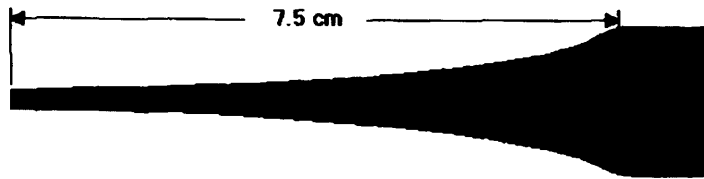


Fig.5 Broadband Impedance Transformer Layout

Putting the matching network into ADS Simulator results in the response shown in Fig. 6. In this case port 1 reference impedance is set to 10 Ω and port 2 reference impedance is set to 50 Ω .

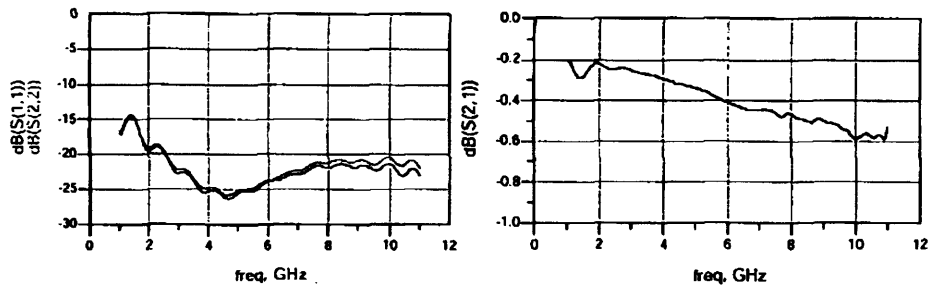


Fig. 6 Broadband Impedance Transformer Response

The transformer has managed to transform 50 to 10 Ohm over a large bandwidth with maximum -15 dB return loss and -0.6 dB insertion loss at 10 GHz. For a lossy transformer like the one shown above, the load-pull power requirements to present a 1 Ohm into the system of Fig.3 will increase slightly from 190 to 199 Watt.

5. SYSTEM DESCRIPTION

Fig. 7 illustrates the block diagram of a measurement system combining time domain waveform measurements and harmonic active load-pull developed over the past few years at Cardiff University^[2], modified to incorporate the impedance transformers. The two channel MTA is used to measure the absolute incident and reflected waveforms on the device input and output ports, the synthesized sweeper is used as a signal generator, while the active load-pull system comprises a set of signal generators at multiple frequencies which could be set using a CAD program. To perform load-pull measurements at high power levels a 200 W power amplifier is used to drive the fundamental path while 20 W power amplifiers are used to drive the harmonic frequencies paths. A high power bias-tee has also been developed at Cardiff University Centre for High Frequency Engineering^[3] Apart from the DUT, the characteristic impedance of the system is 50 Ohm.

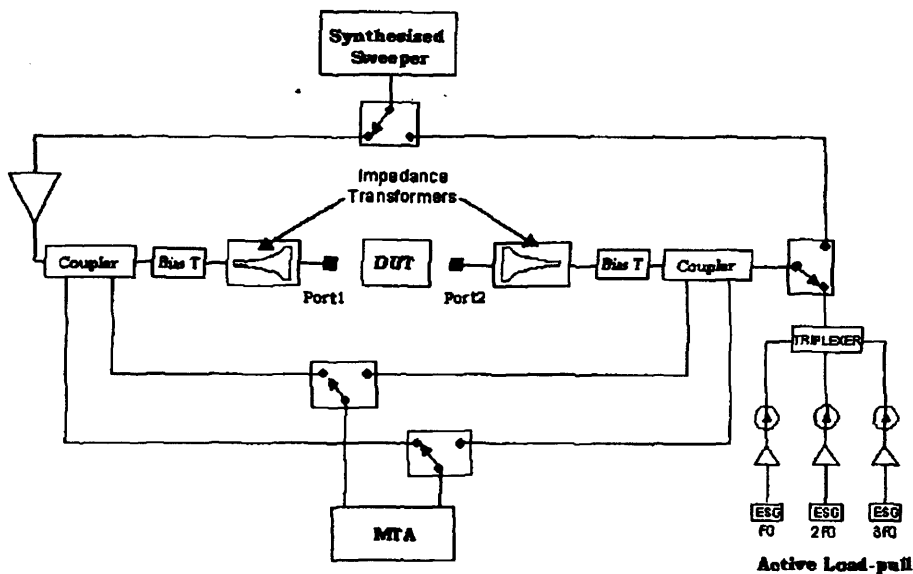


Fig.7 Active Load-Pull Measurement System

6. CONCLUSION

The novel active load-pull system proposed in this paper has shown the ability to reduce the load-pull power requirement significantly; this is due to the broadband impedance transformer. Such a system should be able to synthesize any impedance at any frequency at the DUT plane with an acceptable active load-pull power requirement.

Future work will involve realizing the system practically and doing the necessary measurements.

REFERENCES

- [1] Y. Takayama, "A new load-pull characterization method for microwave power transistors," in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 1967, pp. 218-220.
- [2] J. Benedikt, R. Gaddi and P. J. Tasker, "High power time domain measurement system with active harmonic load-pull for high efficiency base station amplifier design" in *IEEE MTT-S Int. Microwave Symp. Dig.*, June 2000, pp. 1459-1462
- [3] J. Benedikt, P. Tasker, "High power time-domain measurement bench for power amplifier development," *ARFTG Conference Digest*, Fall 2002. 60th, 5-6 Dec. 2002, pp.107-110.
- [4] R. W. Klopfenstein, "A Transmission line taper of improved design," *Proc. IRE*, vol. 44, pp. 31-15, January 1956.
- [5] P. Bouysse, J. Nedus, J. Coupat, and J. Villotte, "A novel accurate load-pull setup allowing the characterization of highly mismatched power transistors," *IEEE Transaction on Microwave Theory and Techniques*, vol. 42 No. 2, February 1994.
- [6] David M. Pozar, "Microwave Engineering," Wiley, ISBN 0-471-17096-8.

Compact, Narrow Bandwidth, Lumped Element Bandstop Resonators

Zaid Aboush and Adrian Porch

Abstract—This letter describes the design and simulation of novel, highly compact, lumped element bandstop resonators. The resonators are fabricated using copper microstrip lines, with resonant frequencies around 5 GHz but with areas of only $1.075 \text{ mm} \times 1.275 \text{ mm}$. Each resonator consists of 8 interdigital capacitive fingers in parallel with a straight line inductor. The new design offers at least a 40% size reduction compared with similar resonators [1], [2]. Furthermore, adjustment of the input and output feed line geometries enables resonator tuning at the design stage over a bandwidth of approximately 100 MHz. The measured characteristics show good agreement with the simulated responses. Ultimate performance of this type of bandstop resonator is achieved using superconducting thin films, and to conclude a 20-finger, superconducting resonator (of area $1 \text{ mm} \times 0.41 \text{ mm}$) is described and simulated.

Index Terms—Bandstop resonators, interdigital capacitance, lumped element devices, superconductivity.

I. INTRODUCTION

MOBILE communication systems have always demanded compact, high performance filters. Due to the large (and thus expensive) bandwidth required by 3G systems, there is an increased need for narrower bandpass and bandstop filters that use the allocated bandwidth more effectively. This letter describes efficient design and measurements of a bandstop resonator using a lumped element circuit with an extremely narrow stopband with very high insertion loss. It is possible to adjust its resonant frequency simply by changing the configuration of the input and output ports. The new structure is based on the design reported in [1], [2] but uses copper instead of superconductor to validate the concepts experimentally; an analogous structure using superconducting materials has been designed and simulated, and this is discussed at the end of the letter.

II. DESIGN AND MODELING OF THE RESONATOR STRUCTURE

Consider the three distributed element, bandstop resonator circuits (A, B, and C) shown in Fig. 1. Circuit A is based on that presented in [1] while circuit B is derived from A but demonstrates that it is possible to obtain almost the same high quality response but at a lower frequency, without having to increase the geometrical size. Finally, C is a new circuit which has superior performance compared to the circuits A and B. A single section of this new resonator circuit C offers a combination of excellent

Manuscript received February 15, 2005; revised April 28, 2005. This work was supported in part by Labtech, Ltd. and Rogers Co. The review of this letter was arranged by Associate Editor J.-G. Ma.

The authors are with the School of Engineering, Cardiff University, Cardiff CF24 0YF, U.K. (e-mail: aboushz@cf.ac.uk; porcha@cf.ac.uk).

Digital Object Identifier 10.1109/LMWC.2005.852793

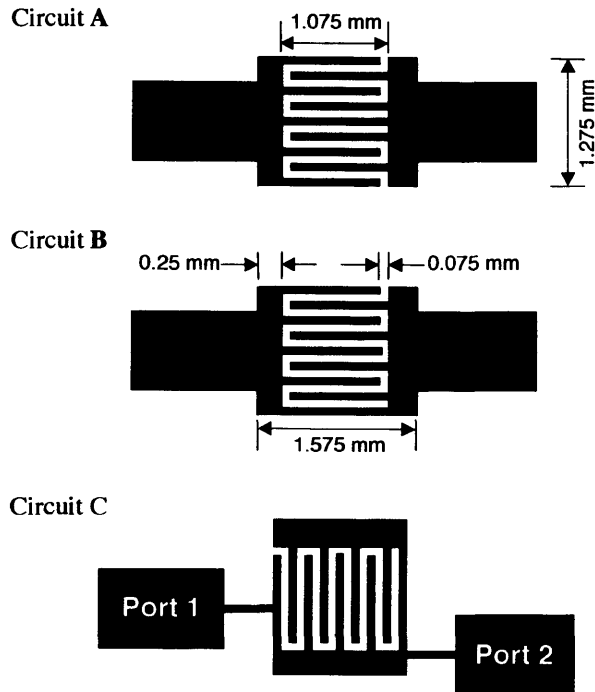


Fig. 1. Schematic layouts of the bandstop resonators (circuit A) proposed in [1], (B) adapted from (A), and the new circuit (C).

response, size reduction and low frequency for a given device area.

Frequency domain simulation using ADS Momentum yields a resonant frequency of circuit A of 10.2 GHz (assuming RT Duroid RO3010 circuit board with a dielectric constant of 10.2, dielectric thickness of $635 \mu\text{m}$ and copper thickness of $35 \mu\text{m}$). By moving the central inductor to the resonator edge and doubling the capacitance (as in circuit B) the simulated resonant frequency decreases to 7.3 GHz.

The new circuit C uses the same geometry as circuit B but with a different configuration of input and output ports. Circuit C can be implemented into a bandstop filter using the layout shown in Fig. 2(a), from which the exact equivalent lumped element circuit of Fig. 2(b) can be deduced. Where L is the edge line inductance [3], C is the capacitance of the interdigital fingers [4], L_1 is the inductance of the short circuit ends of the interdigital fingers [5] and C_1 is the total capacitance to ground.

III. DEVICE FABRICATION, SIMULATION AND MEASUREMENT

The circuits A, B, and C shown in Fig. 1 have been fabricated from RT Duroid RO3010 circuit board specified above using

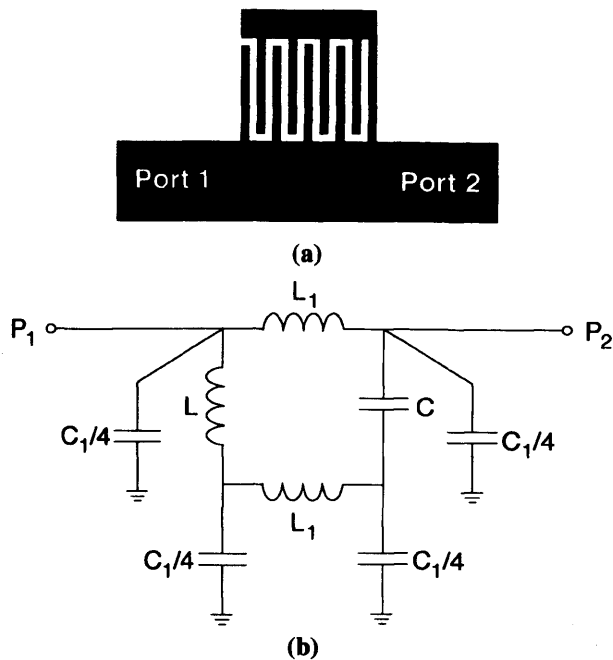


Fig. 2. (a) New resonator configuration. (b) Exact equivalent circuit of circuit C of Fig. 1.

standard photolithography followed by wet etching. These structures have been grounded to a brass block and SMA launchers have been used for the coax-to-microstrip transitions at each port. Measurements of the S parameters were performed in the frequency domain using an HP8510 vector network analyzer. A comparison of the measured insertion losses $IL = -20 \log |S_{21}|$ in the frequency domain for the three circuits A, B and C are shown in Fig. 3(a), with the data for circuit C compared with its simulation (using ADS) in Fig. 3(b). Although the insertion loss for circuit C is not as high as for A and B in its stopband, its bandwidth is much narrower and it suffers little from the asymmetric response observed for the other two circuits. The experimental and simulation results for circuit C agree very well with each other.

In these simulations, the measured dimensions of the feature sizes are used, which differ slightly from those designed owing to slight over-etching of the copper sheets during processing. The resonant frequency of circuit C can be tuned at the design stage by sliding port 1 along the first finger of the interdigital capacitor. Simulation of this shows that up to 100 MHz tuning of the center frequency can be achieved without significant degradation of the bandstop response.

IV. SIMULATION OF A SUPERCONDUCTING CIRCUIT

The performance of the new circuit C, although promising, is limited by the finite surface resistance of the copper used for its conductors. To determine its ultimate performance, consider finally simulations of circuits A, B, and C when the conductors are replaced by 20-finger resonators made of a superconducting thin films. A new simulation using niobium (Nb, transition temperature 9.2K) has been performed. Here the surface impedance [6], [7] is assumed to be $(0.01 + j2.00) \text{ m}\Omega$ at 5 GHz

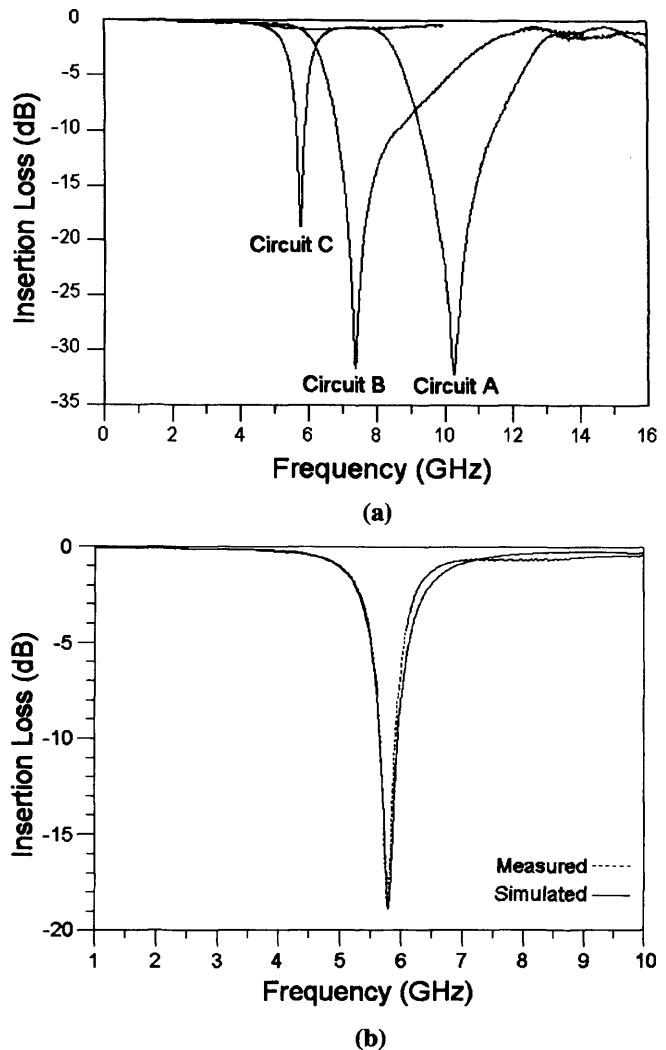


Fig. 3. (a) Measured results for the insertion loss in the frequency domain for circuits A, B and C, and (b) comparison of the ADS simulation and measurement for circuit C.

and 4.2 K, the substrate thickness is $410 \mu\text{m}$ and the dielectric constant is 9.6 (for magnesium oxide or sapphire substrates). The ADS simulator has been used to simulate circuits A, B, and C, where the simulation mesh frequency had been set to 20 GHz and the results are shown in Fig. 4. It can be seen that circuit C offers significant improvements compared with circuits A and B, most notably a stopband rejection in excess of 50 dB and a 3 dB bandwidth of around 90 MHz, making it a very effective bandstop filter.

V. CONCLUSION

In this letter, a new design of bandstop filter has been discussed that improves upon the performance of similar structures reported in the literature. By adjusting the configuration of the input and output ports it is possible to change the centre frequency by up to 100 MHz. The measured and simulated response in the frequency domain of the new circuit agree very well when using copper for the circuit conductors, and an equivalent circuit for the circuit has been developed as a design

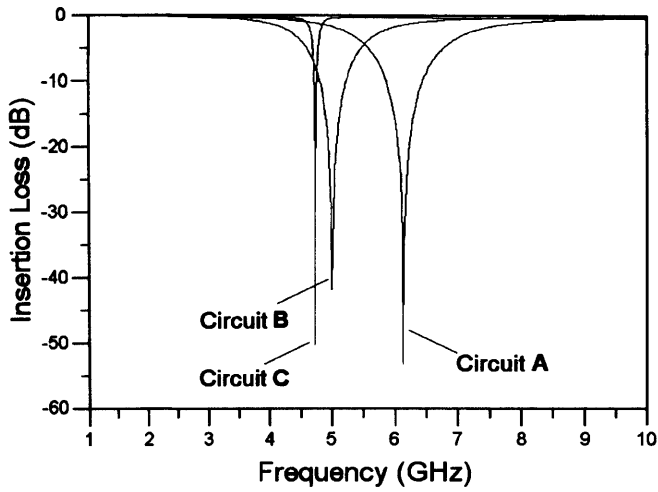


Fig. 4. Simulated response of circuits A, B, and C when using thin films of Nb superconductors.

aid. Ultimate performance is obtained by replacing copper with superconducting thin films, allowing the number of interdigital capacitive fingers to be increased whilst preserving narrow bandwidth, low insertion loss either side of the resonance and high insertion loss at resonance. The simulated results for the new circuit geometry using superconductors demonstrate the effectiveness of the new circuit geometry, and further work is planned that will implement the new design using niobium thin films.

ACKNOWLEDGMENT

The authors wish to thank Prof. M. Lancaster (Birmingham University, U.K.), Dr. P. Mauskopf, C. Dunscomb, Prof. P. Tasker and Dr. J. Benedikt (Cardiff University, U.K.), for their technical advice.

REFERENCES

- [1] M. J. Lancaster, F. Huang, A. Porch, B. Avenhaus, J.-S. Hong, and D. Hung, "Miniature superconducting filters," *IEEE Trans. Microwave Theory Tech.*, vol. 44, no. 7, pp. 1339–1346, Jul. 1996.
- [2] H. T. Su, F. Huang, and M. J. Lancaster, "Highly miniature HTS microwave filters," *IEEE Trans. Applied Supercond.*, vol. 11, no. 1, pp. 349–352, Mar. 2001.
- [3] D. M. Sheen, S. M. Ali, D. E. Oates, R. S. Withers, and J. A. Kong, "Current distribution, resistance, and inductance for superconducting strip transmission lines," *IEEE Trans. Applied Supercond.*, vol. 1, no. 2, pp. 108–115, Jun. 1991.
- [4] G. D. Alley, "Interdigital capacitors and their application to lumped-element microwave integrated circuits," *IEEE Trans. Microwave Theory Tech.*, vol. 18, no. 12, pp. 1028–1033, Dec. 1970.
- [5] F. Huang, B. Avenhaus, and M. J. Lancaster, "Lumped-element switchable superconducting filters," *Proc. Inst. Elect. Eng.*, vol. 146, no. 3, pp. 229–233, Jun. 1999.
- [6] A. Porch, M. J. Lancaster, and R. G. Humphreys, "The coplanar resonator technique for determining the surface impedance of $\text{YBa}_2\text{Cu}_3\text{O}_{7-\delta}$ thin films," *IEEE Trans. Microwave Theory Tech.*, vol. 43, no. 2, pp. 306–314, Feb. 1995.
- [7] M. J. Lancaster, *Passive Microwave Device Applications of High-Temperature Superconductors*. London, U.K.: Cambridge Univ. Press, 1997.

