Development of Novel Design Methodologies for the Efficiency Enhancement of RF Power Amplifiers in Wireless Communications

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Abstract

The research work presented in this thesis sets out to investigate improvements to the power amplifier design cycle through the use of recently developed radio-frequency waveform measurement and characterisation systems. One key objective of this work is to improve the overall efficiency of the modern wireless communication system by focusing on the radio-frequency power amplifier stage. More specifically, the direct utilisation of waveform-engineering techniques in the development of methodologies for the design and realisation of efficiency enhanced radio-frequency power amplifiers was targeted.

In developing these power amplifier design methodologies, work has also led to significant advancements into the possibilities of 'first-pass-design' success. Through the direct import of captured waveform data into a computer-aided design environment, along with efficiency-optimised multi-harmonic and intermediate-frequency impedance information, a stable and highly efficient power amplifier has been realised. This direct implementation of waveform measurements completely by-passes any involvement with potentially unreliable nonlinear device models. Hence this has eliminated the need for multiple iterations of matching networks, resulting in a dramatically more time-efficient design process.

Waveform-engineering-based designs completed in this research have been demonstrated with both very high-efficiency (70-80%), narrowband modes of operation, as well as a high-efficiency (60-70%) broadband mode covering almost an octave bandwidth. All designs throughout have been realised as prototype power amplifiers.

Key Contributions

Contribution 1: Development of a novel power amplifier design methodology for achieving record high (up to 84%) efficient modes of device operation in a packaged gallium nitride power transistor.

Contribution 2: Right-first-time realisation of very high-efficiency power amplifier prototypes from direct import and utilisation of optimised waveform measurement data in a computer-aided design environment.

Contribution 3: Novel investigation, experimentation and practical demonstration of the class-J mode of power amplifier for achieving high-efficiency device operation across more than 50% relative bandwidth.

Contribution 4: Overall, furthered research by providing investigations and results which continue to validate 'waveform-engineering' as a useable technique for designing and realising performance-optimised radio-frequency power amplifiers for wireless communications.

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List of Publications

First-Author Conference Papers:

1. P. Wright, J. Lees, P. J. Tasker and J. Benedikt, "GaN Power Transistors in Narrow and Wide Bandwidth Applications", 2008 IET Wideband Receivers & Components Conference, London, UK, May 2008.

2. P. Wright, C. Roff, T. Williams, J. Lees, J. Benedikt, and P. J. Tasker, "RF Power Amplifier Design for High Efficiency Applications", 2008 SPIE Europe: Security & Defence Conference, Cardiff, UK, September 2008.

3. P. Wright, A. Sheikh, C. Roff, P. J. Tasker, J. Benedikt, "Highly efficient operation modes in GaN power transistors delivering upwards of 81% efficiency and 12W output power," IEEE MTT-S 2008 International Microwave Symposium Digest, pp. 1147-1150, Atlanta, GA, USA, 14-19 June 2008.

4. P. Wright, J. Lees, P. J. Tasker, J. Benedikt, S. C. Cripps, "An Efficient, linear, broadband class-J-mode PA realised using waveform engineering," IEEE MTT-S 2009 International Microwave Symposium Digest, pp. 653-656, Boston, MA, USA, 7-12 June 2009.

First-Author Transactions Paper:

1. P. Wright, J. Lees, P. J. Tasker, J. Benedikt, S. C. Cripps, "A Methodology for Realizing High Efficiency Class-J in a Linear and Broadband PA," IEEE Transactions on Microwave Theory and Techniques, Volume 57, Issue 12, pp. 3196-3204, December 2009.

Other Papers:

1. S. Bensmida, K. Morris, J. Lees, P. Wright, J. Benedikt, P. J. Tasker, M. Beach, J. McGeehan, "Power Amplifier Memory-Less Pre-Distortion for 3GPP LTE Application", IEEE European Microwave Conference, pp. 1433-1436, 29 September-1 October 2009.

2. A. Al-Muhaisen, P. Wright, J. Lees, P. J. Tasker, S. C. Cripps, J. Benedikt, "Novel Wide Band High-Efficiency Active Harmonic Injection Power Amplifier Concept," IEEE MTT-S 2010 International Microwave Symposium Digest, pp. 664-667, Anaheim, CA, USA, May 2010.

Other Achievements During PhD Course:

1. Runner-up in the IEEE MTT-5 Student High Efficiency Power Amplifier Design Competition at the International Microwave Symposium 2008, Atlanta, GA, USA. - Measured PAE of 73.01%.

2. Winner of the IEEE MTT-S Student Paper Competition at the International Microwave Symposium 2009, Boston, MA, USA, for paper entitled: "An efficient, linear, broadband class-J-mode PA realised using waveform engineering."

List of Symbols and Abbreviations

A, mA – Amperes, milli-Amperes

ACP – Adjacent Channel Power

ACPR – Adjacent Channel Power Rejection

ADS – Advanced Design System

AM – Amplitude Modulation

AM-PM – Amplitude-Modulation-to-Phase-Modulation

Avg. Eff./Pout – Average Efficiency/Output Power

BER – Bit Error Rate

C – Capacitance

c – Speed of Light in a Vacuum

CAD – Computer-Aided Design

CF – Centre Frequency

Class-F^{-1} – Inverse Class-F

CW – Continuous Wave

d – Dielectric Thickness

dB – Decibels

dBc – Decibels (reference to carrier power)

dBm – Decibels (reference to 1mW)

DC – Direct Current

DUT – Device-Under-Test

ECM – Environment Climate Monitoring

E_g – Energy Gap

eV – Electron Volts

EVM – Environment Climate Monitoring

F, pF – Farads, pico-Farads

FET – Field Effect Transistor

Freq., *f* – Frequency

GaAs – Gallium Arsenide

GaN – Gallium Nitride

H, mH – Henrys, milli-Henrys

Hz, GHz – Hertz, Giga-Hertz

I, *i* – Current

I_{dq} – Quiescent Drain Current

I_{dss} – Saturation Drain-Source Current

I_{gen}-Plane – Current-Generator Plane

IM – Inter-modulation

j – Denotes the imaginary component of a complex impedance

k_0 – Wave Number

L – Inductance

LDMOS – Laterally Diffused Metal Oxide Semi-conductor

LP – Load-Pull

m, μm – metres, micro-metres

MAG – Maximum Available Gain

NL - Nonlinear

P – Power

P1dB – Output power at 1dB gain compression

PA – Power Amplifier

PAE – Power-Added Efficiency

PAR – Peak-to-Average Ratio

pHEMT, HEMT – Pseudomorphic High Electron Mobility Transistor

PUF – Power Utilisation Factor

R – Resistance

RF – Radio Frequency

S-parameters – Scattering Parameters

Si – Silicon

SiC – Silicon Carbide

TMM® - Thermoset Microwave Laminates

TRL – Thru, Reflect, Line

UAV – Unmanned Aerial Vehicle

V, *v* – Voltage/Volts

VNA – Vector Network Analyser

W – Transmission-line Width

W, mW – Watts, milli-Watts

WCDMA – Wideband Code Division Multiple Access

X – Reactance

Z – Impedance

ε_r – Relative Dielectric Constant

ε_e – Effective Dielectric Constant

η – Efficiency

Ø - Electrical Length

Γ, ρ – Reflection Coefficient

Ω – Ohms

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Chapter 1. Introduction

1.1 RF Power Amplifiers for Wireless Communications

With worldwide mobile communications subscribers ever on the increase, and ongoing advancements in communications services available to these users, the drive for improving the overall efficiency of the modern-day wireless communication system has never been greater. Such industry motivations for power-efficient or 'greener' systems include the demand for increased functionality of mobile handset devices. This directly leads to higher communication data rate requirements (Fig. 1.1) and all whilst maintaining a practical battery life expectancy within the wireless handset. The relatively recent introduction of 'smart-phones' and commercial 3G (3rd generation) networks has enabled users to now access broadband internet and basic streaming services whilst on the move - but ultimately at a high financial cost to the network provider and, hence, end subscriber.

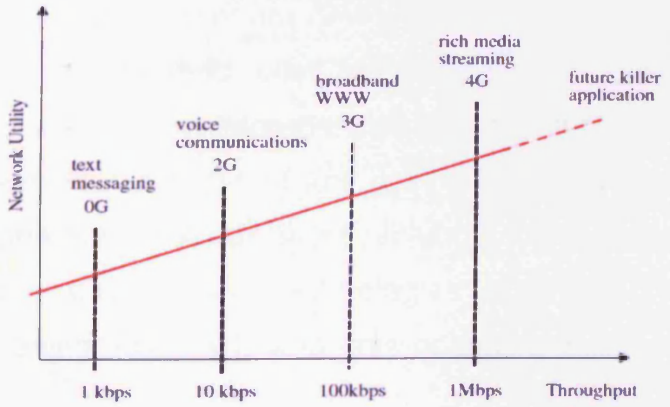

Fig. 1.1. Network utility to the user versus the achievable data throughput [1].

Drivers for improved power-efficiency not only come from the mobile handset market, but also from the network provider infrastructures, where the base-station costs are responsible for a very high percentage of the overall communication system cost as a whole. Military communications are also prone to size, weight and portability issues with the added stringent reliability requirements having to be met, above those of commercial handsets.

Ultimately, therefore, it is the power-hungry RFPA (radio-frequency power amplifier) stage which determines the major considerations in terms of efficiency; Whether this be driven by the required portability of mobile wireless handsets containing lower-power amplifiers, the necessity for highly reliable and durable military front-line communications, or the cost of cooling requirements for the very-high-power amplifiers present in fixed base-stations. It is this RFPA (or PA) stage that potentially holds the most gains for efficiency enhancement of the modern wireless communications system.

1.2 Research Objective - Novel Development Cycle Methodologies for Efficiency Enhancement of RFPAs

In the age of CAD (computer-aided design) environments, the process of PA design has become potentially much more time-efficient. As a part of this computer-aided design process, nonlinear device models for use in the simulation environment are now widely implemented in PA designs [2-3]. However this method relies very heavily on the accuracy of the device models used. Any discrepancies present in the more-difficult-to-model nonlinear characteristic of any device lead to the inherently time-consuming stage of the PA designers project of multiple design iterations. With new generation device technologies emerging continuously, a means of removing this costly and time-consuming stage of PA design

would be a welcome development. On many occasions the requirement for highly accurate device models for these corresponding new transistor technologies is not met.

In the majority of RF transmitters the PA usually operates well below a 50% conversion of DC (direct current) to RF power [4]. The total system efficiency will be further reduced by dealing with the DC power not converted to RF power, but dissipated as heat. This situation persists despite the large number of known PA architectures - as discussed by Cripps, Rhodes, Raab, Grebennikov [4-9] - capable of significantly higher average efficiencies. However, these enhanced PA modes of operation rely on an intricate interaction between the fundamental output power and harmonic loading making their design challenging as no design solutions currently exist that allow for this fully. Hence, despite the large number of mathematical descriptions for various highly efficient PA modes, the interesting practical implementations and observations are not being investigated due to the limited availability of waveform capture and combined load-pull measurement systems.

There is a direct need for device waveforms in order to establish procedures for designing and analysing complex PA modes. This therefore includes the need for multi-harmonic (hence, broadband) measurement capability in order to look at device interaction through the use of dynamic load-lines.

Nonlinear measurement solutions are now becoming more prevalent in the PA design industry [10-13]. Thus the availability of measured waveform data and waveform-shaping or 'engineering' techniques will also increase. The result of this trend will likely see a shift in nonlinear PA design techniques, towards systematic waveform-engineering. In order for these measurement systems to be leveraged to their full

potential for PA design, a thorough understanding of the procedures involved in 'tuning' for high-efficiency in a nonlinear measurement system will be necessary.

In response to this need, systematic procedures for developing working, high-efficiency PAs using waveform-engineering principles are investigated in this thesis. This research describes investigations set out to find solutions to the PA development cycle issues. Using a high power active load-pull waveform measurement system [10], for characterisation of high power packaged transistor devices, PA topologies can be accurately and precisely measured on actual device samples through engineering the output waveforms. A review of literature, in **Chapter 2**, specific to this area focuses on a very-high-efficiency class-F amplifier topology that has previously been emulated[1] with on-wafer devices using waveform-engineering design techniques [14]. However, we are yet to see any waveform-engineered designs be followed through and translated directly to a realised amplifier. It is therefore the aim of this research to investigate novel design methodologies for efficiency enhanced high-power amplifiers using waveform-engineering techniques on packaged transistors. To make use of the captured data during the design of suitable matching networks, and develop working PA prototypes for application in the RF industry, is the next major objective.

1.3 Current PA Design Approaches Used in Industry

PA design processes take several forms with particular techniques adopted for each individual design specification and requirement. In modern RF communication PA design there has been an increased interest in high-efficiency mode approaches. This re-evaluation has

[1] The term "***emulated***" has been used here, and will be throughout this thesis, to describe the use of active load-pull to present specific reflection coefficients to the DUT (device-under-test) in initiating a particular mode of operation in the DUT, without the use of passive matching.

become possible as additional circuit techniques such as digital pre-distortion and drain modulation have evolved which can be wrapped around PAs operating in these modes to enhance linearity and power back-off performance [4].

Such high-efficiency-mode PAs are commonly classified by the shape of their current and voltage waveforms [4] and denoted as 'complex' modes of operation, often requiring multi-harmonic impedance matching to obtain optimum performance levels. When designing in CAD, the additional harmonic impedance requirements add a further dimension to the level of required accuracy of the designers' device model. A design process, to allow for the rapid optimisation of multi-harmonic impedances in complex modes of RFPAs, requires a systematic strategy in order to overcome further time-consuming multi-iterative PA design.

Taking the design specification of efficiency as an example, the maximum efficiency performance of an active device in a given mode will only occur if the designed circuitry engineers the most efficient output current and voltage waveforms. Therefore, in order to best design for these modes it is highly advantageous to have access to the current and voltage waveforms at the active device terminals. So too the capability to relate circuit parameters to these engineered waveform shapes. This is where the simulation with device models in CAD falls down, and where waveform-engineering practices can hold their advantages.

1.4 Waveform-Engineering on Power Transistors for the Development of High-Efficiency PA Design Methodologies

RF waveform measurement and active load-pull systems previously described in [10-13] have been developed with the objective of being able

to accurately characterise transistor device samples in a variety of impedance environments, input drive and bias conditions. Since real samples of semiconductor wafers or packaged power transistors are characterised, one of the main attractions of these systems is the ability to obtain a true measure of performance from the active DUT (device-under-test) when it is set in the environment for which it is intended for a particular application.

This research has made use of high power waveform measurements and active multi-harmonic load-pull to obtain and analyse RF current and voltage waveforms[2] from the DUT. This gives the designer the ability to 'see' how the device RF characteristics interact with the 'hard' or physical device current-voltage boundaries (DC I-Vs). More importantly, however, this waveform capture enables a powerful means of analysis and device performance manipulation, known as 'waveform-engineering' [15]. This concept is of key importance, underlying the research throughout this thesis by providing the unifying link between fundamental circuit theory, PA prototyping and final performance testing and verification [15].

Using a waveform-engineering design approach, the aim of this research was to investigate how parameters such as bandwidth, linearity, efficiency and power can all be compromised or traded-off in a single design according to the design requirement of the PA. In doing this it has been possible to make advancements in developing methodologies that have resulted in the efficiency optimisation and enhancement of RFPAs. Scalability of these design procedures in terms of frequency and drain voltage bias settings has also been shown.

Much of this research focuses on the use of packaged power

[2] From now onwards, the plural use of the word "***waveforms***" alone in this thesis directly corresponds to the DUT ***current and/or voltage waveforms*** that are captured using the measurement system.

transistors, posing the question over the usefulness of the captured RF waveforms compared with the actual device performance occurring at the intrinsic device plane or 'current-generator plane' ($I_{gen.}$-plane). In these cases the use of parasitic de-embedding has been stated and described [16] and has led to genuine comparisons with, and verifications of, the investigated PA mode theory. This has proved crucial when considering further in-depth analysis and investigation into complex PA modes.

Several prototype PAs have been realised from this research with first-pass-success demonstrated, clearly illustrating an advantage of waveform-engineering design processes for PA design. PA designs developed using the high power waveform measurement system have been followed through to realised PA prototypes for the first time, whilst displaying closely comparable performance to that initially emulated. As a means of obtaining near theoretical-optimum performance from devices, whilst considering the importance of "Watts-per-Dollar", clear improvements, above those previously presented, have been shown when applying the rapid design cycles developed in this research. For the purpose of interest, comparisons with the performance achieved with nonlinear models in CAD are also continuously made.

1.5 Broadband Waveform Measurements for Performance Verification

Research into enhanced-efficiency PA design methodologies demands, by definition, the requirement for broadband frequency consideration. This is due to the requirements for harmonic content information within the DUT's output waveforms which needs to be engineered appropriately in order to limit the overlap in the output current and voltage waves, and thus limit the dissipated DC power [5, 14, 17]. In this research broadband measurement capability has enabled the development of a very-high-

efficiency class-F^{-1} (inverse class-F) PA design methodology. Whilst this procedure employed three-harmonic load tuning, many more higher harmonics were able to be measured and analysed. This in fact has facilitated the suggested reasoning behind why a comparable three-harmonically optimised class-F PA design was less efficient.

Continuing this theme, the methodologies discussed previously were adapted for the development of a novel methodology for designing a class-J-mode PA [4, 6]. Broadband measurement capability has provided a means of not only developing the efficient and broadband PA design but also for testing of the built prototype amplifier. This in itself enables a means of performance verification and comparison with the class-J theory from which the initial design stemmed from.

The above are just two examples illustrating the benefit of broadband waveform measurement capability. Its novel use and crucial role, combined with the active multi-harmonic load-pull implemented throughout the research presented in this thesis, has demonstrated a means of furthering the PA development cycle.

1.6 Device Technology Potential Applied to PA Design

Choosing a device technology for its suitability to a particular application is a vital part of any PA design and design methodology. Previous works have demonstrated the performance degradation observed when a device with relatively low breakdown voltage rating was applied to a PA design with inherent high voltage peaking [18]. The root cause of the result in [18] could be clearly seen when the DUT output waveforms were observed, indicated by an increase in current during the peak in the output voltage waveform cycle. Following on from this result, the importance of selecting an appropriate device technology is

considered, and using waveform measurements this can be done more intuitively. Not only is this an important consideration in terms of device reliability, but when considering the Watts-per-Dollar criteria once again the importance of achieving a worthwhile return from devices is of paramount interest to the designer.

GaN (gallium nitride) transistor technology is used for the majority of the research presented in this thesis; a wide band-gap semiconductor technology enabling very high peak output voltage swings, and thus potentially high power and efficiencies, to be achieved [19]. Such an application of GaN is presented in **Chapter 3**, where a novel class-F^{-1} design methodology based on a waveform-engineering approach has yielded not only a highly efficient PA, but one which also has a good output 'power-utilisation factor' (PUF) [4].

1.7 Objectives and Thesis Synopsis

This thesis is divided into three main sections. The first describes the development of a PA design methodology implementing waveform-engineering for the specification of optimised, very highly efficient device operation. The next main section sees the implementation of the captured waveform measurement data from an emulated PA design, into a CAD environment for the realisation of matching network structures and an overall PA prototype. The third main section investigates a novel broadband PA design in which good efficiency, linearity and output power are also key specifications. This final main section draws on the all aspects of the research presented in the previous sections.

To summarise, **Chapter 2** presents a literature review of current-day, and most recent advancements in, PA design procedures. As a case study, a low-power, on-wafer class-F design in [14] is introduced and its

applicability to higher power packaged transistors also discussed. This chapter also describes in more detail the process of waveform-engineering, the applicability of GaN to high power RF amplifiers, and begins to formulate ideas for class-F^{-1} and class-J mode PA development by introducing these modes of operation as discussed in the literature.

Chapter 3 begins the first main section of this research and presents a PA design methodology for achieving very high-efficiency device operation in a 10W GaN HEMT (high electron mobility transistor). The waveform-engineering-based procedure is explained and demonstrated at two fundamental frequencies; 0.9GHz and 2.1GHz. Verification of the obtained optimised performance is also detailed through the use of RF waveform analysis and comparisons to theoretically predicted figures. Stability analysis considerations are also presented in this chapter.

In **Chapter 4**, realisation of the PA prototype is initiated, making use of the measured waveform data obtained in Chapter 3 for import into a CAD environment. Here, direct use of the optimised performance results are implemented in the design of suitable input and output multi-harmonic matching networks in the form of microstrip layouts, enabling a right-first-time PA prototype to be realised. Comparison of the PA performance with the emulated design, and also nonlinear device model simulations, verify the first-pass-success that has been achieved here.

The third main part of this research begins in **Chapter 5**, and introduces the concept of the class-J mode of power amplifier and investigates its potential for broadband high-efficiency, whilst also maintaining good levels of linearity and output power. This developed design methodology is once again centred about the implementation of a high power waveform measurement system and active load-pull capability, and investigates the best level of efficiency achievable across

a 'significant' bandwidth (i.e. more than a 50% relative bandwidth). The class-J mode's suitability for this application is discussed. Drawing on extensive theoretical analysis of class-J, this chapter presents two prototype broadband PAs which have been realised around a GaN device.

Chapter 6 describes the conclusions from this research and poses questions for discussion, while **Chapter 7** introduces potential future work which could see further improvements to the PA development cycle as an extension to the work in this thesis.

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Chapter 2. Literature Review

2.1 Introduction

This review chapter presents a look at the currently utilised and most recent advancements in PA design procedures. A description of the process of waveform-engineering, the applicability of GaN in developing high-power RF amplifiers, and the formulation of ideas for class-F^{-1} and class-J mode PA development following introduction of these modes of operation are discussed from the literature.

As highlighted in **Chapter 1** - and to be further revealed in detail within this chapter - there is a direct need for RF waveforms in order to establish procedures for designing and analysing complex PA modes. A wide-frequency measurement capability is thus in the forefront of requirements in order to look at DUT RF-dynamics/DC-boundary interactions in these complex modes. Such a measurement system is identified in this chapter, while a case-study covering a low-power, on-wafer class-F design procedure (making use of active load-pull and waveform-engineering techniques synonymous with the aforementioned measurement set-up) is also detailed.

The aim of the research described in this thesis is to respond to the revealed need for systematic design procedures for high-efficiency, high-power amplifiers using RF waveform-engineering-based principles.

2.2 Existing PA Design and Realisation Methods and Associated Design Cycle Problems

2.2.1 Basic Passive Matching Network Design Principles

A standardisation for the impedance of most RF and microwave system equipment and apparatus was introduced in the 1930s when the development of microwave coaxial cables required a suitable trade-off between the power-carrying capability and the contributable losses of the resulting coaxial line [1]. It is therefore paramount that every stage in a modern 50Ω (Ohm)-standardised RF communications system closely follows and matches this standard characteristic impedance in order for RF power transfer from one stage to the next to be completed as efficiently as possible. This inevitably includes the power amplifier stage which, for example, occurs prior to the antenna stage where the wireless transmission of the RF signal takes place.

Several components however - such as the active device(s) in the PA stage - cannot necessarily meet this port impedance requirement directly as a result of their fabrication processes. It is thus the job of the PA designer in this situation to fabricate the necessary passive matching networks around the active device(s) in order to facilitate the efficient transfer of RF power from and to the preceding and subsequent stages respectively. This despite any present mismatch in port impedances between the DUT input/output impedance and the 50Ω standard.

Fig. 2.1 shows a simple example of the requirement for matching in order to facilitate the maximum transfer of power (Eq. 2.1 [2]) between a source impedance (Z_s) of 10+j25Ω and a characteristic port impedance (Z_o) of 50Ω. The 'j' term denotes the imaginary component of the complex impedance.

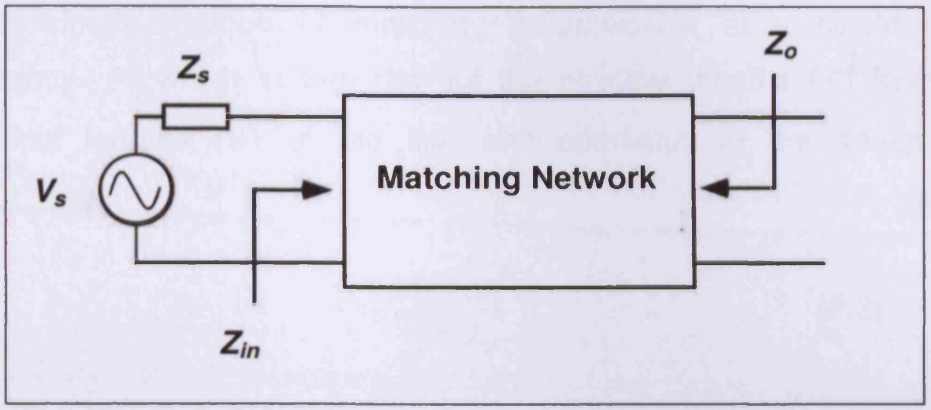

Fig. 2.1. Introducing a matching network to facilitate maximum power transfer between the mismatched source and 50Ω port impedances.

Maximum power transferred [2]:

$$P_{\max} = \frac{1}{2}.|V_s|^2.\frac{1}{4.\Re(Z_s)} \text{ when; } Z_{in} = Z_s^* \qquad (2.1)$$

The implementation of a simple open-stub microstrip transmission-line matching network, to meet the requirement of the mismatched source and 50Ω port impedance, is shown in Fig. 2.2. This was achieved using the Smith-Chart matching tool available in Agilent's ADS (Advanced Design System) simulation environment.

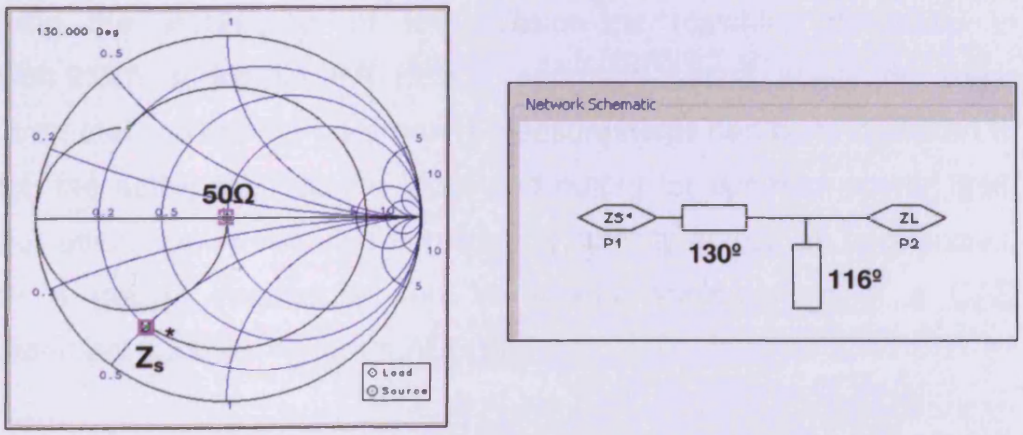

Fig. 2.2. Open-stub microstrip matching (facilitated by Agilent's ADS Smith Chart tool) providing maximum power transfer between source and 50Ω port example.

This simple method of matching is applicable at a single spot-frequency (f) which in turn defines the physical lengths (ℓ) from the electrical lengths (ϕ) of the line and open-stub in the design, by Eq. (2.2) [2]:

$$\ell = \frac{\phi.(\pi/180)}{\sqrt{\varepsilon_e}.k_0} \qquad (2.2)$$

where the effective dielectric constant (ε_e) for a microstrip line is usefully approximated by Eq. (2.3), when the relationship between the microstrip line width (W) and substrate thickness (d) is within the limit $W/d \geq 1$;

$$\varepsilon_e = \frac{\varepsilon_r + 1}{2} + \frac{\varepsilon_r - 1}{2}.\frac{1}{\sqrt{1+12d/W}} \qquad (2.3)$$

and where the wave number is given by Eq. (2.4);

$$k_0 = \frac{2\pi.f}{c} \qquad (2.4)$$

2.2.2 PA Design Based Around S-Parameter Measurements for the Active Device

Using the techniques of transmission-line matching described in section 2.2.1, a simple PA design approach based solely on linear S-parameter (scattering-parameter) measurements can be undertaken to match the active DUT at the input and output for optimum power, gain and/or efficiency, whilst also considering stability across all frequencies. Such a design procedure can be rapidly implemented in a CAD environment such as Agilent's ADS [3].

Figs. 2.3 and 2.4 show a couple of the stages of this type of design process; the simulation circuit layout and the data display providing a means of stability analysis and indicating matching impedance

requirements. The matching tool shown previously in Fig. 2.2 can then be implemented to complete the PA design.

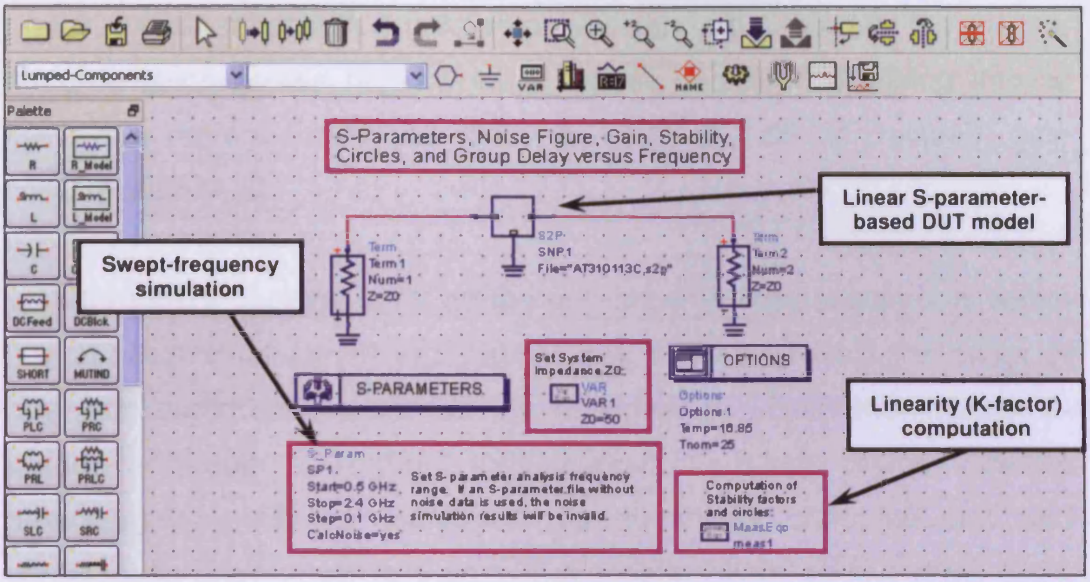

Fig. 2.3. ADS design schematic for an example PA design simulation based around a linear S-parameter device model [3].

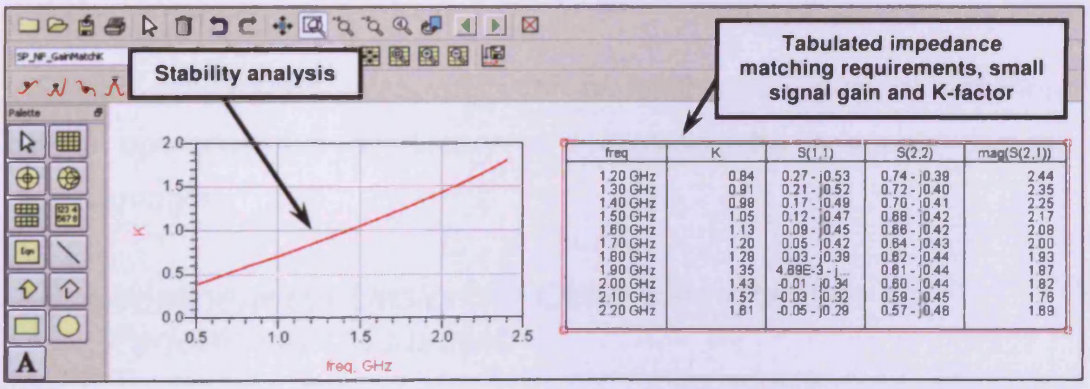

Fig. 2.4. ADS data display reveals the requirements for stabilisation of the device model, the small-signal gain and DUT input and output impedances.

The major and obvious disadvantage of using a linear model for the DUT is the limited accuracy and thus applicability of such a PA design across any significant dynamic range, particularly approaching large-signal operation. This remains the case even if the small-signal S-parameters of the active DUT used in the design simulations have been previously measured on a real device using a VNA (vector network

analyser). In a business where the cost-efficacy - or Watts-per-Dollar - criteria is just as much of a concern to the PA designer as output power, linearity and efficiency, it is common to see practical implementations of a power amplifier design methodology which will consider the device characteristics across high dynamic ranges of power, including into its nonlinear region up to at least a level of 1dB (1 Decibel) gain compression [4-5].

This renders designs such as the one shown here useable only within the device's small-signal application, well backed-off from the onset of any gain compression and device nonlinearity. Even then, linear S-parameter-based designs implemented around some device technologies, such as GaN with its commonly observed soft and continuously compressing gain characteristic, even at low drive [6-7], would result in discrepancies in the realised PA performance compared to the simulated design.

Design procedures accounting for at least some level of nonlinear device operation are necessary in overcoming these simple designs disadvantages.

2.2.3 Nonlinear PA Design for Optimising Absolute Performance Measures

The majority of wireless communications require the PA block as a whole to perform linear amplification of incident signals. However additional sub-sections to the PA block in the form of pre-distortion [8-9], combined with the 'acceptance' for "some" level of PA nonlinearity during signal amplification [10-11], has seen PA designers move more and more towards developing PAs intended to operate further into the nonlinear regions of the devices' transfer characteristics. This can lead to greater

cost-efficacy of the active devices by driving towards increased output power, with the intention of applying linearity enhancement techniques (such as in [8-9]) following the completion of the PA design.

Measurement set-ups, such as the one presented in [12] and represented in Fig. 2.5 as a block diagram (implementing passive load tuners [13]), enable investigations into, and the characterisation of, nonlinear power transistor devices intended for the development of high power amplifier designs. In this case the DUT can be characterised through the measurement of incident and reflected waves from both the device input and output, whilst absolute power can be directly recorded through power meter measurements, as indicated in Fig. 2.5.

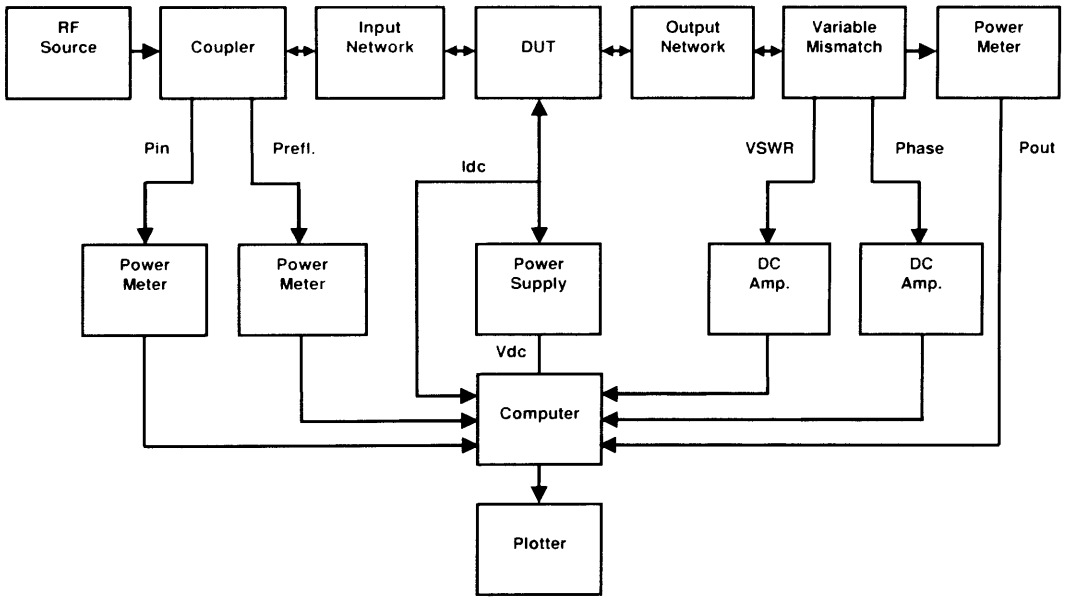

Fig. 2.5. Schematic set-up for measuring absolute power and input/output reflection coefficients of the DUT, with additional passive load-tuning capability [12-13].

This kind of measurement and characterisation set-up enables measurement plots such as load-pull contours, dynamic power sweeps and the location of local optima input and output impedances; all of which can lead to the design of suitable input and output PA matching networks, resulting in optimised PA designs as presented in [14-17].

However, many published PA results claiming specific modes of operation having been achieved - most notably when investigating high-efficiency PA designs [16-18] - are done so at quite a high level of discretion and approximation. The system design framework shown in Fig. 2.5 allows for accurate measurements of power at the fundamental signal frequency. However there is naturally a lack of separation between any harmonic signal components, and thus makes any detailed analysis when considering modulated stimuli impossible. This 'missing' information is frequently obtained through additional separate measurements such as harmonic spectra, but difficulties arise when trying to relate the separate measurements back together due to a missing time or phase reference. When trying to investigate complex modes of PA operation with such a system as in Fig. 2.5 it is impossible to identify when and where the DC power supplied to the DUT has been transformed into the fundamental or harmonic power. As a result of these factors, any focus on the development of energy-efficient RF systems will be based on numerous build and test iterations.

A more productive solution to this frequent design problem of prototyping and realising complex PA modes is to develop an RFPA design methodology which is based around the current and voltage waveforms associated with the DUT, the product of which in turn defines the associated produced and dissipated powers. The need for RF waveforms is a crucial part of enhancing the design methodologies behind realising more efficient RFPAs.

2.2.4 Waveform-Based PA Designs and the Utilisation of Nonlinear Device Models in CAD

When considering PA design methodologies which make use of the availability of voltage and current waveform information, the direct link

back to fundamental circuit theory is enabled. This fundamental amplifier circuit theory is widely publicised in text books [19-21]. However more recently than this, many journal and research paper publications have helped "define", through experimental analysis, some of the highly-discussed complex high-efficiency modes of amplifier operation, in particular covering B, E, F and F^{-1}-class modes[3] [22-32], as well as other efficiency-enhancing PA architectures such as the Doherty mode [33-34].

Some of the highest published PA efficiency figures which make use of RF waveforms - at the time that this research started out - are listed in [35-38]. Here, although working at modest power levels less than 1W (Watt), efficiencies (drain and/or power-added efficiencies) consistently above 70% are presented. In these examples the PA architecture commonly implemented is a class-F or inverted class-F mode[3] of operation, highlighting the critical importance of obtaining waveforms at the device-plane in being able to define the mode achieved.

Through more careful detailed inspection it can be shown that an approach based on waveform measurements has the potential capability to unify all design and manufacturing stages of RF systems (Fig. 2.6) enabling the replacement of measurements such as S-parameters, ACPR (adjacent channel power ratio), EVM (error vector modulation), BER (bit error rate) and pulsed I-V plane characterisation [39].

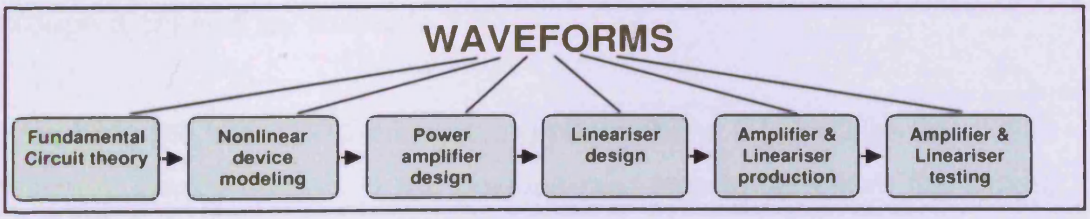

Fig. 2.6. Flow diagram indicating the stages of PA design for wireless communications; The unifying link between them all is "Waveforms" [39].

[3] Description of the PA modes of high relevance and importance to this thesis will follow in subsequent sections of this chapter.

Fig. 2.7 shows example output voltage and current waveforms where relatively high-efficiency performance (61%) is initially observed. This case could quite easily represent a condition which may be appear as a local optimum on a contour plot, obtained from a measurement set-up solely based around power measurements (i.e. Fig. 2.5). It is only on inspection of the current and voltage waveforms seen at the device-plane that any analysis of the perceived "optimum" condition can be carried out. In this example (Fig. 2.7) the loading of the harmonic frequency components can be adjusted such to dramatically improve the efficiency of the device operation and emulate closely a high-efficiency amplifier mode [26, 29], as shown in Fig. 2.7 (right).

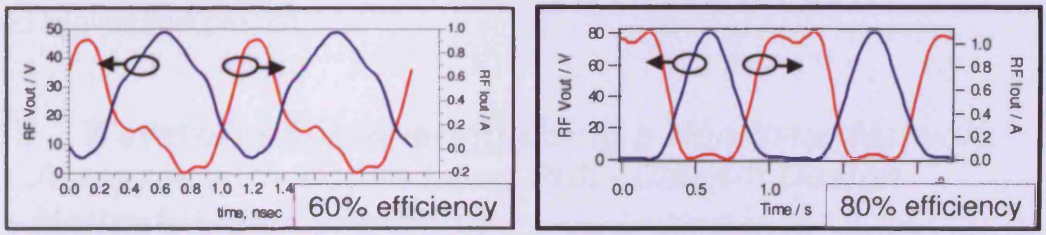

Fig. 2.7. Observing the current and voltage RF waveforms enables a great insight as to where device performance could be improved; In this case, efficiency.

It is vital therefore not only to measure the device waveforms but also to control the relationship between the current and voltage waveforms through waveform-engineering. This can be achieved through the impedance control at each of the harmonics in the signal spectra, i.e. an application of Ohm's law. Section 2.3 describes this in more detail through a case-study example.

Applying the waveform-engineering concept in a CAD environment with nonlinear device models is the obvious next step to take from the simple CAD-based S-parameter design approach described in section 2.2.2. It is here though that empirical or equation-based models, such as those implemented in Doherty PA designs in [40-41], reveal the difficulties in

developing accurate nonlinear models rapidly following the transistor's release to the PA design community. Thus these complex nonlinear device models can be insufficient for efficient and effective PA design, the accuracy of which relying heavily on development time. In response to these perceived reliability issues, several research groups are now focusing on developing new types of measurement systems which enable highly accurate nonlinear device characterisation right down to a RF waveform level in combination with the ability to actively and precisely terminate the DUT in any impedance environment, at multiple harmonics independently [42-46]. Such systems set up the potential for waveform-engineering directly on the device intended for a particular PA design, with the intention of avoiding long and multi-iterative-prone PA design and realisation processes.

2.3 Waveform-Engineering Using a Nonlinear Network Analyser with Active Load-Pull - Class-F Design Methodology Case-Study

2.3.1 A Waveform Measurement System for Enabling Waveform-Engineering

Fig. 2.8 details a waveform measurement and characterisation system with the potential for rapid PA mode design and emulation [44]. The problems highlighted in section 2.2.4 of simulating nonlinear device models in a CAD environment can be overcome by investigating an alternative overall solution to the current design methodology problem. Making use of newly developed measurement set-ups and techniques available, as in [44], is one way of investigating these potentially novel PA design methodologies.

In Fig. 2.8 it can be seen that all waveform capture is focused around a Tektronix 4-channel time-domain microwave oscilloscope. This has

broadband measurement capability up to 12GHz, with the individual channels fed from the forward and reverse signals from port1 and port2 by the four directionally-coupled paths respectively. Precise attenuation is placed in the couple paths to the oscilloscope to ensure power levels do not exceed the compression level of the instruments receivers, but also that the intended working dynamic power range was within the dynamic range of the receivers' measurement capability. Input and output high power bias-tees manufactured in-house feed the necessary current and voltages to the DUT as specified by the user in the control program. An external load-pull test-set is made up of triplexing structures and individual Agilent ESG signal generators (all phase locked using the 10MHz lock capability) with power amplifier stages for each triplexed frequency component. These active load-pull signals are amplified and by using circulators to isolate the output signal from the DUT, the magnitude and phase of each individual load-pull signal can be precisely controlled in the load-pull program. This enables a means of varying the load reflection coefficients seen by the DUT at one or each of the harmonic frequencies [44].

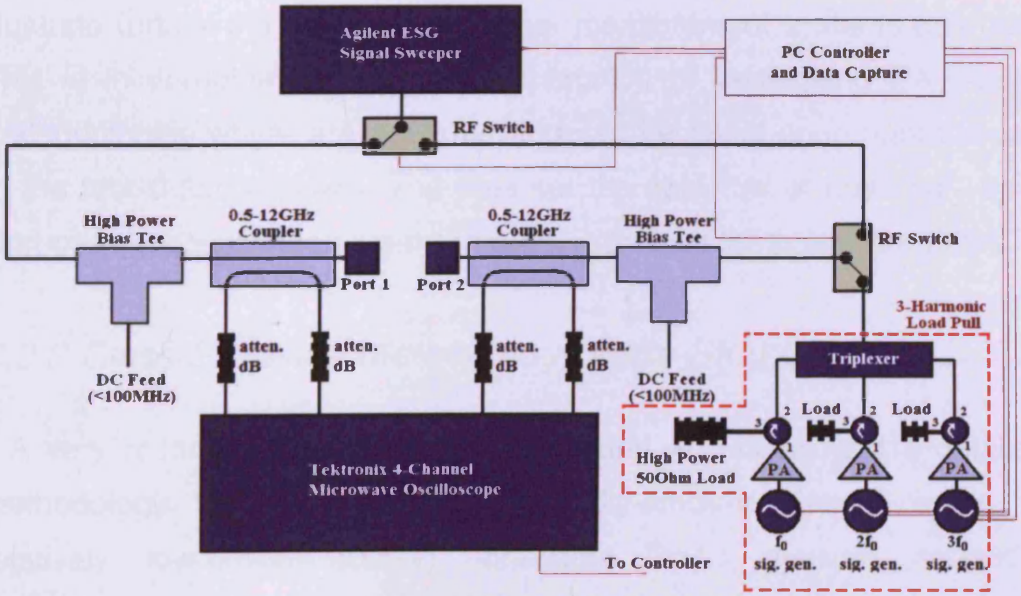

Fig. 2.8. Schematic overview of the waveform measurement and active load-pull system [44].

The RF switches provide a means of repeatable switching of the RF signal sweeper (an Agilent ESG RF signal generator) between port one and port two in order to perform small signal S-parameter measurements on the DUT.

Such a nonlinear measurement system as the one shown schematically in Fig. 2.8 has not only the capability to independently capture the magnitude and relative phase of the forward and reverse waves at the DUT input and output ports, but also the additional combined control of gate and drain bias and multi-harmonic load impedance environments. This system enables a novel means of PA design; one which can be investigated directly on the real DUT and all at power levels up to 120W CW (continuous wave) [44].

These types of nonlinear measurement systems and techniques open up many new possibilities, not only in terms of power amplifier designs implemented directly on a real DUT, but also in terms of device characterisations. These have already been illustrated and presented in [47]. The key aspect of the research presented in this thesis is to illustrate further the role that nonlinear measurement systems can play. This is in combination with the importance of developing PA design methodologies which are accurate and can be relied upon right through to the fabrication process, and thus set the objective of realising - on a 'first-pass success' basis - performance-optimised RF power amplifiers.

2.3.2 Class-F Design Methodology Case-Study

A very recent publication has investigated and developed a detailed methodology for designing an optimally-efficient class-F mode in relatively low-power (0.5W), on-wafer GaAs (gallium arsenide) transistors [48]. This is one of the first research publications which

present results from a combined waveform measurement and multi-harmonic active load-pull-based systematic design approach to engineer the DUT waveforms to suit a specific amplifier mode of high-efficiency operation.

The main objective of this previous research was to make direct use of widely available theory of the class-F mode [23, 27, 30-31, 35, 38], and emulate this theory in a practical approximation of a class-F amplifier. To begin with the class-F mode itself must be defined. Fig. 2.9 shows the ideal characteristic class-F current and voltage waveforms, made up of a perfectly half-wave rectified sinusoid and square waveform respectively. This represents the ideal 100%-efficient device operation synonymous with this mode.

The Fourier transform of these ideal waveforms is also shown in Fig. 2.9, revealing the frequency-domain components. The class-F design methodology in [48] sets out to develop a three-harmonic approximation of the class-F mode. Therefore considering up to the first three-harmonics of the ideal case, and applying the inverse Fourier transform to this spectrum, the waveforms for a three-harmonic approximation of class-F are obtained. However the theoretically-optimum efficient, or 'maximally-flat' [23] case for a three-harmonic approximation of class-F sees the fundamental, second and third harmonic components adjusted from those of the ideal infinite case, as shown in Fig. 2.10. The efficiency of this three-harmonic approximation is in-turn reduced from that of the 100% ideal case, and is so by bandwidth-limiting factors imposed on the current and voltage waveforms respectively [23]. This results in an optimum efficient condition of 90.6%, as components of the current and voltage waveforms have the potential for overlap, and thus lead to a proportion of power dissipation.

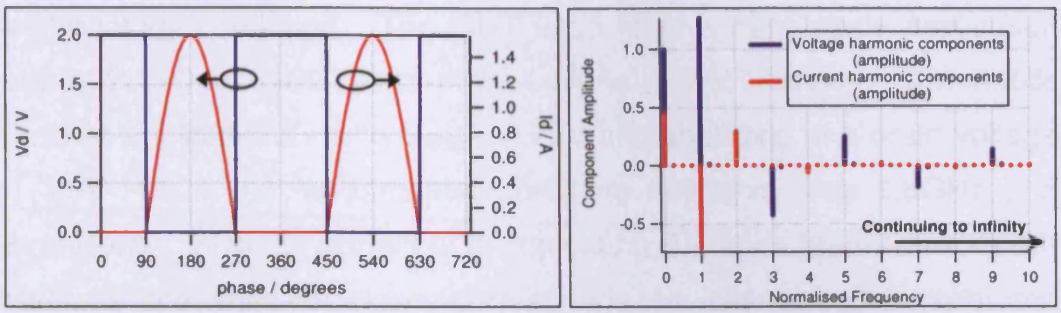

Fig. 2.9. (Left): Ideal (infinite-harmonic) class-F output voltage and current waveforms, (Right): Frequency-domain spectrum of the same ideal class-F case.

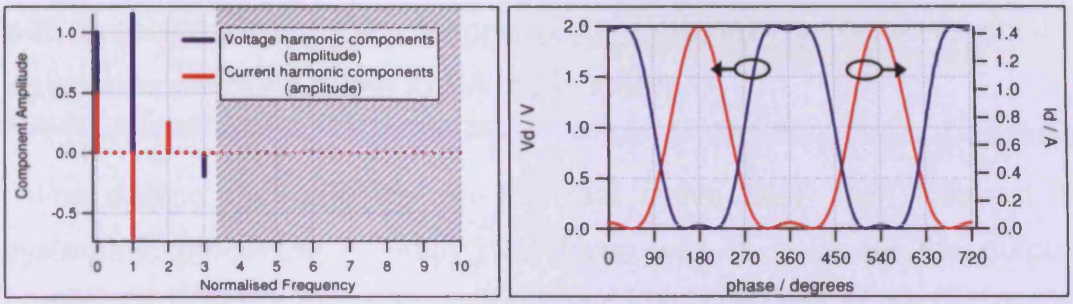

Fig. 2.10. (Left): Spectrum for a maximally-flat three-harmonic approximation of class-F, (Right): Resultant time-domain current and voltage waveforms for the class-F approximation.

This maximum achievable device efficiency is in fact further reduced by the discrepancies between an ideal RF switch and the GaAs technology pHEMT (pseudomorphic HEMT) intended for the design. Such non-idealities extend to the turn-on characteristic of the real DUT and thus the achievable minimum voltage (voltage-offset, or 'V_{knee}') and available range for the voltage waveform to develop. This reduces the overall achievable efficiency (η) figure from 90.6% to approximately 71.2% when working with a fixed drain voltage supply (V_{DC}) - a result shown by Eq. 2.5:

$$\eta_{drain} = \frac{V_{DC} - V_{knee}}{V_{DC}} \times 90.6\% = \frac{3.5 - 0.75}{3.5} \times 90.6 = 71.2\% \qquad (2.5)$$

With the design theory set and an efficiency target enabling a means of performance verification, the development of a class-F design

methodology continues. The DUT used for this case-study application was a 2x100μm (100 micro-metre) GaAs pHEMT device - for mobile handset applications - with V_{knee} =0.75V and operating at a drain voltage of 3.5V [48]. The fundamental operating frequency was 1.8GHz (1.8 Giga-Hertz). A major benefit of investigating PA mode theory directly on-wafer is the relative close correspondence between the calibrated (measured) and the device current-generator plane RF waveforms. Hence in this example there is a limited requirement for de-embedding, with only the output capacitance (C_{ds}) to remove in order to obtain waveforms which correlate to PA mode theory.

The design methodology on the real active DUT then followed a systematic procedure. Firstly, the focus was to engineer the output current waveform into the three-harmonic approximation of the half-wave rectified sinusoid, whilst driving the device into its optimum fundamental load. Essentially the bias point (V_g) of the device enables control of this, and it was the objective of the work in [48] to analyse the individual output current harmonic components and adjust V_g accordingly to ensure the third-harmonic output current component is nulled. This then eradicates any overlap in waveforms (and hence power dissipation) with the third-harmonic voltage component which will be, by definition, present in the squared voltage wave. With the optimum gate voltage not completely independent of the drive level to this real device (Fig. 2.11), the measurement system on which this design methodology was implemented [44] provided the means by which to independently control and/or fix drive, and so give the designer a means of choosing a drive level and bias point at which to set the design.

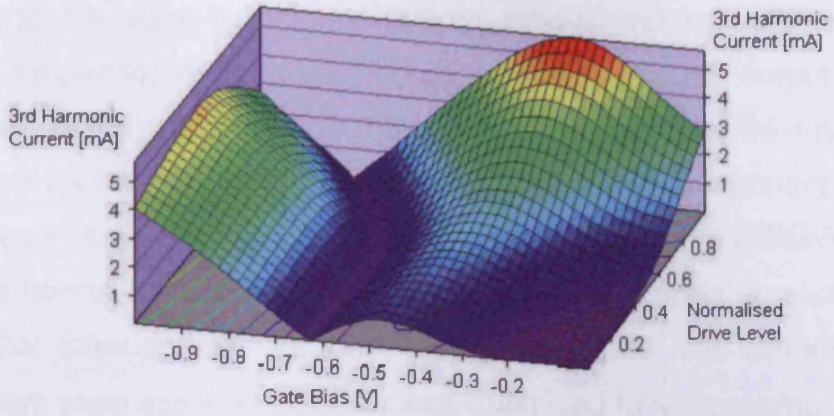

Fig. 2.11. Third-harmonic current magnitude as a function of gate bias and normalised drive level (ranging from linear operation to hard compression) [48].

Following this, the attention of this methodology then switched to engineering the output voltage waveform in order to obtain the optimum and theoretically maximum-efficient condition predicted by theory (Eq. 2.5) of 71.2%. In setting the required second-harmonic short impedance, thus to remove any unwanted second-harmonic component from the output voltage waveform, several observations were made in [48]. It became apparent that there was an importance in the 'quality' of the short; that being the ratio of the real second-harmonic load compared to the real fundamental load. A ratio of any less than 1/10 saw a degradation in the efficiency recorded. This poses the challenge of scaling the class-F design methodology to higher power devices where the fundamental optimum load tends to be lower, thus succumbing to the difficulty in realising second-harmonic loads a tenth of the size. This observation however opens up the opportunity to investigate other modes of operation where a second-harmonic 'short' is not necessarily required. This could potentially be something as simple as replacing the second-harmonic 'short' with an 'open' impedance where a scaling of 1:10 from the fundamental optimum load is more realistic - i.e. the class-F^{-1} mode (see section 2.5).

Finally for the class-F design in [48] the third-harmonic load impedance can be independently controlled so as to now square the output voltage waveform. This requires, from theory of class-F [22], a third-harmonic voltage component of 1/6 of the fundamental voltage component, and as such through the use of the active load-pull element of the utilised system the third harmonic load was adjusted towards an 'open' impedance to satisfy this criterion. By carefully re-adjusting bias and harmonic load parameters once again the design was optimised fully, revealing the very high-efficiency device operation that had been obtained.

The described case-study in this section has demonstrated the novel use of an RF waveform measurement system, in combination with multi-harmonic load-pull, for waveform-engineering high-efficiency modes described by theory. In this example a peak efficiency of 75% was recorded, in line with - and in fact just above - that predicted by prior analysis and calculation. Fig. 2.12 shows the RF waveforms from this optimum condition, once again providing a highly reliable means of validation that a class-F-mode approximation has been achieved from this systematic methodology.

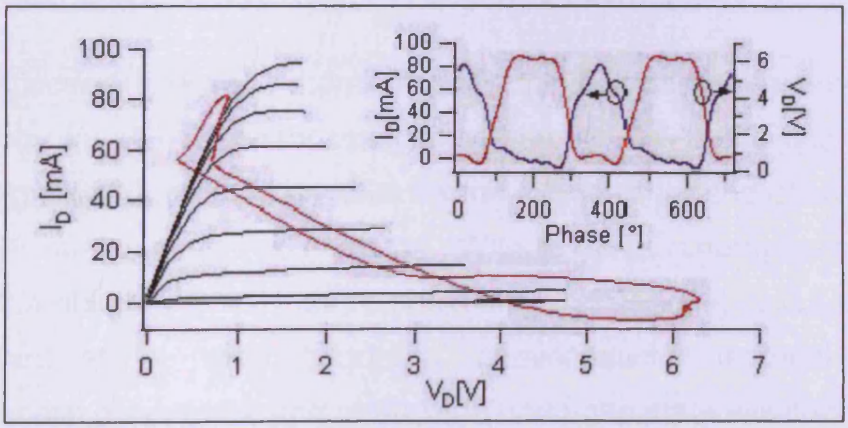

Fig. 2.12. Final peak-efficient RF waveforms obtained in [48] following class-F design.

Described in the research paper itself [48], the role of C_{ds} has led in-

part to the distortion of the current waveform away from the theoretically-defined shape as a result of current flow across C_{ds}, which in-turn has been caused by the third-harmonic voltage component that was present. This parasitic element has not being fully accounted for in this methodology, and the acknowledgement that larger device-based designs would increasingly require the removal of C_{ds} in order to obtain meaningful waveforms is an important one. It is the objective of the work described in the subsequent chapters of this thesis, to investigate such larger device-based design methodologies and thus enable a scaling of waveform-engineering processes to high-power amplifier designs for base-station applications, where efficiency enhancement is also crucial. Of similar importance is the investigation into waveform-engineering-based PA designs implementing different device technologies to that already looked at in this design case-study - particularly in light of newly emerged device technologies such as wide band-gap GaN RF transistors [49-50].

2.4 GaN Device Technology and Applications Within PA Design for Wireless Communications

2.4.1 GaN Compared with GaAs and Si LDMOS

The successful development of gallium-nitride-based semiconductor technology for RF transistor applications during the 1990s has brought with it significant potential benefits for the PA designer and of course the wider RF communications industry. With a typical energy gap (E_g) of 3.4eV (3.4 electron Volts) - three times that of Si (silicon) or GaAs - GaN is defined as a 'wide band-gap' semiconductor material. This characteristic gives GaN, and other wide band-gap materials such as SiC (silicon-carbide), not only a much higher breakdown voltage property [6, 49], but also a lower turn-on-resistance (R_{on}), making it highly suited to high efficiency RF PA applications [49]. GaN retains these benefits

without compromising on longer electron transit times, and thus lower transit-frequencies (f_T); this being the case if FETs (field effect transistors) fabricated from GaAs (for example) were re-dimensioned to accommodate the same high voltage operation [49] (Fig. 2.13). The ability to operate at much higher voltages once again in-turn means that GaN transistors can exhibit very high output powers per size of gate periphery - more than 10W/mm at S and C-band frequencies (approximately halving at X-band frequencies), as opposed to typically less than 1W/mm from GaAs FETs [6].

Overcoming initial reliability issues encountered with the new fabrication processes of GaN RF transistors, the technology has now developed further enough for many RF device manufacturers - such as Nitronex [51], CREE [52] and Fujitsu [53] to name just a few - to commit to commercial manufacture of GaN transistors and benefit from the important new power amplifier applications that GaN technology promises, as already detailed above.

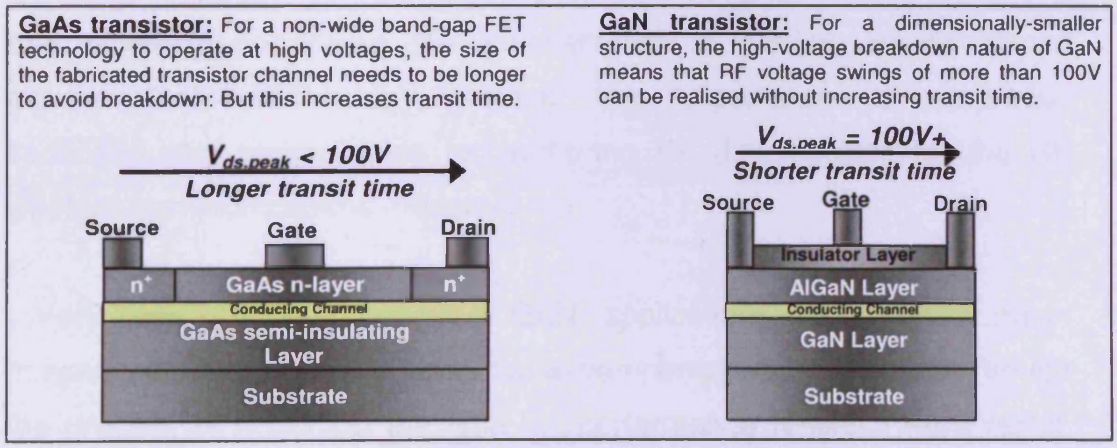

Fig. 2.13. Comparing breakdown of conventional semiconductor FETs with wide band-gap GaN transistor technology.

Some examples where Si LDMOS (laterally diffused metal-oxide semiconductors) or GaAs transistor technology are utilised in high-

efficiency PA designs which develop high peak output voltages, i.e. class-E [14] and class-F^{-1} [18] - where the peak voltage swing is by definition more than three-times the DC voltage bias level - have had to employ a trade-off on the DC drain voltage bias level; reduced from the nominal 28V to 18-20V. An example where a 28V drain voltage was implemented in a class-F^{-1} mode design around a Si LDMOS device details the observation of the onset of breakdown [54], clearly indicating the problems of comparably low voltage breakdown in Si LDMOS.

The high-voltage breakdown capability of GaN makes it a more suitable choice for PA designers developing designs where high peak voltages, several times larger than the utilised drain voltage, will be exercised.

2.4.2 Current Applications of GaN Device Technology in RFPAs

There are many reported applications of GaN in PA designs which exhibit and reveal the beneficial properties of this relatively young RF device technology. Bandwidth-enhanced PA designs such as in [55-57], and efficiency-enhancing PA architectures in [58-59], all developed around GaN technology, reveal the importance of improved semiconductor technologies for furthering PA development for the RF wireless communications industry.

Very few of these reported GaN applications have, once again however, presented any substantial experimental waveform data through the process of obtaining the final PA performance results. As a result, despite observing improved device performance than may be realisable with previous device technologies, there is no clear indication as to whether a 'final-optimum', e.g. in terms of efficiency or bandwidth, has been obtained.

Here, waveform-engineering-based design methodologies have the potential to reveal to the PA designer whether optimum device performance has been achieved, just as is possible for any device technology. The independence as regards to the DUT technology utilised - whether more established, or in its relative infancy - means that each specific PA design methodology can in theory be adapted to suit any RF device technology. In the case of gallium nitride, this could potentially be extending peak RF voltages such as in the class-F^{-1} mode (section 2.5.1), or carrying out investigations into combined optimum broadband-efficient modes ('class-J', section 2.5.2) with a technology arguably best-suited to such operation.

2.5 Efficiency-Enhancing PA Modes for the Basis of Novel Waveform-Engineering Design Methodologies

2.5.1 The Inverse Class-F Mode of Power Amplifier

Similarly to the more commonly-seen class-F mode (as described in section 2.3.2) the inverse class-F mode is defined by its characteristic half-wave rectified sinusoid and perfectly square output waveforms, however in this case these waveform shapes correspond to the output voltage and current respectively (Fig. 2.14); a reversal from that defined by the standard class-F mode [26]. This mode too has the theoretical capability of developing 100%-efficient device operation, and is a mode that has relatively recently been gaining increased interest by PA designers for high-efficiency applications at high powers [17, 28-29].

Conversely to class-F, the current waveform in this case is now square, containing a fundamental component and all odd harmonics. The way in which this is achieved, as regards to device operation, is to bias the DUT in class-A, and drive it hard into compression such that the output current waveform is clipped perfectly square by the device operation boundaries.

It is then necessary to open-circuit load all of the even harmonic components, whilst short-circuiting the odd harmonic components, in order to shape the output voltage to a perfect half-wave rectified sinusoid.

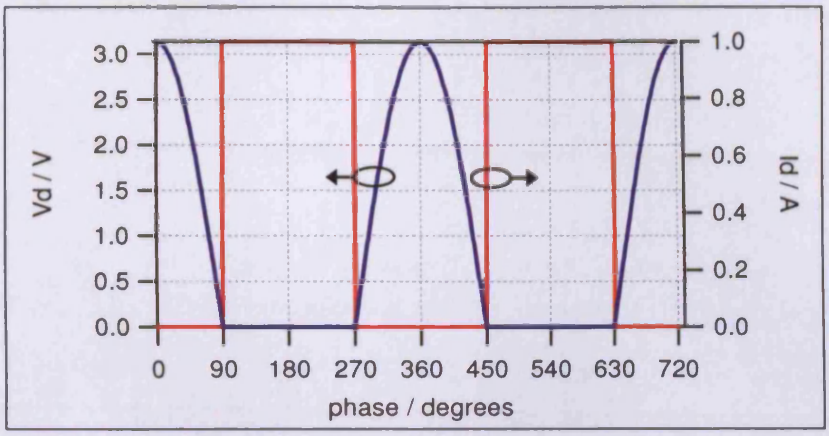

Fig. 2.14. Ideal (infinite-harmonic) class-F^{-1} output voltage and current waveforms.

A class-F^{-1} design methodology could follow similar steps to the class-F methodology described in section 2.3.2, setting out to develop a three-harmonic approximation of the class-F^{-1} mode. Of course, implementing it in real devices with non-ideal characteristics will lead to further performance approximations. However these considerations can all be accounted for in the same way as described for the class-F design methodology, enabling calculated predictions of achievable performance to be obtained prior to design.

It is the objective of part of the research carried out in this thesis to develop a high-efficiency design methodology for realising optimum approximated class-F^{-1} operation. Further challenges of implementing this on a high power packaged GaN device will be investigated revealing a potential solution to the perceived issue (raised in [48]) of scaling waveform-engineering to higher power devices.

2.5.2 Class-J: A Potential for High-Efficiency, Linear and Broadband PAs

Another even more recently presented mode is the class-J amplifier. Although the mode itself is not a new concept as regards to the practical PA, it is only recently (2006) that the operation has been defined theoretically [60]. Since this, only a small number of research publications have followed which recognise the class-J-mode operation [61-63].

In [60] Cripps initially defines class-J as a more practically applicable mode of operation than the more classical modes in that it makes direct use of intrinsic parasitic elements such as the drain-source capacitance (C_{ds}) present within a real device as part of the physical DUT loading criteria. The objectives of the theory surrounding class-J is described by Cripps as taking the approach of somehow incorporating the device non-idealities into the PA mode theory leading to deviations away from classical harmonic short and open terminations used in other efficiency-enhanced PA modes [60]. In a practical class-B PA design it is the ratio between X_C (the capacitive reactance of C_{ds}) and R_L (the optimum fundamental load) that defines how close to classical class-B the practical PA approximation will be. A ratio less than 1 assumes class-B operation with shorted harmonics. However this ratio, although not periphery dependent, is technology dependent and it is shown in [60] that by applying a range of reactive offsets to the fundamental load, the class-J mode can be 'tuned' so as to enable a broader range of X_C/R_L (above 1) to suit the requirement for the peak-efficient linear condition associated with the bias point implemented (78.5% for class-B) [60].

The frequency dependence of X_C opens up the scope for this mode of operation - based around more practically applicable theory - to be

investigated further through experimental measurements for its broadband potential in achieving efficiency enhanced PA operation.

Working alongside more recently published research (2009) which defines the class-J mode through a robust combination of theory and experimental validation [64], the research presented in the subsequent chapters of this thesis has investigated the use of this newly presented amplifier mode-theory for the development of a broadband amplifier design methodology. Just as for the class-F and class-F^{-1} modes described previously, it is the objective to optimise device performance in a systematic manner by means of waveform-measurements and multi-harmonic impedance control. From the already-presented theory covering the class-J mode, there is shown a potential for efficiency-enhanced device performance across a significant bandwidth. In making a full characterisation of the mode, connections between the theory and real devices under-test can be established. Once again, waveforms enable such means for comparison and further understanding of the mode. Thus in-turn, this provides a means for a more systematic and measurement-focused approach to realising the full potential of class-J; a mode which although may already be being implemented inadvertently by PA designers, is one which will aim to avoid the blind-folded, non-optimal design approach that arguably exists currently.

2.6 Chapter Summary

This review chapter of current literature on the topics surrounding the efficiency enhancement of RF power amplifiers has revealed several important factors. These most notably includes the limitations that current PA design practices exhibit as regards to yielding (of which is crucially the key, and arguably the most important aim of any PA design) the best possible performance from your device. Focusing on the implementation of specific modes of PA operation for the purpose of achieving optimum efficient device operation, many of the existing PA design methodologies lack any use of RF waveform measurements in the validation of such modes. This by definition requires the complex device output waveforms to be shaped, or 'engineered' to a precise degree. This review has described the increasing capability to measure RF waveforms accurately and across very wide frequency bandwidths, which thus paves the way for novel PA design methodologies - such as those presented in the following chapters of this thesis. It is this direct use of measured RF waveforms which is key in this work. And in fact is the crucial concept when designing and engineering specific modes of operation described by the PA mode theory already presented by many of the authors referenced throughout this and subsequent chapters.

Presented in this review have been several examples of PA designs where the prototyped PA has not fully met predicted performance. Yet without waveform data in the practical design a means of determining the reasons for any discrepancies cannot be made. Methodology examples in this review where RF waveforms *have* been utilised in the form of CAD models, rely heavily on the accuracy of such models. Thus any performance discrepancies revealed by the prototype PA once again succumb to a lack of waveform data on the real device itself for comparison.

The work detailed in the following chapters of this thesis aims to make a more sophisticated use of the RF waveforms measurement capabilities which already exist, with the further aim of developing novel design approaches to overcome the PA design methodology problem of realising performance-optimised power amplifiers, particularly for the design of efficiency-enhanced amplifiers for wireless communications applications. This, most notably, will make use of newly emerging high-power packaged GaN devices; a semiconductor technology which has already shown the potential for high-voltage, high-efficiency and high-bandwidth operations.

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Chapter 3. High Power Waveform-Engineering-Based High-Efficiency PA Design

3.1 Introduction

As detailed in **Chapter 2**, a previous design methodology has investigated the use of waveform-engineering for optimising efficiency in GaN on-wafer devices [1]. In this chapter, the step-up in device size and output power capability poses several new questions in terms of how a design methodology for yielding very high-efficiency device operation needs to be adapted from that described in [1]. The work undertaken and detailed within this chapter sets out the development of a new methodology to answer these questions. Such procedure adaptations from that in [1] include the obvious difference in device packaging and requirement for extensive de-embedding; from intrinsic parasitics[4] with on-wafer devices, to full extrinsic and package de-embedding with larger, higher power devices made up of multiple transistor cells.

In this chapter the chosen mode of operation, and thus starting point for theoretical investigation, was the class-F^{-1} mode (as investigated and discussed elsewhere in [2-3]). A previous study on class-F^{-1} design has shown that higher theoretical efficiencies can be obtained compared to class-F amplifiers when considering 'on-resistance' effects [3]. Another

[4] "***Parasitics***" is used as a plural to describe the total effect of the individual output parasitic elements.

reason for choosing this mode includes the large voltage swing associated with class-F^{-1} operation, which is key to achieving the high power and high efficiencies with this mode of operation (see **Chapter 2**). This can often be difficult to realise with many current device technologies (e.g. Si LDMOS, GaAs) due to the limitations induced by device breakdown voltages [4]. However, with advancements in wide band-gap semiconductor technologies (GaN, SiC), larger voltage swings, and thus DC rail voltages, become feasible, hence allowing for power amplifiers with very high-efficiency performance to be realised [5]. For the case of the device output power being held constant, an additional advantage arises in that the maximum drain current swing can be reduced to minimise any effect of the 'knee' (offset voltage) [6-7]. This wide band-gap device technology was to be the basis of this power amplifier design methodology.

In this study a 10W GaN HEMT from CREE Inc. (part number CGH40010F, see **Appendix A1** for device datasheet) was used. Investigations were carried out at two fundamental frequencies, of 0.9GHz and 2.1GHz - two of the major wireless communication frequencies in which, for example, satellite services and 3G telecommunications are situated respectively - using a high power active harmonic load-pull waveform measurement system [8-9]. A procedure developed for optimising class-F operation for on-wafer devices in [1] has been adapted in the development of a class-F^{-1} design procedure for optimising efficiency of packaged high power GaN devices. The implemented de-embedding process [10] allows for analysis and engineering of the RF waveforms that exist at the device current-generator plane, and hence, with further waveform measurements of the final optimised design, and comparisons with PA mode theory, enables a means of determining the degree of success as regards achieving the target mode of operation.

3.2 Measuring High Power Packaged Devices

3.2.1 Device Stability Analysis

As with any PA design approach, the importance of prior stability analysis of the device intended for a design is a key stage in the development of all high power amplifiers. As described in **Chapter 2**, the waveform measurement system can implement a broadband '50Ω' impedance environment from 0.5GHz, up to 12.5GHz [8-9]. This set-up enables a good and accurate means of measuring small-signal S-parameters across similarly wide frequency ranges as described in [8-9].

A device fixture was developed to accommodate the packaged GaN HEMT device, whilst maintaining the broadband 50Ω impedance through the use of microstrip lines milled onto Rogers TMM® (a thermoset microwave laminate). Fig. 3.1 shows this fixture with the DUT in place, along with the manufactured TRL (thru-reflect-line) standards for calibration [11] (see **Appendix A2** for details on this TRL calibration).

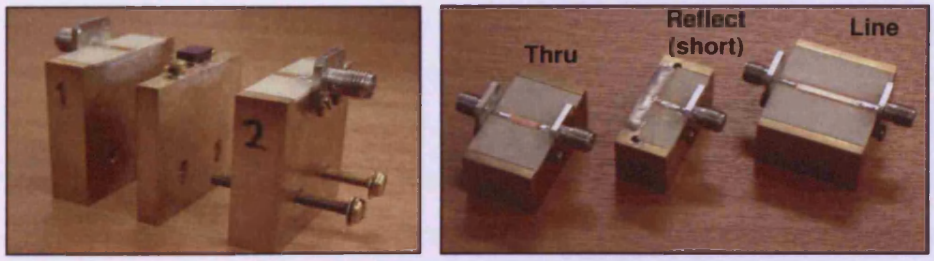

Fig. 3.1. Device fixture (left) and TRL calibration standards for use in measuring the DUT (CGH40010F)

Measured bias-dependent S-parameters of the DUT (CGH40010F) were made between 500MHz and 6.5GHz with steps of 100MHz, encompassing the important potentially-unstable frequency band upper-limit of approximately 3.5GHz, as well as the intended device operation centre frequencies of 0.9 and 2.1GHz, and appropriate harmonics.

Saving this data to a touchstone ".S2P" file format, and importing directly to Agilent's ADS CAD environment, the stability 'K'-factor, as well as load and source stability circles, can then be calculated and plotted for each frequency of interest on the Smith Chart, an example of which is shown in Fig. 3.2 for the bias condition V_{gs}= –1.8V.

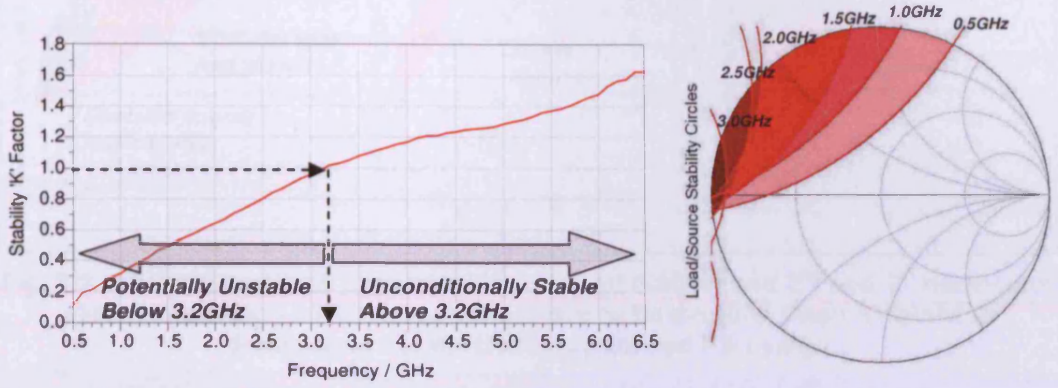

Fig. 3.2. Left: Calculated wideband K-stability factor, and Right: Load-stability circles from measured small signal S-parameter data of CGH40010F, shaded areas indicating frequency-dependent unstable regions of the unity Smith Chart.

Although a relatively straight forward procedure, this practical analysis of the device S-parameters enables an essential insight into the DUT's broadband behaviour, not only in terms of small-signal gain (S21), but also the potential for instability and oscillation as a function of presented load and/or source impedance(s). Since these S-parameters have been measured directly from a real working device at a given bias condition, they give a much more reliable and precise indication of which regions on the Smith Chart are to be avoided during the load-pull stage of the multi-harmonic impedance control and DUT performance optimisation (Fig. 3.3).

Since the DUT being implemented here is a packaged power transistor device, the impedance considerations for stability apply to the calibrated reference plane of the device package-plane. The intention during the PA design methodology development was to apply parasitic de-

embedding and observe operation at the $I_{gen.}$-plane, hence careful regard for potentially-unstable regions of the Smith Chart needs to be adhered to at the appropriate reference planes.

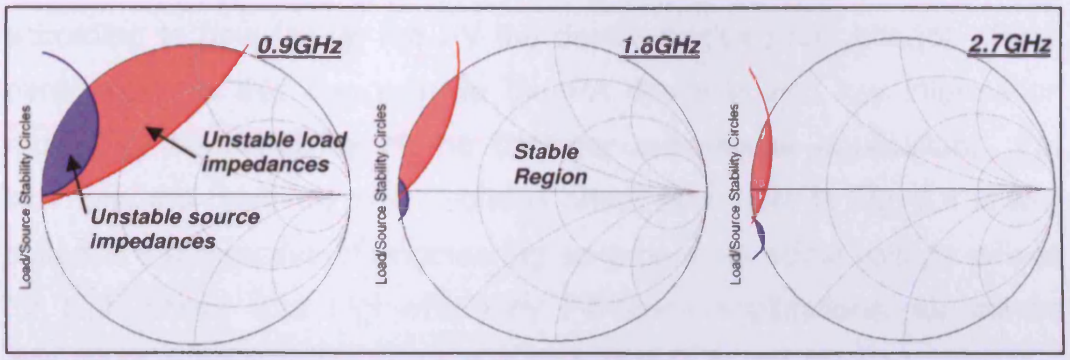

Fig. 3.3. Smith Chart with load stability circle at 0.9GHz and 2nd and 3rd harmonics clearly indicating which impedances are to be avoided when it comes to developing the efficiency-optimised PA design.

A more detailed description of the full stability analysis procedures implemented can be found in **Appendix A3**.

3.2.2 Understanding the Device Waveforms

As previously discussed in this chapter, the utilised TRL calibration generates a calibrated measurement reference-plane at the device package and not, as is the case for on-wafer measurements, close to the device $I_{gen.}$-plane. Thus, by generating an equivalent circuit model for the approximated package network and output parasitics, it is possible to enable a means of predicting and analysing device operation at the approximated $I_{gen.}$-plane during the design process [10]. This process is essential for enabling RF waveform-engineering from PA-mode theory, as it allows for correlation between the measured dynamic I-Vs and the device DC-IV plane which defines the boundaries of the device performance.

Fig. 3.4 shows a typical output DC-IV plane of the device 'CGH40010F'

following static-IV characterisation. Also indicated on this figure is an example class-A-mode load-line (35Ω) from which the DC voltage offset, or 'knee-voltage', is determined. The knee-voltage arises as a result of the non-ideal turn-on characteristic of the transistor, and hence will vary according to how far up the I-V the device peak current hits [6]. Such parameters as this can provide the PA designer with key information regarding the suitability of the DUT for a particular application. For example, the relatively small voltage offset seen here in Fig. 3.4 is well suited to the objective of engineering as-large-as-possible voltage swings for high power and high-efficiency PA-mode applications, as will be discussed in more detail in the following section of this chapter.

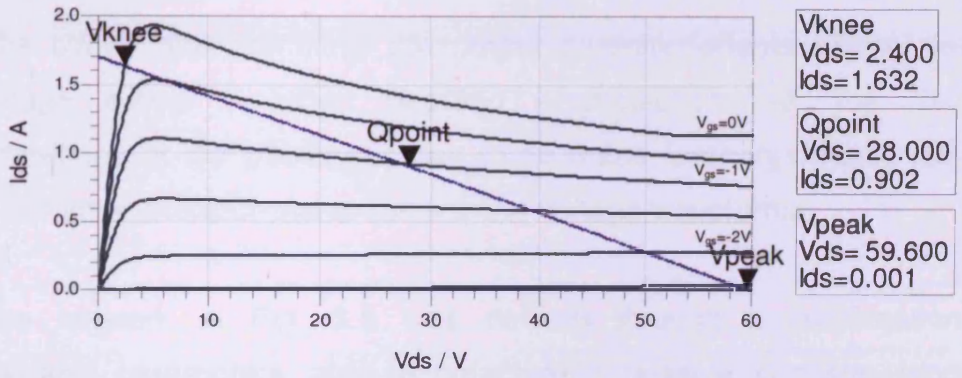

Fig. 3.4. Static output DC-IVs of device CGH40010F indicating saturated drain current level, DC voltage offset ('knee voltage') for an example load-line, and the device I-V characteristics between V_{ds}=0 to 60V.

Continuing to remember that the device output DC-IV characteristic defines the hard, outer boundaries of the device operation at the $I_{gen.}$-plane, the need therefore exists to translate these boundaries to the device package-plane when scaling up from DC to RF frequencies.

Fig. 3.5 shows a schematic circuit that was developed to represent approximately the output parasitics of the CGH40010F GaN HEMT device.

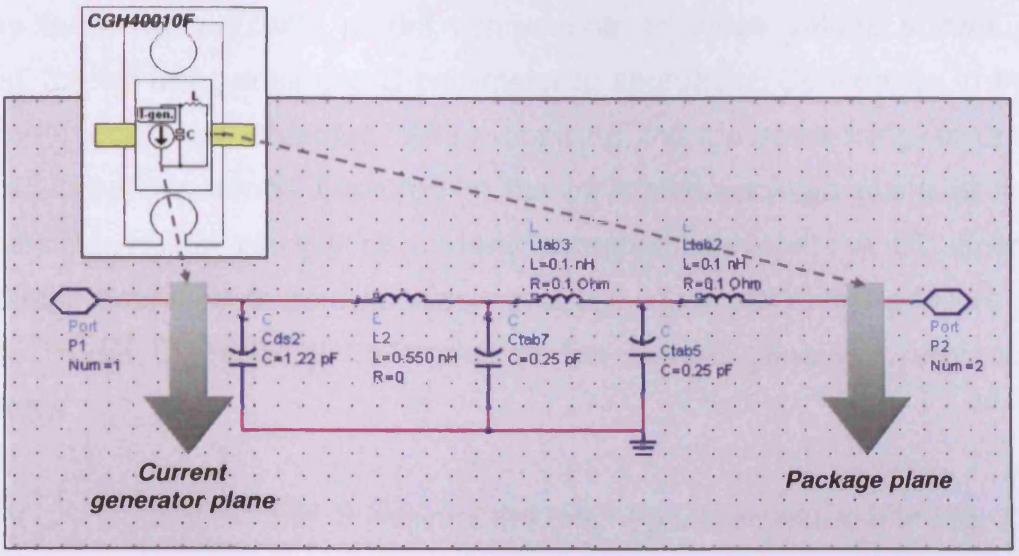

Fig. 3.5. Approximated equivalent network of device output parasitics for DUT CGH40010F.

The circuit approximating the output parasitic effects of the device package allows – when negated – predictions for the desired terminations at the package-plane to be made, and importantly reveals the current-generator-plane current and voltage waveforms.

The network in Fig. 3.5 was derived through a combination of datasheet parameters and manufacturer's passive package models. Specifically, the output capacitance (Cds2, Fig. 3.5) is stated in this transistors datasheet (see **Appendix A1**). The inductance L2 (Fig. 3.5) approximates the total bonding wire inductances. The number of bonding wires for this transistor was known, as well as their approximate dimensions. Thus by simulating these individually using the 'Lbond' bond-wire modelling component in ADS the approximate total inductance was obtained for the parasitic model. The remaining part of the output parasitics to model was the tab of the packaged transistor. This was modelled as a pair of series-L/shunt-C components (Ltab2, Ltab3, Ctab5, Ctab7 in Fig. 3.5). The package model that had been provided by the transistor vendor as an S-parameter file then enabled an optimisation of

the individual parasitic model components to those values shown in Fig. 3.5 by using a simple S-parameter-fit approach. Confidence in the model could be obtained when applying the de-embedding to any measured waveforms captured at the calibrated package plane of the transistor. Any voltage or current 'overshoot' beyond the DC knee-voltage boundary or zero-boundary respectively would reveal a failure in the model to perfectly de-embed to the current generator reference plane.

It is important to note, that since the output parasitic network in Fig. 3.5 consists of passive elements only, there are no nonlinear characteristics associated with it. Therefore all de-embedding applied in this work is done so without explicitly considering any nonlinear elements that may exist in reality. This approximation is more closely applicable to GaN devices than for LDMOS, most especially with regards to the output capacitance C_{ds} (component Cds2 in Fig. 3.5). However due consideration of this in-place approximation must be taken into account when applying this de-embedding network. The de-embedding applied in this case is used to enable a strong indication of the mode of operation that is being facilitated during the multi-harmonic load-pull optimisation stage of the PA design. In combination with the device output performance figures it is been possible to analyse, and thus optimise, the device performance for the class-F^{-1} mode of operation that is detailed in this chapter in a much more rapid manner (see **Appendix A4** for a specific example of the application of this de-embedding analysis) [10].

Using the theoretical class-F^{-1} loading [2-3] detailed in **Chapter 2**, the passive model, developed to represent the output parasitics of the GaN device, enables the complex loads required at the package-plane to be found. This is done through the translation of the ideal class-F^{-1} 'real' loads via S-parameter simulations in CAD (see **Appendix A4)**. Table-3.1

presents the second harmonic open and third harmonic short reflection coefficients (fundamental loading is presented in the next section of this chapter), at both the current generator and package reference planes of the CGH40010F device, required to establish a three-harmonic approximation of class-F^{-1} operation.

Frequency	*Ideal Class-F^{1} reflection coefficient at $I_{gen.}$-plane*	*Ideal reflection coefficient at package-plane for f_0=0.9GHz*	*Ideal reflection coefficient at package-plane for f_0=2.1GHz*
$2f_0$	$1\angle 0°$ *(open)*	$1\angle 95°$	$1\angle 160°$
$3f_0$	$1\angle 180°$ *(short)*	$1\angle -149°$	$1\angle -89°$

Table-3.1. Class-F^{-1} harmonic load reflection coefficients at current generator, and embedded package-plane at 0.9GHz and 2.1GHz.

The package-plane complex impedances correspond to two operation frequencies; 0.9GHz and 2.1GHz respectively, as intended for the PA designs in the following section of this chapter.

With clear definitions of where the waveforms of interest exist, the development of a waveform-based design methodology can begin.

3.3 Inverse Class-F Theoretical Performance Prediction

The ideal class-F^{-1} output waveforms, shown in Fig. 3.6*(a)*, of half-wave rectified voltage and square current represent a perfectly functioning, 100% efficient class-F^{-1} amplifier. In reality this ideal performance is compromised by the DC offsets, as well as the ability to generate the perfect harmonic terminations required, as previously detailed in **Chapter 2**.

For the theoretical predictions made for this particular design case it is assumed that the output current waveform will contain components up to the fifth harmonic (through hitting the current boundary conditions at peak

drive), whilst the output voltage waveform - shaped by the active loading provided through waveform-engineering - would be optimised up to the second harmonic component. These 'ideal approximations' of the output waveforms are shown in Fig. 3.6*(b)*. In this approximated case current and voltage bandwidth limitation factors now become applicable when calculating the maximum theoretically achievable device drain efficiency, depending on the number of harmonic components being optimised in the each of respective output waveforms [2-3, 12-13].

Applying the equation for drain efficiency (η_{drain}) in [3], the theoretical efficiency for the above harmonic-approximation of a class-F^{-1} amplifier design, with DC voltage offset, V_{knee}, becomes that shown in Eq. 3.2:

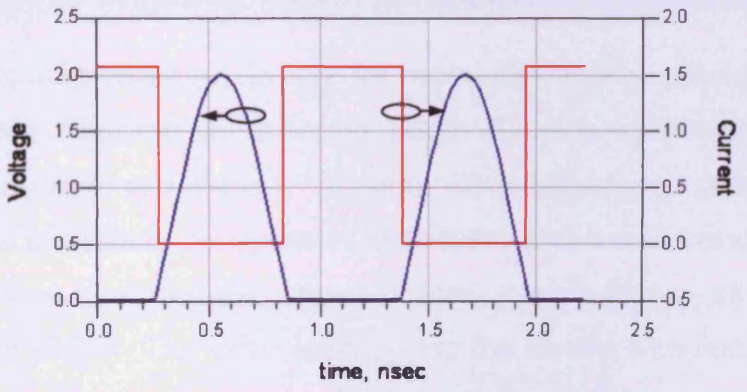

Fig. 3.6*(a)*. Ideal class-F^{-1} output current and voltage waveforms.

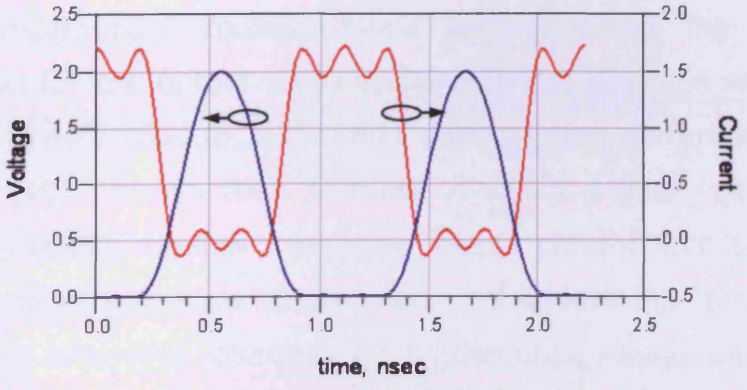

Fig. 3.6*(b)*. Class-F^{-1} output current and voltage waveforms, approximated to five and two harmonics respectively.

$$\eta_{voltage} \cdot \eta_{current} = 1.000 \times 0.854 = 0.854 \quad (3.1)$$

$$\eta_{drain} = 100 \times \frac{V_{DC} - V_{knee}}{V_{DC}} \times \eta_{voltage} \cdot \eta_{current} = 100 \times \frac{28 - 0.5}{28} \times 0.854 = 83.9\% \quad (3.2)$$

Where $\eta_{voltage} \cdot \eta_{current}$ is the product of the voltage and current bandwidth limitation factors derived from [2, 12]. V_{knee} is the value of the DC voltage offset (0.5V used here), whilst V_{DC} is the drain voltage bias (28V here).

3.4 Waveform-Engineering High-Efficiency Modes

3.4.1 Practical Implementation at 0.9GHz

Processes implemented in [1] for obtaining highly efficient class-F designs were adapted in order to begin developing a procedure for obtaining an optimised class-F^{-1} design. This included a sweep of gate bias voltage to identify an optimum bias point which was conducted with the necessary fundamental and harmonic terminations, as stated in Table-3.1, in place. The drive level during the sweep was such that gain compression was approximately –3dB.

Once package-plane measurements were obtained, the equivalent circuit model for the output parasitics and device package was utilised once again to de-embed to, and reveal, the $I_{gen.}$-plane current and voltage waveforms [10]. It was then possible to select a gate voltage which would more readily enable a squared output current and half-rectified output voltage waveform to be obtained. To achieve this, both the ratio of the second harmonic voltage to the fundamental voltage, and the ratio of the third harmonic current to the fundamental current, was selected in accordance with class-F^{-1} theory.

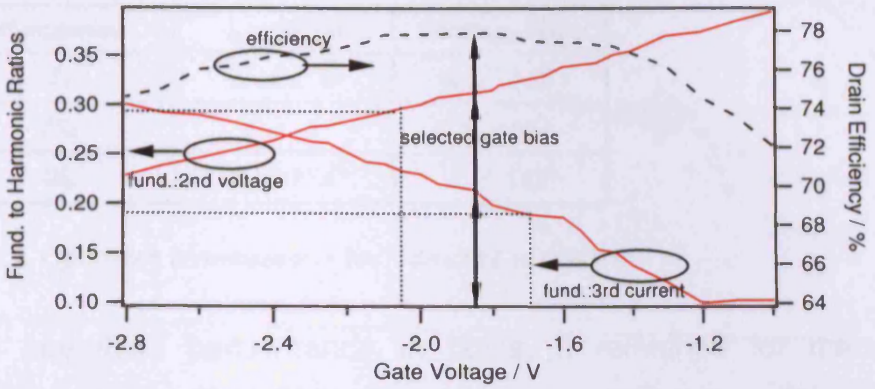

Fig. 3.7. Gate sweep at 28V drain voltage bias condition at 0.9GHz.

Due to the limited number of harmonic terminations employed, the optimum (maximally flat [13]) harmonic current and voltage ratios required were less than those for the infinitely terminated design; approximately 0.18 and 0.29 respectively [3]. Tradeoffs between both of these ratios were necessary as the required voltage and current ratios did not occur at the same point in the gate voltage sweep. Therefore, at 0.9GHz, the final gate bias of –1.85V was selected at the efficiency peak, as shown in Fig. 3.7.

3.4.2 The Final Optimised Design

Following the selection of the gate bias, the theoretical class-F^{-1} load impedances from Table-3.1 were optimised. In a first step the fundamental load impedance at the I_{gen}-plane was swept between 60Ω and 70Ω, in accordance to exercising approximately 1.2A (1.2 Amps) current swing at 28V drain bias. Once the optimum fundamental impedance was determined the phase of the second harmonic was swept by ±10° of the figure in Table-3.1 to compensate for any small errors in the approximated package model. The same sweeping principle was then applied to the third harmonic phase, with the resulting optimised impedance values at the I_{gen}-plane are given in Table-3.2.

Frequency	$I_{gen.}$-Plane	Package-Plane
f_0	0.14 ∠ 0°	0.27 ∠ 86°
$2f_0$	1 ∠ -6°	1 ∠ 91°
$3f_0$	1 ∠ -174°	1 ∠ -142°

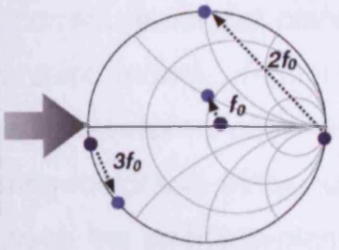

Table-3.2. Optimum terminations for Vds=28V at 0.9GHz.

With optimised performance in place, it remained for the device operation to be verified as the intended class-F^{-1} mode. The following section describes this process making further use of the RF waveform measurement and analysis capability available.

3.5 Performance Analysis of Achieved Device Operation

3.5.1 General Analysis of Emulated Performance

A power sweep was conducted with the optimised gate bias, fundamental load and 2nd and 3rd harmonic impedances in place. The results of this power sweep characterisation at 0.9GHz are shown in Fig. 3.8. The maximum efficiency achieved was 81.5%, at a total gain compression of approximately –4dB, with measured fundamental output power of 40.9dBm.

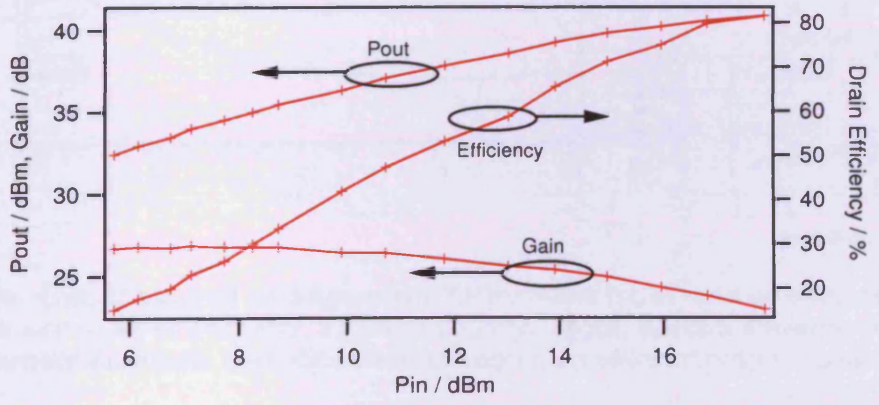

Fig. 3.8. Power sweep at 28V drain voltage bias condition at 0.9GHz.

All waveforms measured were imported into Agilent's ADS simulation

environment [14] and were de-embedded to the current generator plane using the previously described device output parasitic model. Fig. 3.9 shows the de-embedded output current and voltage waveforms obtained at a number of drive levels, including that delivering maximum efficiency of 81.5%. Fig. 3.10 shows the comparison between the package-plane and de-embedded $I_{gen.}$-plane RF load-lines.

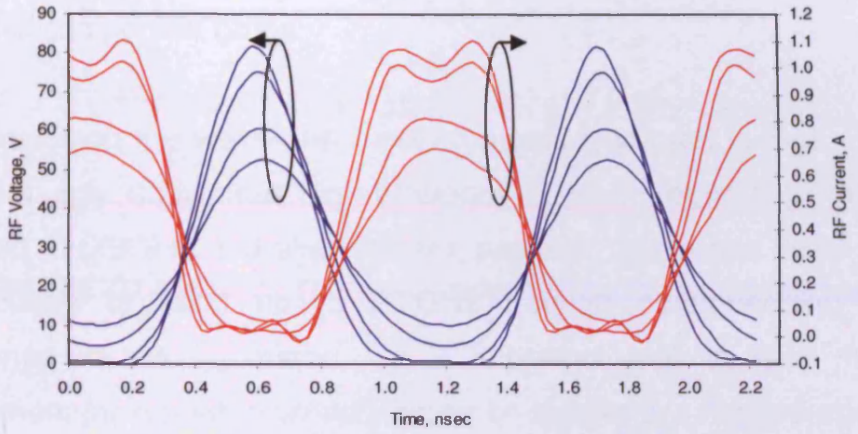

Fig. 3.9. Left: Measured RF waveforms, including at peak 81.5% efficient operation, de-embedded to the $I_{gen.}$-plane at Vds=28V and 0.9GHz.

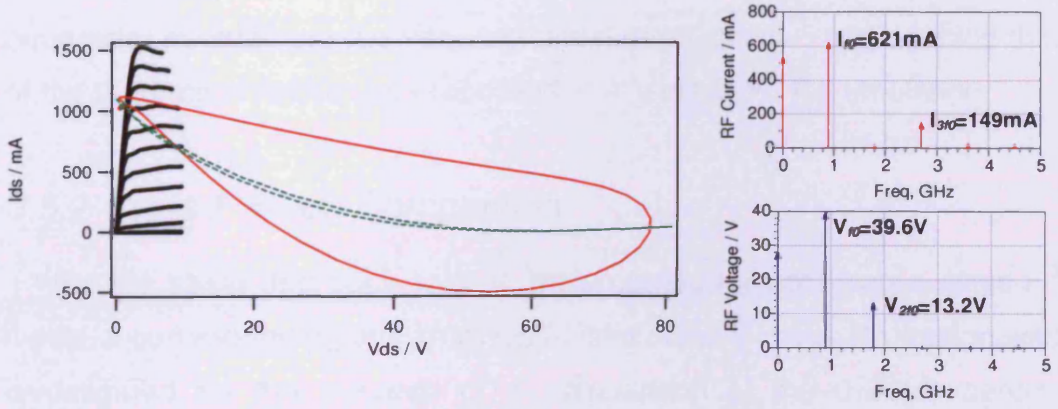

Fig. 3.10. Left: Measured package-plane RF load-line (solid) and de-embedded RF load-line (dotted) at Vds=28V, 81.5% efficiency. Right: Spectra showing voltage and current harmonic components in the optimum efficient output waveforms.

Observing the harmonic components present in the output voltage and current waveforms from Figs. 3.9 and 3.10, the final ratios of second

harmonic voltage-to-fundamental voltage, and third harmonic current-to-fundamental current are;

13.2V / 39.6V = ***0.33*** and *149mA / 621mA* = ***0.24***, respectively.

Although slightly higher, these ratios correspond relatively closely to the desired values of 0.29 and 0.18 respectively; while a second cycle of this design loop would realistically be able to achieve further improved harmonic component ratios.

In conclusion the waveform measurements, captured in Figs. 3.9 and 3.10, not only show that high-efficiency class-F^{-1} operation has been achieved at 0.9GHz, but also that the package model has been verified as accurate at least up to 2.7GHz through de-embedding of the waveforms to the $I_{gen.}$-plane. It is important also to note that any requirement for repeated design cycles or iterations, as stated above, do not require the costly build and test of any PA hardware since the PA emulation can be 'tuned' repeatedly through the measurement system's active load and bias control. In this case, however, just one cycle was necessary in obtaining the very high level of efficiency - approaching that of the theoretical maximum - recorded in this class-F^{-1} PA emulation.

3.5.2 Class-F Mode Comparison

With the same approach to that implemented for obtaining a class-F^{-1} mode, a corresponding efficiency-optimised class-F mode PA design was investigated for the purpose of a comparison at the 0.9GHz centre-frequency. The theoretical and final optimum harmonic reflection coefficients for this design are listed in Table-3.3.

Frequency	*Ideal Class-F reflection coefficient at $I_{gen.}$-plane*	*Ideal reflection coefficient at package-plane for f_0=0.9GHz*	*Optimum reflection coefficient for best efficiency ($I_{gen.}$-plane)*
$2f_0$	$1\angle 180°$ (short)	$1\angle -160°$	$1\angle -170°$ (174°)
$3f_0$	$1\angle 0°$ (open)	$1\angle 124°$	$1\angle 116°$ (-9°)

Table-3.3. Class-F terminations at current generator & package planes for 28V drain voltage at 0.9GHz.

Following optimisation of the gate bias voltage (set to –3.4V) in order to null the most significant odd-harmonic components in the output current waveform, and thus keep efficiency at a maximum, the fundamental load was tuned to 49Ω ($I_{gen.}$-plane). Results of this three-harmonic optimised design are shown in a power sweep in Fig. 3.11, while peak efficient de-embedded output waveforms are shown in Fig. 3.12.

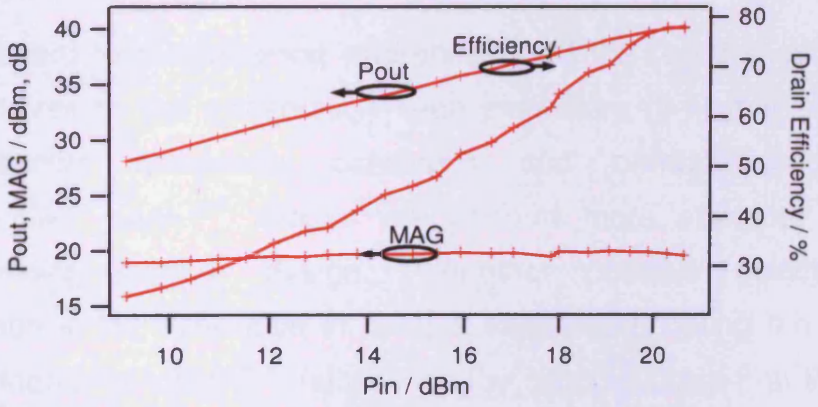

Fig. 3.11. Optimised class-F PA design power sweep at 0.9GHz.

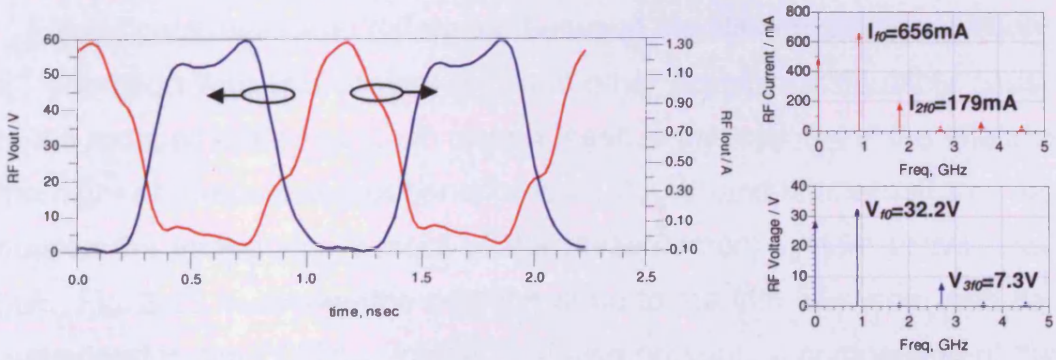

Fig. 3.12. Left: De-embedded output RF waveforms for optimum efficient class-F-mode PA design at 0.9GHz. Right: Spectra showing voltage and current harmonic components in the optimum efficient output waveforms.

The results show a peak measured efficiency of 77.7% in this approximated class-F-mode, which has been confirmed through the time domain waveforms, as well as the spectral analysis of the de-embedded output current and voltage, as in Fig. 3.11, which indicate third-to-fundamental voltage, and second-to-fundamental current component ratios of 0.23 and 0.27 respectively. The results show a moderate reduction in peak measured efficiency to that of the optimised class-F^{-1}-mode design of 81.5%.

Although only a relatively small difference, the 3-4% reduction in peak efficiency observed in this class-F mode emulation, compared to that of the optimised class-F^{-1} design, can be attributed to several device-related and also system-related factors.

With regard to the following references [3-4] the result shown in this work adheres to the observation seen elsewhere [3-4] that under the same limited bandwidth conditions and on-resistance device characteristic, class-F^{-1} modes will perform more efficiently than a corresponding class-F design. Another possible device-related explanation is the difference in relative ease in fabricating the short at third harmonic for class-F^{-1}, rather than the open for class-F at the same harmonic as a result of the influential and relatively high C_{ds} in GaN.

A significant measured difference between the class-F mode and class-F^{-1} operation with this device, and one other possible attributable cause to the reduced performance in class-F seen in this section, is the effect of the higher harmonic components present (fourth and fifth terms) that are outside the impedance control of the measurement system active load-pull. Fig. 3.13 illustrates the position of up to the fifth harmonic load de-embedded to the DUT $I_{gen.}$-plane, and also presents a comparison of the harmonic currents as a ratio of the fundamental component. Importantly,

a key difference between the class-F^{-1} and class-F current spectra is the size of the fourth and fifth harmonic ratios. As seen in Fig. 3.13, the fourth harmonic ratio present in the class-F output current waveform is two-and-a-half times larger than that in the class-F^{-1} waveform, and a similarly greater fifth harmonic current ratio. Although, with regards to the fourth harmonic, the magnitude ratio is more approaching that required by theory, it is the incorrect phase of this component that in fact leads to the detriment in efficiency, and the 'misshapen' output current waveform, away from the required half-wave sinusoid, seen in Fig. 3.12.

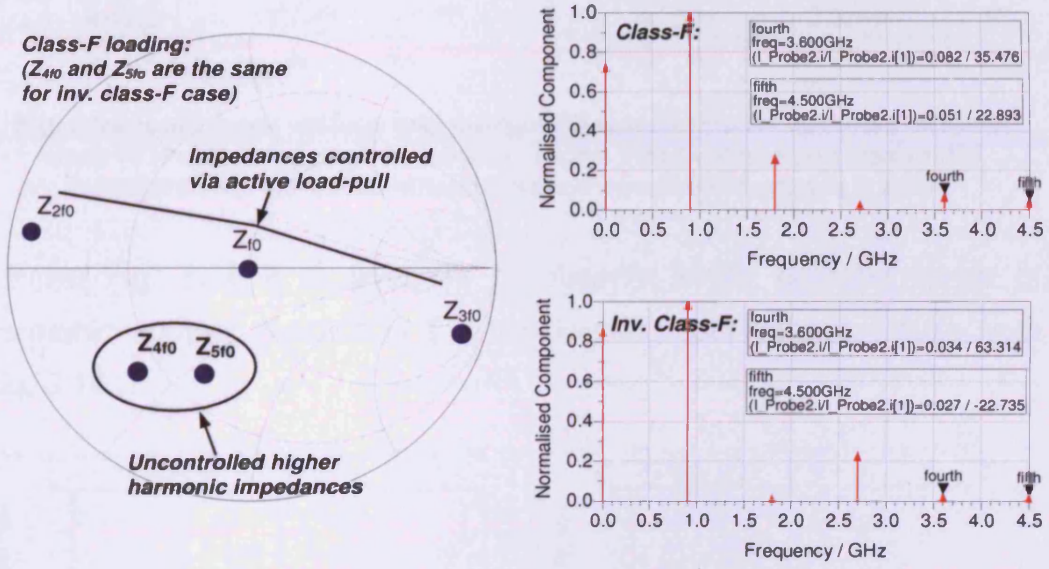

Fig. 3.13. Left: Impedance plane indicating the class-F 3-harmonic loading, and uncontrolled 4th and 5th harmonic impedances. Right: (Top) Output current ratio spectrum for optimised class-F case and (lower) class-F^{-1} case.

Since the fourth and fifth harmonic load impedances are outside of the active load control of the measurement system, without passively tuning, or extending the active load-pull loop to cover five harmonics, the performance within this class-F mode in this device is limited to that obtained here. Thus in this design example the class-F^{-1} mode of operation under three-harmonic load optimisation shows better efficient performance.

The higher harmonic problems can also be further attributed to the varying harmonic content generated at the input of the device as a function of the gate voltage being applied - a result present and noticed with this specific GaN device technology. Fig. 3.14 shows two sets of input waveforms captured from the optimised class-F^{-1} and class-F modes at several drive levels.

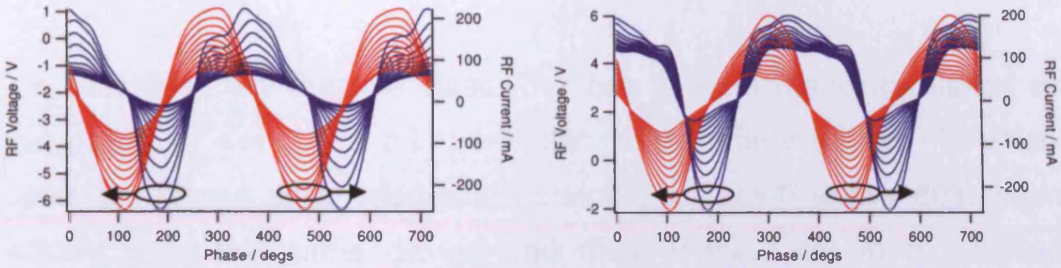

Fig. 3.14. Left: Input voltage and current RF waveforms for optimum efficient class-F^{-1}-mode PA design at 0.9GHz. Right: Input voltage and current RF waveforms for optimum efficient class-F-mode PA design at 0.9GHz.

From Fig. 3.15 it is possible to observe subtly different levels of harmonic content present in the two largest input voltage waves from Fig. 3.14.

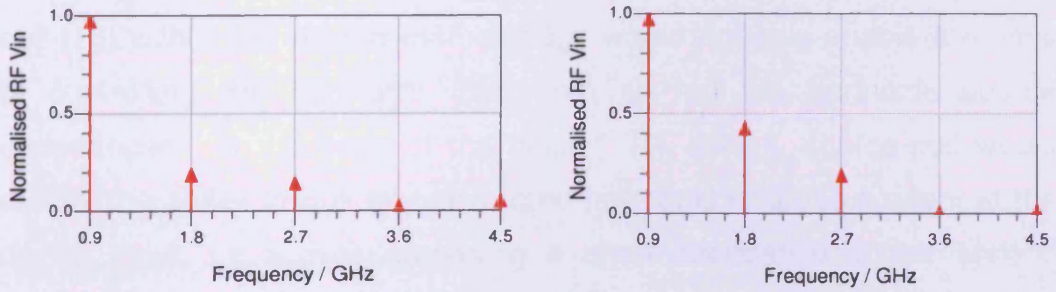

Fig. 3.15. Left: Input voltage spectrum for optimum efficient class-F^{-1}-mode PA design at 0.9GHz. Right: Input voltage spectrum for optimum efficient class-F-mode PA design at 0.9GHz.

As Fig. 3.15 shows, there is a much larger second harmonic component present in the input voltage wave in the class-F mode compared to that in the class-F^{-1} mode. It could be argued that this would help facilitate generation of more of the favourable second-

harmonic component in the class-F output current waveform. However, it is perhaps more likely that this has led to an overall incorrect proportion of second harmonic output current, and potentially additional unwanted harmonic terms within the output current wave - such as Fig. 3.13 indicates, in the form of a non-zero fifth harmonic output current term. This would then lead to the miss-shaped and reduced-efficient output current and voltage waveforms observed in this mode (Fig. 3.12).

It becomes clear that the class-F^{-1} mode is more readily facilitated by this particular device on this particular measurement set-up. To overcome the issues associated with obtaining a class-F above 80% drain efficiency on the same device and measurement set-up a modified measurement process could be implemented in the form of harmonic source-pull [15]. Since up until now the DUT input is set in an approximate 50Ω broadband impedance environment, harmonic voltage components induced at the device input will be developed across the source in an uncontrollable fashion.

Although not carried out here, the additional implementation of source-pull [15] within this design methodology would not only enable a means of controlling the harmonic loads but so too the harmonic source impedances. In the case of the class-F PA design, source-pull would enable the ability to null any unwanted harmonic voltages present at the device input, by actively providing a short impedance at the second harmonic, thus further optimising the overall PA design emulation achieved as a result.

3.6 Scaling the High-Efficiency PA Design Methodology

3.6.1 High-Efficiency Design at 2.1GHz

With the successful waveform optimisation for class-F^{-1} at 0.9GHz

completed, performance scalability to higher frequencies was investigated. For this purpose the entire design procedure was repeated at 2.1GHz with the same GaN DUT. This time the initial gate voltage bias sweep delivered an optimum of V_{gs}= –2.5V in generating the appropriate harmonic-to-fundamental component ratios.

However, after applying the predicted load impedances from Table-3.1 at the fundamental frequency of 2.1GHz, the resulting power sweep showed a disappointing 69.3% drain efficiency was obtained with 40.9dBm fundamental output power at 28V drain voltage. To gain a further efficiency-optimised performance, the phases of the harmonic loads were now swept across a wider range than the previous ±10°, with the aim of obtaining an optimum efficient mode of operation. Following this second optimisation of the harmonic impedances a high density sweep of the fundamental load was conducted resulting in an optimised $I_{gen.}$-plane fundamental load with a more substantial reactive offset. The final optimised package-plane and de-embedded harmonic loads are listed in Table-3.4 for a drain voltage bias condition of 28V. Utilising these values, and with a 28V drain voltage, a power sweep was conducted, the results of which are displayed in Fig. 3.16 indicating a maximum drain efficiency of 82.3% having been achieved (Fig. 3.17).

Frequency	*$I_{gen.}$-Plane*	*Package-Plane*
f_0	*0.14 ∠ 39°*	*0.52 ∠ 129°*
$2f_0$	*1 ∠ -75°*	*1 ∠ 129°*
$3f_0$	*1 ∠ -170°*	*1 ∠ -69°*

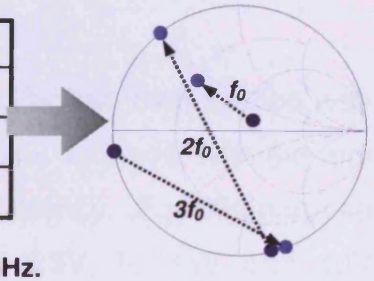

Table-3.4. Optimum terminations for Vds=28V at 2.1GHz.

Although a question remains over the mode of operation that has been obtained here in this efficiency-optimised 2.1GHz PA design - reasons for this to be discussed in *Section 3.6.3* - the procedure has indicated good

scalability from 0.9GHz to 2.1GHz. Peak efficiencies above 80%, whilst operating above 10W fundamental output power, have been achieved in both optimised design emulations.

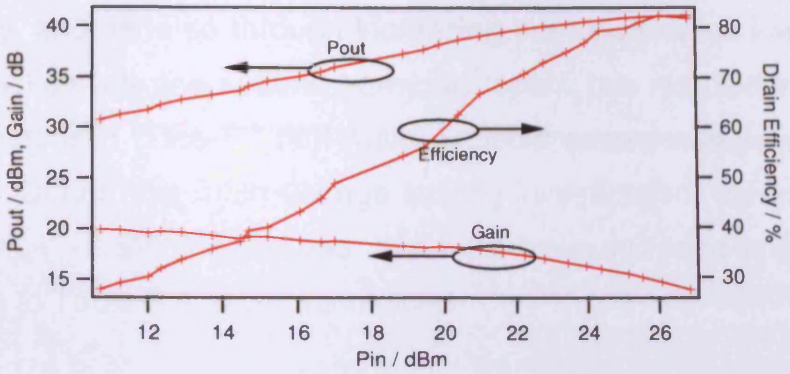

Fig. 3.16. Power sweep at 28V drain voltage bias condition at 2.1GHz

3.6.2 Scaling Performance with Increased Drain Voltage

The high voltage breakdown nature of the wide band-gap GaN device technology proves ideal in securing the very high voltage swings required for high power class-F^{-1} operation [5]. This combined with the very low knee-voltage offset, also inherent with this GaN HEMT device technology, offers the possibility of reaching very high levels of drain efficiency whilst operating at these high power levels. This is, however, providing that the effect of any 'knee-walkout' behaviour, occurring as a result of increasing V_{ds}, is kept to a minimum [6].

With the design procedure scaled to 2.1GHz, further investigation was initiated on its scalability towards higher drain bias voltages, with the aim of further increasing peak achievable device efficiency. For this purpose the drain bias voltage was increased above 28V, to 35V and 40V respectively. 40V was the maximum limit of drain bias voltage tested on this device so as not to develop peak RF voltages beyond the drain-source breakdown condition of this GaN device.

The same GaN HEMT device (CGH40010F) was used, keeping output power and gain compression levels approximately constant for each of the DC drain voltage design cases. As the DC drain voltage was increased, an appropriate reduction in the output current swing was necessary, and done so through increasing the fundamental load. Thus, in combination with the second harmonic 'open', this resulted in shaping the characteristic class-F^{-1} half-wave sinusoid output voltage waveform required. During this drain voltage scaling investigation, the same gate bias of V_{gs}= –2.5V and second and third harmonic load impedances, according to Table-3.4, were maintained.

The obtained results at a 35V drain voltage bias condition saw the drain efficiency improve up to 82.8% whilst with a 40V bias condition 84.0% drain efficiency was measured.

3.6.3 Conclusions on Scalability of the Presented Methodology

Fig. 3.17*(a)* shows the de-embedded output current and voltage waveforms present at the approximated I_{gen}-plane at maximum drain efficiency of 82.3% at V_{ds}=28V. As is seen in Fig. 3.18*(a)*&*(b)* and 3.19*(a)*&*(b)*, with decreasing current swing the de-embedded current and voltage waveforms were beginning to extend beyond the defined DC-IV boundaries of the device. This was due to the inaccuracies in the package model becoming more apparent at the higher harmonic operating frequencies, as well as the increased effects from the weakly nonlinear output capacitance. Nevertheless, these de-embedded waveforms are still effectively indicating the performance of the device at the $I_{gen.}$-plane. As can be seen from Fig. 3.17*(a)*, the de-embedded voltage waveform maintains the half-rectified sinusoid indicative of class-F^{-1}. However, squaring of the current waveform is also indicated in the de-embedded output current waveform, but to a lesser extent. The

same measurements and analysis were made for the 35V and 40V drain voltage conditions showing almost ideal voltage waveforms, but continuously diverging current waveforms away from the ideal (Fig. 3.18*(a)*&*(b)* and 3.19*(a)*&*(b)*).

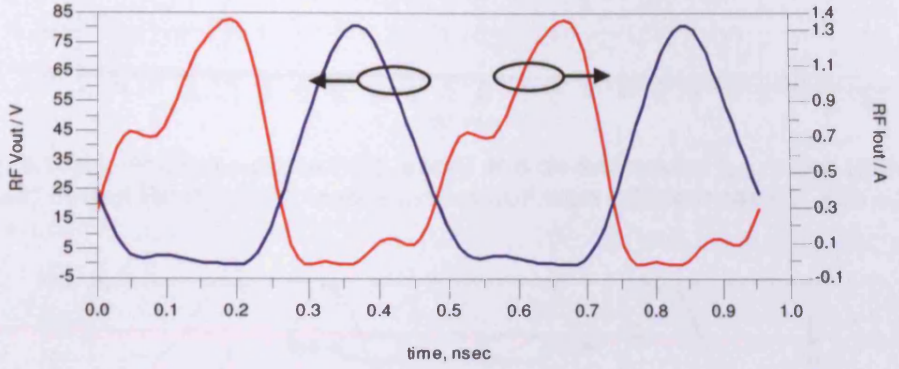

Fig. 3.17*(a)*. De-embedded output RF waveforms for optimum efficient case at Vds = 28V (82.3%)

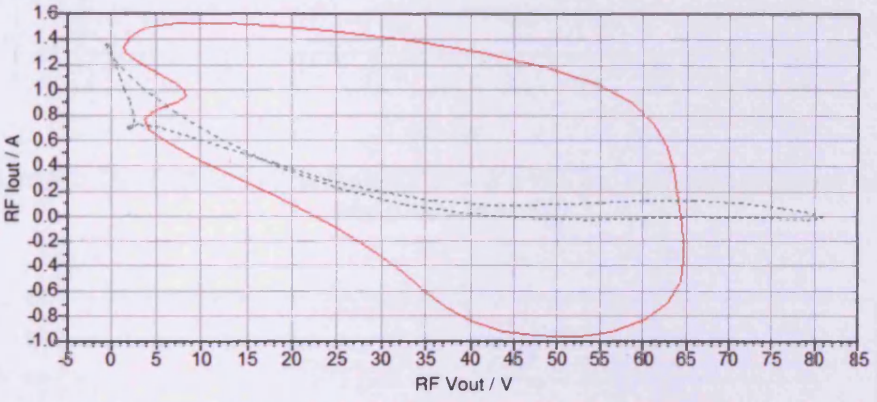

Fig. 3.17*(b)*. Package-plane (red, solid) and de-embedded $I_{gen.}$-plane (green, dotted) output RF dynamic load-lines for optimum efficient case at Vds = 28V.

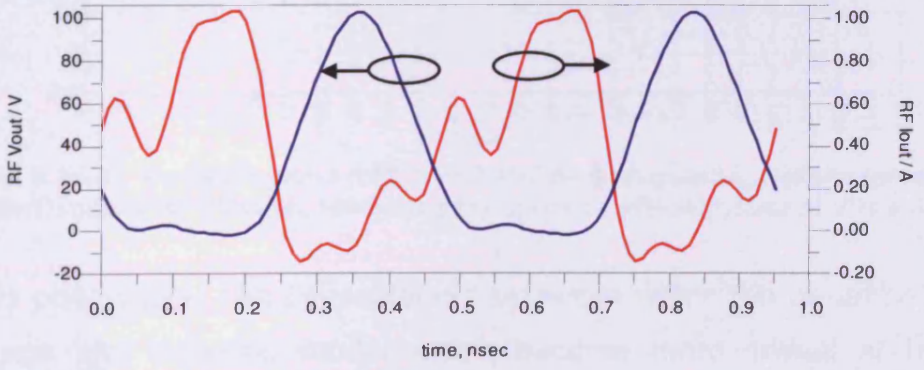

Fig. 3.18*(a)*. De-embedded output RF waveforms for optimum efficient case at Vds = 35V (82.8%).

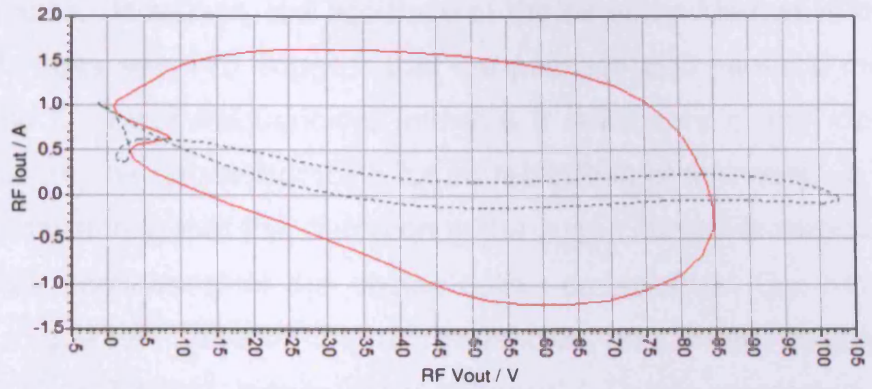

Fig. 3.18*(b)*. Package-plane (red, solid) and de-embedded $I_{gen.}$-plane (green, dotted) output RF dynamic load-lines for optimum efficient case at Vds = 35V.

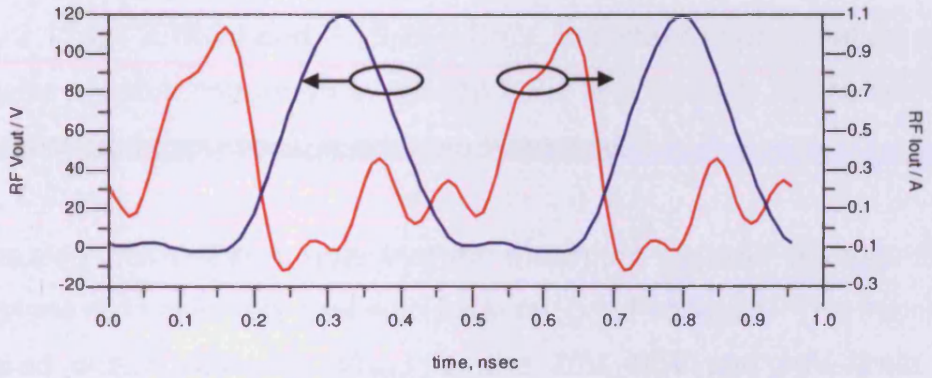

Fig. 3.19*(a)*. De-embedded output RF waveforms for optimum efficient case at Vds = 40V (84.0%).

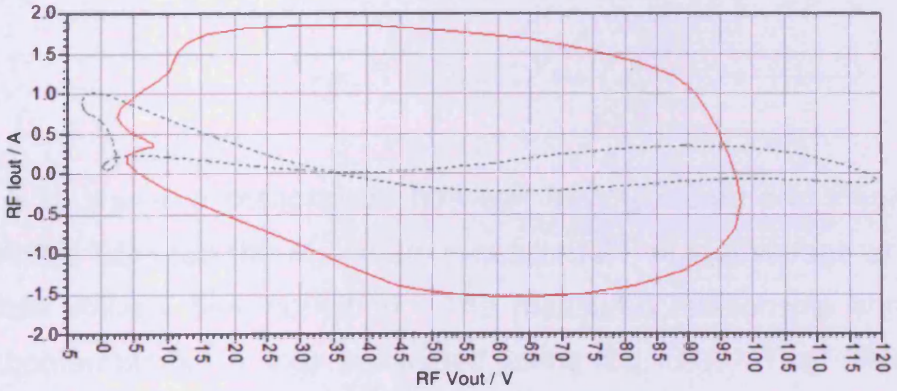

Fig. 3.19*(b)*. Package-plane (red, solid) and de-embedded $I_{gen.}$-plane (green, dotted) output RF dynamic load-lines for optimum efficient case at Vds = 40V.

This observation can be explained by errors within the de-embedding package and parasitic model which become more critical at higher

frequencies. However, the accuracy of the de-embedded waveforms at 0.9GHz does seem to suggest that the package and parasitic model is accurate for lower frequencies, and that a refinement of the model for 2.1GHz may be necessary for a future replication of this work. It is also worth considering that the distortion in the output current is introduced by the slight nonlinearity of the device output capacitance, C_{ds}, having an increasing effect towards higher freqencies and, more notably from Figs. 3.17*(a)*-3.19*(a)*, higher drain voltages. This is supported by the observed increase in current distortion as V_{ds} increases, which is also visible in the increased 'looping' of the RF dynamic load-line in each of Figs. 3.17*(b)*, 3.18*(b)* and 3.19*(b)*. Thus, the linear approximation of the parasitic network described in section 3.3.2 is potentially not sufficient as frequency and drain voltage are both increased.

It is also interesting to note that the maximum incurred voltages at the $I_{gen.}$-plane did scale very well with increasing rail voltages. The maximum incurred output voltages ($V_{max.}$) for the 28V, 35V and 40V drain bias conditions are 82V, 102V and 121V respectively, and very closely replicate the theoretical values for class-F^{-1} obtained from Eq. 3.3 below.

$$V_{\max.} = \pi \cdot (V_{DC} - V_{knee}) \qquad (3.3)$$

Fig. 3.20 shows a comparison between the measured and theoretical relationship between the maximum measured RF output voltage and the DC drain voltage bias condition. The measured relationship shows a good conformance to that calculated using Eq. 3.3. The difference between the theoretical and measured $V_{max.}$, (approximately 3V observable in Fig. 3.20 at each drain bias voltage) can be accounted for by the smaller fundamental-to-second-harmonic voltage ratio being implemented due to trade-offs in the gate bias voltage chosen, as well as the maximally-flat ratio being applied in the first instance.

Conclusively, the utilised GaN technology did not indicate any onset of RF drain-source breakdown up to 121V. Furthermore, the very high efficiencies obtained in this study, particularly observed in the Class-F^{-1} cases (e.g. Fig. 3.9), are achieved at a high extent of measured gain "compression" (between 4 to 5dB reduced gain from that of the device small-signal gain). It is important to stress that since such a level of device "compression" is not observed as extensive clipping in the measured waveforms of Fig. 3.9, the cause of the reduced power gain from that seen at small signal can perhaps be attributed more to the tangential-shaped transfer characteristic of the real device. This would lead to distortion of the output waveforms - and thus device gain reduction - long before any waveform clipping is observed. Hence the efficiencies measured in this work are deemed a result of the implemented waveform engineering process and not merely the result of a highly-compressed/clipped device 'mode'.

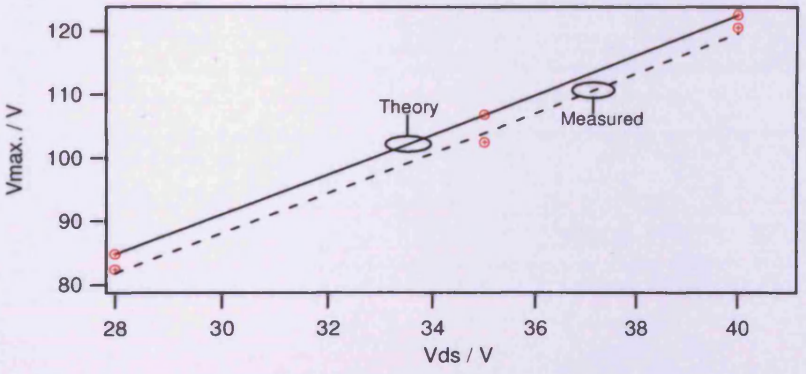

Fig. 3.20. Measured and theoretical peak output voltage at $I_{gen.}$-plane.

In any case, even under such reduced gain levels, the device utilised continues to operate very efficiently and at gain levels of 14dB and above. Consequently, PAE is lower only by 0.5 to 3.5% compared to drain efficiency across all optimised efficiency conditions detailed in this chapter of work. The high gain of this GaN device lends itself very well to this high-efficiency application.

3.7 Chapter Summary

The procedures described in this chapter, to obtain very high-efficiency performance from a GaN HEMT, show a systematic methodology in which maximum achievable practical efficiencies of a class-F^{-1} amplifier topology are obtained and analysed at 0.9GHz. At 2.1GHz the uncontrolled measurement system harmonic impedances conspire to prevent class-F^{-1} operation from being achieved, and instead another high-efficiency mode is obtained. This performance was shown and verified through the combination of high-power waveform measurements and device package de-embedding, whilst also analysing how increased DC drain bias voltage can lead to further improved record efficiencies, and the output voltage scaling as defined in the half rectification of the output voltage waveform.

3.8 References

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Chapter 4. Use of Optimised Waveform Measurement Data for PA Prototyping

4.1 Introduction

Equation-based device models are now widely used in PA designs which are subject or prone to nonlinear device operation [1-5]. With this brings the heavy reliance upon the accuracy of such models. The consistent flow of new generation device technologies leads to the on-going requirement for corresponding nonlinear device models. The time required for a PA design developed in a CAD environment to be realised as a working PA prototype can often succumb to several iterations of the realised matching networks to account for the errors in newly-emerged device models.

The waveform-engineering-based efficiency-optimisation methodology detailed in **Chapter 3**, has already demonstrated a GaN HEMT device operating very close to maximum theoretical levels of efficiency, with the device non-idealities[5] taken into account. Several attempts of performance-optimised PA designs have now been emulated thus far, using waveform-engineering practices [6-8]. However none as yet have been followed through and translated directly to a realised PA prototype using only the waveform measurement data obtained during the

[5] Non-Idealities: The characteristics of real devices which lead to, for example, the divergence of the output DC characteristic away from the 'ideal'.

emulation stage as design parameters. Thus, this chapter aims to develop and follow through a methodology - with the objective of utilising the captured measurement data from the load-pull emulation of the high-efficiency modes described in **Chapter 3** - and enable a direct and rapid approach in realising input and output matching networks for a working prototype PA.

CAD tools have been utilised in the design and realisation of the passive input and output PA networks, but importantly, and key to this section of work, without the use of a nonlinear device model for the GaN HEMT. Instead, a generic microstrip matching network architecture implemented in a previous class-F^{-1} amplifier design [5, 9], has been adapted in order to present the required fundamental, second and third harmonic load impedances specific to the PA designs emulated in **Chapter 3** [8]. These matching network designs have been carried out with reference to the calibrated (and measured) package-plane waveform and impedance data. However, consideration of the waveforms that exist and impedances presented at the $I_{gen.}$-plane was also crucial in verifying the PA mode of operation being implemented.

The microstrip layout and prototyping stages of these PA designs were initiated through utilisation of the emulated class-F^{-1} PA measurements detailed in **Chapter 3**, firstly at 0.9GHz and then also at 2.1GHz. Working at a fixed drain bias voltage of 28V, the optimum emulated performance in this design saw an output fundamental power of 12W and drain efficiency of 81.5% for the 0.9GHz PA design [8]. The result of the work detailed in this chapter has demonstrated two very high-efficiency working prototype PAs at centre frequencies of 0.9GHz and 2.1GHz respectively, importantly, with the PAs' performances exhibiting very close agreement to the load-pull emulated designs.

4.2 Use of Measurement Data and CAD for PA Prototyping

4.2.1 Collating the required harmonic impedance environment information

Since the design, performance-optimisation and nonlinear analysis has been all been carried out during the waveform-engineering stage (**Chapter 3**), the obvious next step in this novel PA development cycle was to collate all of the performance variables from the obtained dataset. From this measured device dataset, a translation from the load-pull emulated impedance environment to a realisable passive matching network could be initiated. The objective was to realise a PA that would replicate the exact same high performance mode that was initially emulated on the GaN HEMT device using active harmonic load-pull. CAD tools would be utilised in the network design and realisation process, although exclusively without the use of a nonlinear device model for the GaN HEMT.

Frequency Domain Data
Optimum Power Sweep

Carrier Freq. (GHz)	0.9
No. of Harmonics	5
Pin (dBm)	17.93
Pout (dBm)	40.88
Gain (dB)	22.95
Efficiency (%)	81.53

DUT performance measures

Load reflection coefficients required to obtain above performance

Harm.	Gam. Ld. Mag	Gam. Ld. Phase	Pout (dBm)	v1 Mag (V)	v1 Phase (degs)	i1 Mag (mA)	i1 Phase (degs)	v2 Mag (V)	v2 Phase (degs)	i2 Mag (mA)	i2 Phase (degs)	Gam. Src. Mag	Gam. Src. Phase
0	-	-	-	-1.80	0.0	0.0	180.0	27.98	0.0	536.8	0.0	-	-
1	0.27	86.1	40.88	2.36	0.0	251.9	77.9	38.26	163.8	739.5	-46.2	0.93	-159.2
2	1.00	90.8	-	0.50	171.9	13.8	14.8	11.64	-19.3	236.1	70.7	0.26	-129.7
3	1.00	-138.7	-	0.40	-34.4	5.4	145.2	2.28	-133.3	120.9	137.8	0.20	0.7
4	0.11	-57.3	4.49	0.11	-82.3	4.1	77.7	0.57	151.7	10.0	-17.1	0.34	152.1
5	0.41	143.5	5.36	0.18	101.4	5.8	-52.2	0.46	64.8	17.3	-145.4	0.33	-137.4

Fig. 4.1. Frequency-domain dataset for the optimised class-F^{-1} design at 0.9GHz fundamental frequency.

A frequency-domain dataset obtained at a specific optimum emulated device condition is shown in Fig. 4.1. This figure indicates the key device

parameter values which have culminated in the highly efficient, class-F^{-1} device operation achieved at a 0.9GHz fundamental frequency, as described in **Chapter 3**. All data corresponds to the calibrated measurement reference plane at the DUT package.

Table 4.1 summarises the key load reflection coefficients (fundamental, and second and third harmonics), pulled from the optimised parameters shown in Fig. 4.1. The target for the proposed passive matching network was to replicate these multi-harmonic loading criteria, and thus satisfy the corresponding $I_{gen.}$-plane reflection coefficients defined by PA mode theory for class-F^{-1} operation [10]. The specific $I_{gen.}$-plane impedance values for this example have also been obtained by de-embedding the device output parasitics from the optimised package-plane loads, providing a further means of verification of the mode obtained in this design case.

Harmonic Component	*Package-Plane ρ @0.9GHz*	*Approx. $I_{gen.}$-Plane ρ*
f_0	$0.27 \angle 86°$	$0.14 \angle 0°$
$2f_0$	$1 \angle 91°$	$1 \angle -6°$
$3f_0$	$1 \angle -139°$	$1 \angle -174°$

Table 4.1. Optimum terminations found through waveform-engineering [8].

Table 4.2 summarises some of the other key performance parameters measured from the class-F^{-1} emulation on the 10W GaN device.

Again, it is important to mention that the objective of the PA output network realisation was to replicate the fundamental and second and third harmonic load reflection coefficients measured at the optimum-efficient performance during the waveform-engineering process.

Optimised Inverse Class-F Performance – Waveform Measurements	
Frequency:	***0.9GHz*** *fundamental frequency with second and third harmonics optimised.*
Drain Voltage:	***28V*** *set at the device drain tab (consistent for all drive conditions).*
Gate Voltage:	*Gate bias set to approx.* ***-1.8V*** *ensuring* I_{dsq} *(quiescent drain current) of* ***420mA*** *(mid A/B bias point).*
Power:	*Device* ***P3dB*** *output power of approximately* ***12W****.*
Gain:	*Maximum available stable small signal device gain measured as approx.* ***27dB****.* ***22.9dB*** *power gain measured at optimum efficiency.*
Efficiency:	*Maximum drain efficiency of* ***81.5%*** *measured at* ***12.5W*** *output power.*

Table 4.2. Performance summary; optimum 0.9GHz class-F^{-1} emulation [8].

Similarly, the input network design would focus on obtaining large gain at 0.9GHz (in order to translate the high drain efficiency to high PAE - power-added efficiency). This would involve matching to the optimum device input impedance ($Z_{in.opt}$), which was also captured during the emulation stage, while also considering device stability across all frequencies. Bias networks would also be implemented to obtain a fully functional stand-alone PA with emphasis on a 'right-first-time' design.

4.2.2 Applying optimum impedance environment to device manufacturer's model in CAD

An important stage of this design was to develop a means of comparing the performance obtained from the waveform-engineered DUT with not only theoretical predictions (as in **Chapter 3**) but also with the commercially-available, PA designer's nonlinear device model from the manufacturer. The aim of this latter comparison was to set the device model in Agilent's ADS CAD environment in the same quiescent bias state and terminated up to the fifth harmonic impedance conditions as set at the source and load on the emulated set-up at 0.9GHz. With these conditions set, a sweep of P_{in} (power-in) can be made.

It is important to note that the use of the nonlinear CAD model was in

no way implemented in the design of the PA matching networks that follows in this chapter, but merely as a tool for comparison with the load-pull emulation design strategy. Fig. 4.2 highlights the ADS schematic that was set up to enable direct waveform and performance comparison of the NL (nonlinear) model with the originally emulated class-F^{-1} PA design results.

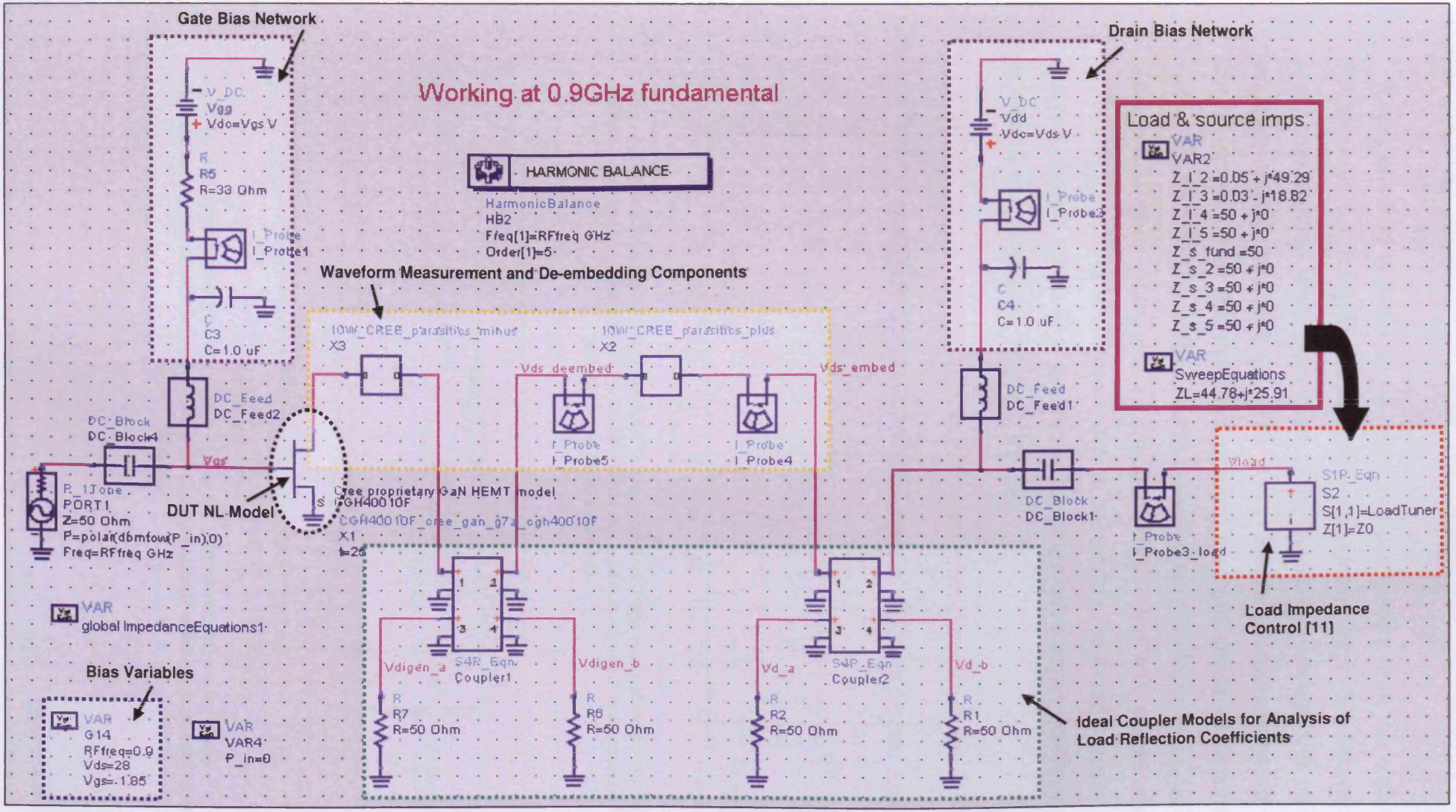

Fig. 4.2. ADS schematic implemented for comparison of emulated class-F^{-1} PA performance with NL device model;
The same quiescent bias condition and optimised 3-harmonic load impedances are set in this simulation, whilst the remaining load and source impedances are set to 50Ohms as was the condition during the waveform measurement emulation.

It was ensured that the same measured parameters from the class-F^{-1} PA emulation at 0.9GHz (Table 4.2) were adhered to in the simulation. Load impedances were controlled in the simulation through the use of equation-based variables in ADS [11]. Simulated waveforms of the device operation at the optimum efficient load-pull-emulated conditions were captured and de-embedded in the same way in which the $I_{gen.}$-plane waveforms were obtained in practice [12]. Fig. 4.3 shows these simulated $I_{gen.}$-plane waveforms with a comparison to those captured on the real device, whilst Fig. 4.4 shows a comparative power sweep of the emulated and simulated PA performance.

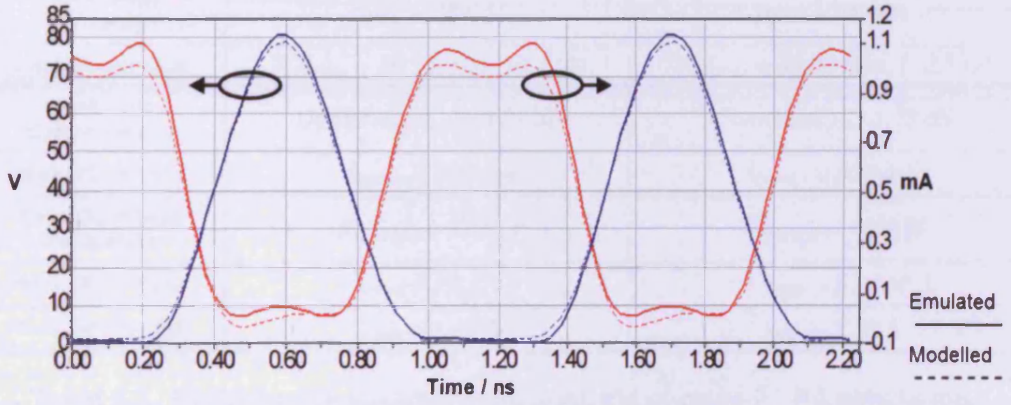

Fig. 4.3. Simulated $I_{gen.}$-plane output current and voltage waveforms from NL device model (dotted traces) overlaid with the optimised emulated class-F^{-1} waveforms (solid traces).

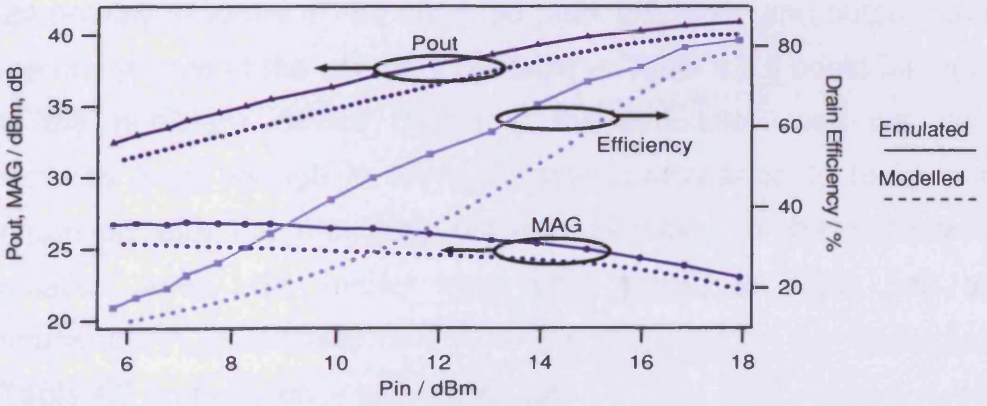

Fig. 4.4. Simulated power sweep of the NL device model under class-F^{-1} conditions (dotted traces) overlaid with the optimised emulated sweep (solid traces).

Making an overall comparison between the use of the NL device model in a CAD environment and the waveform-engineered PA emulation, there are some subtle differences in performance, those of which are also summarised in Table 4.3.

Inverse Class-F NL Device Performance – Simulation Analysis		
	Nonlinear Device Model Simulation	***Load-Pull PA Emulation***
Quiescent Drain Current:	I_{dsq} = 420 mA	I_{dsq} = 420 mA
Gate Bias Voltage:	V_{gs} = -1.824 V	V_{gs} = -1.850 V
Maximum Input RF Power to Device:	$P_{in.max}$ = 17.93 dBm	$P_{in.max}$ = 17.99 dBm
Peak Drain Efficiency:	μ_{drain} = 78.8 %	μ_{drain} = 81.5 %
Peak Power Out:	$P_{out.max}$ = 40.05dBm (10.1 W)	$P_{out.max}$ = 40.88 dBm (12.2 W)
Peak Gain Compression:	$Compress._{max.}$ = 3.31 dB	$Compress._{max.}$ 3.75 dB
Peak DC Current:	$I_{dc.max}$ = 460 mA	$I_{dc.max}$ = 537 mA
Peak DC Power Dissipation:	$P_{diss.max}$ = 12.8 W	$P_{diss.max}$ = 15.0 W
Peak RF Voltage:	v_{peak} = 78.1 V	v_{peak} = 81.1 V
Peak RF Current:	i_{peak} = 1.00 A	i_{peak} = 1.10 A

Table 4.3. Performance summary and analysis of class-F^{-1} PA simulation.

It becomes evident that the simulation performance results are consistently slightly less than that of the load-pull emulated PA design, most notably in terms of the obtained peak efficiency and output power. Upon first glance of the comparative table in Table 4.3 it could be argued that the nonlinear device model in the simulation was not driven sufficiently hard enough in terms of gain compression to make a fair comparison with the emulated results. However in this comparative simulation, even with further input drive power to onset 5dB gain compression P_{out} increases by only 0.1dB above that of the figure stated in Table 4.3 and efficiency just above 80%.

It can be concluded that although the device model simulation has yielded very high-efficient operation and approximate class-F^{-1}-shaped output waveforms, the most notable differences are the reduced peak figures that are predicted by the model from simulation. Important also is the dynamic drain efficiency shown in Fig. 4.4 which shows the simulation results, at certain drive levels, to be up to 20% reduced in efficiency from that of the emulated power sweep performance. The use of waveform-engineering has in fact revealed an improvement in peak output power of more than 0.8dB and almost 3% higher peak drain efficiency over that of the simulation results and therefore holds the advantage over this nonlinear device model in terms of PA performance prediction.

4.2.3 Setting the goals for the required passive matching network

A previously implemented output microstrip network architecture for an class-F^{-1} amplifier (Fig. 4.5) [5, 9] was chosen for this design. The purpose was to apply the architecture in order to design the required fundamental, second and third harmonic load impedances (listed in Table 4.1) that have been measured for the optimally efficient class-F^{-1} design during the waveform-engineering process. Designed appropriately, the matching architecture [5, 9] can provide precise open and short impedances at the second and third harmonic frequencies, which also tend approximately towards respective repetition at higher even and odd harmonic terms [5, 9]. Combined with de-embedding [12] involving modelling the package and output parasitics inherent to the 10W GaN device, the appropriate phases of the required package-plane harmonic load impedances can be designed using the precise approach detailed in [5, 9]. Although not a novel matching architecture in itself here, it is important to note that the key aspect of this work was to focus on the

direct translation of measurement data into a working PA prototype, and this class-F^{-1} matching architecture has been used to enable this translation.

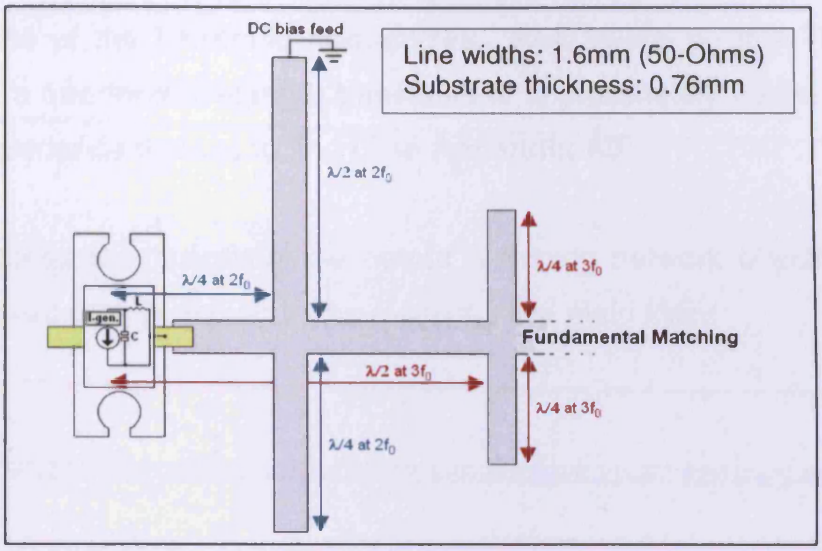

Fig. 4.5. The output microstrip network architecture implemented [5, 9].

While the fundamental and harmonic load impedances are dealt with by the matching architecture, the input matching is carried out using a less complex open stub match for best power gain and thus enhance PAE. The specific design processes of both the input and output matching structures is detailed further in the following section.

4.3 Right-First-Time Realisation of a Very High-Efficiency Complex PA

4.3.1 Implementation of CAD for Realisation – Output Multi-Harmonic Matching

Agilent's ADS CAD simulation environment has been utilised for the design of the high-efficiency class-F^{-1} PA input and output microstrip matching networks. By defining a microwave substrate in the design environment, the chosen laminate (Roger's TMM3®, of thickness

0.76mm) was modelled enabling an implementation of the output matching architecture shown in Fig. 4.5. This was achieved through a combination of microstrip lines, and quarter and half-wavelength stubs to provide the appropriate phase shifting and respective short and open terminations at the harmonic frequencies. At 0.9GHz, on this TMM3® substrate, a quarter-wavelength translates to approximately 25mm length of 50Ω impedance microstrip line (See **Appendix A5**).

The process for designing the output matching network directly from the measured data is shown in the following five main steps:

1. ***The required current generator-plane loads (Table 4.1) are rotated by the DUT output parasitics to the measured package-plane loads (Fig. 4.6) – These are the loads for which to design the external matching to.***

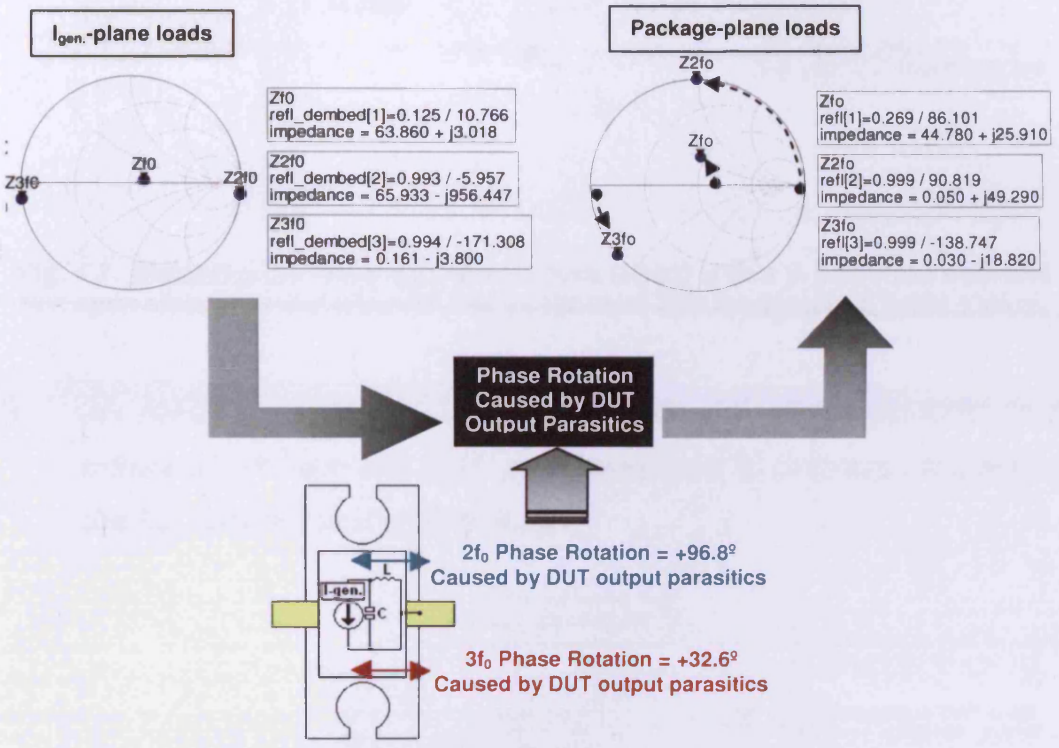

Fig. 4.6. The effect of the output parasitics on the desired optimum $I_{gen.}$-plane class-F^{-1} loading translation to the device package-plane.

2. ***Working back from the device package, we require a length of line that, when added to the parasitic-induced rotation of the second harmonic phase, will be a total of ¼λ (wavelength). A ½λ shorted stub (which also enables a route for DC bias introduction) and a ¼λ open stub both positioned at the end of the ¼λ line provide $2f_0$ with the required open circuit at the DUT $I_{gen.}$-plane (Fig. 4.7).***

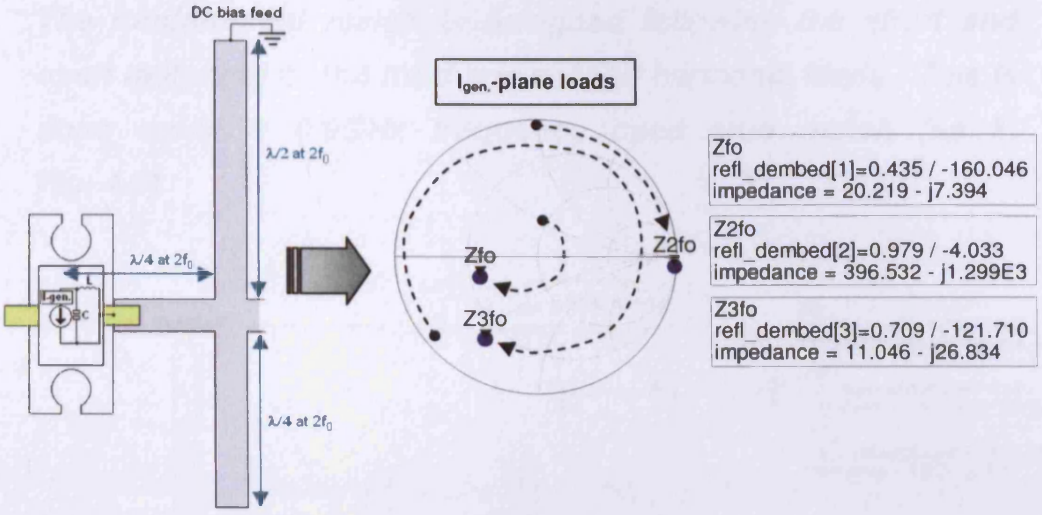

Fig. 4.7. Matching the second harmonic load (open) with a ½ λ shorted stub and ¼ λ open stub, with the effect of this on the third and fundamental loads shown.

3. ***$3f_0$ loading: Two open stubs positioned approximately ½ λ minus 32.6º from the DUT package-plane to provide an open at the $I_{gen.}$-plane for Z_{3f0} (Fig. 4.8).***

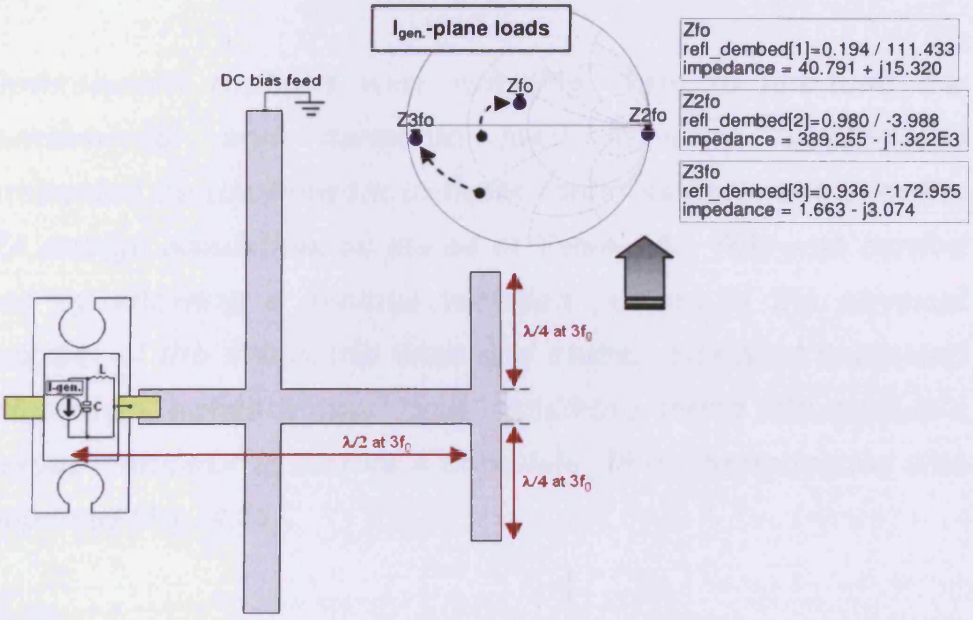

Fig. 4.8. Third (short) and second harmonic loads now matched with the addition of two ¼ λ open stubs. The effect of this on the fundamental load is also shown.

4. ***The fundamental match is designed following the short and open matching of the third and second harmonic loads. This is done using a 0.9GHz frequency open stub match (as in Fig. 4.9).***

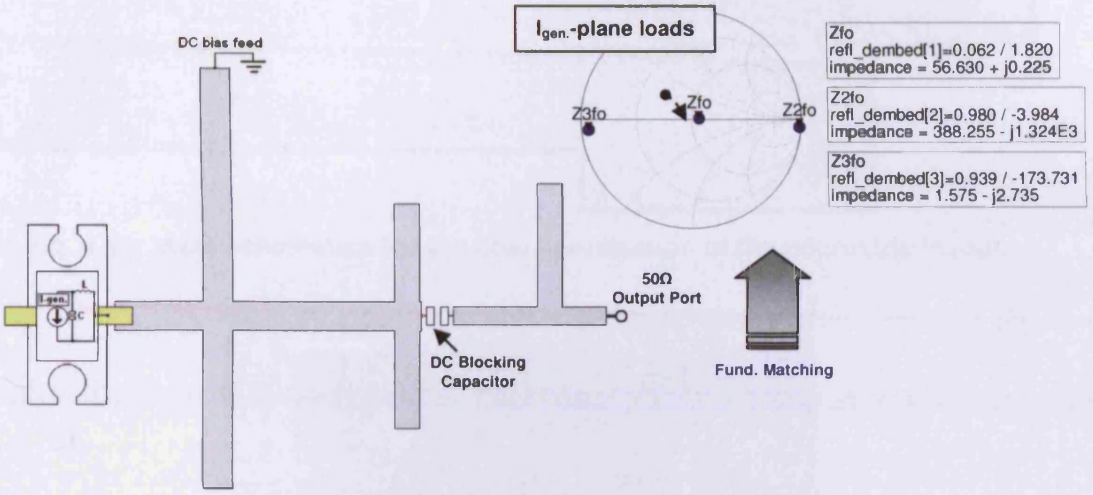

Fig. 4.9. Fundamental loading now completes the three harmonic matching network to approximately the impedances required.

5. ***Optimisation routines were run (Fig. 4.10) to fine-tune the fundamental and harmonic load reflection coefficients presented by the network to those found as optimum from the PA design emulation, as stated in Table 4.1. This was carried out by allowing a minimal variation (±5mm) in the physical lengths of the microstrip lines and stubs. The final optimised microstrip network was then simulated using Momentum's layout simulator to ensure a complete RF characterisation was obtained (Fig. 4.11).***

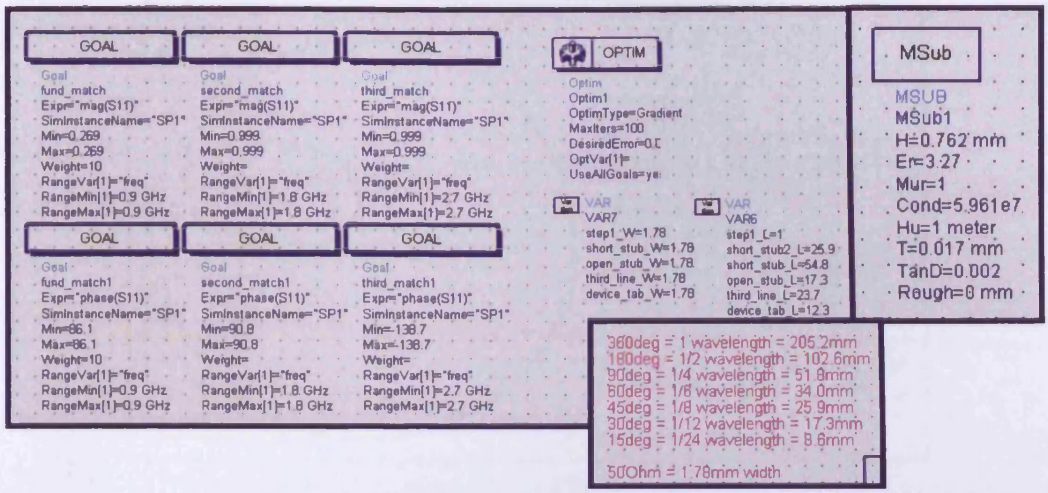

Fig. 4.10. ADS schematics for the final optimisation of the microstrip layout.

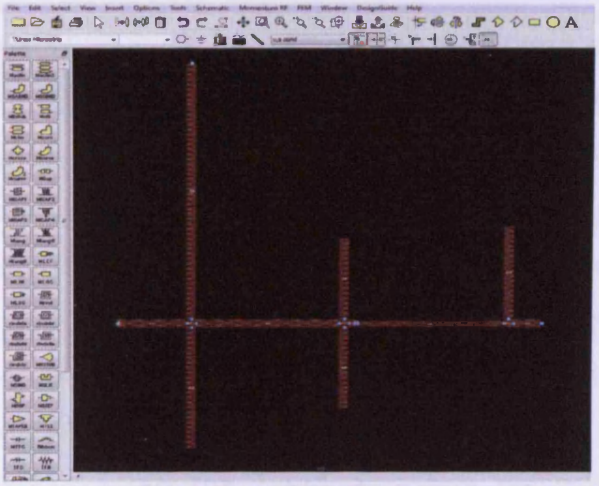

Fig. 4.11. Momentum simulation of the final output microstrip network.

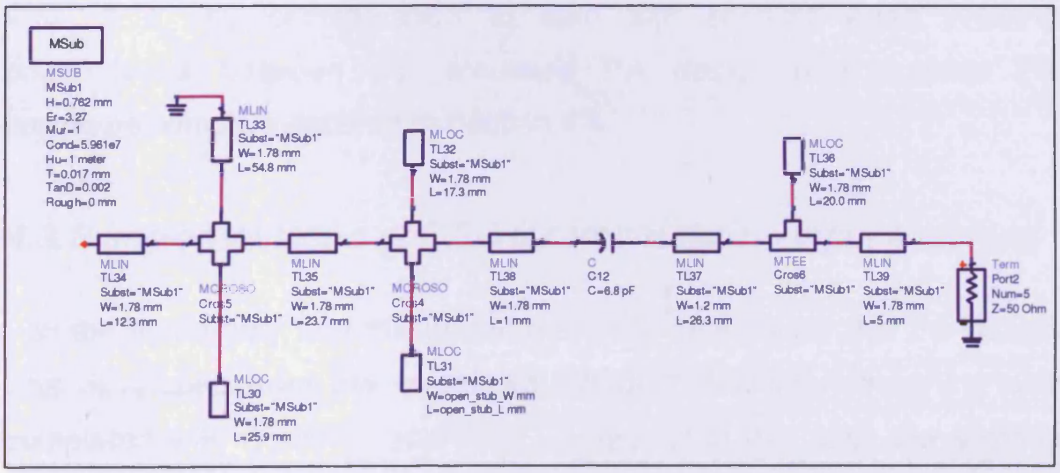

Fig. 4.12. Finalised output microstrip network design for 0.9GHz class-F^{-1} PA design (excluding biasing structure).

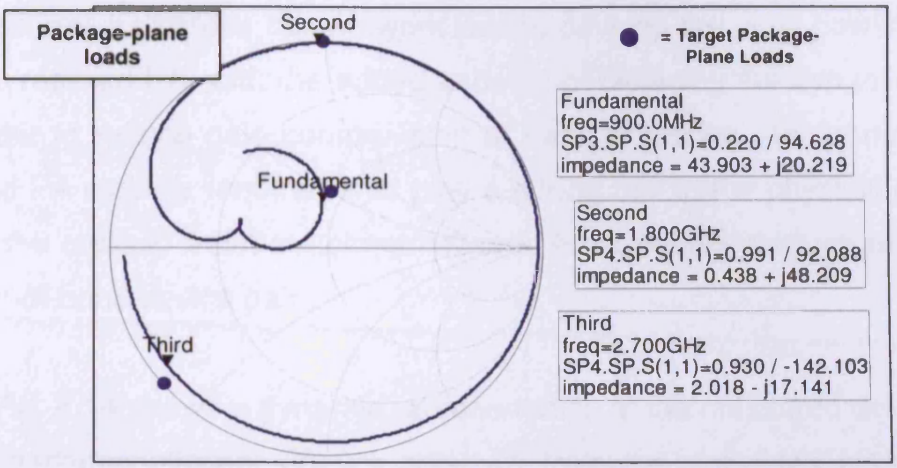

Fig. 4.13. S-parameter simulation results displaying the impedances presented by the output network to the device package-plane, as specified.

Figs. 4.11 and 4.12 show the final layout of the output network that was designed using a microstrip layout in TMM3® microwave laminate. The network S-parameters shown in Fig. 4.13 are those looking in towards the network from where the device output tab would be positioned. The result shows the network S-parameters very closely matching the target package-plane loads for optimum emulated device performance. However as a result of using a non-ideal, lossy substrate and conductor materials (although low-loss) there is now approximately a 0.5Ω and 2Ω real part to the second and third harmonic loads, respectively, which will inherently lead to degraded device performance within the realised PA. This is a key consideration to take into account when drawing comparisons between the emulated PA design and realised PA prototype, which is detailed in Section 4.4.

4.3.2 Implementation of CAD for Realisation – Input Matching

In the same way that the output matching network for this PA design was developed from the measured PA data, the input matching was completed with a similar approach. However in this case the specific requirements of the matching network were different, inasmuch as the

main requirement of this network was to develop the most power gain for the realised PA, with the added impetus of flattening the dynamic gain in order to reduce gain compression at peak efficiency. Inherently device and PA stability requirements play a strong role in the physical structure of the realised input matching network, most notably through minimising out-of-band device gain.

Fig. 4.14 shows a dynamic representation of the measured device input reflection coefficient ($Z_{in.opt}$) obtained from the optimised class-F^{-1} PA emulation at 0.9GHz. From this alone it is possible to observe the potential for designing an input match to suit an input reflection coefficient towards the top end of the power sweep, and thus counter as much as possible, the gain compression by intentionally providing a mismatched input reflection coefficient for lower drive levels.

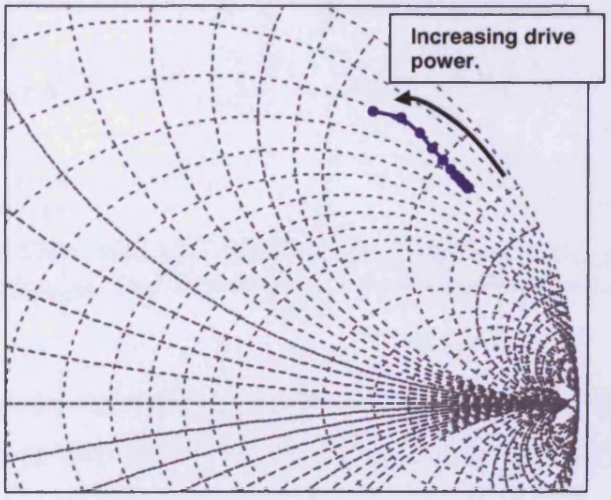

Fig. 4.14. Mapping device $Z_{in.opt}$ (package-plane) with drive for the class-F^{-1} PA emulation.

The measured DUT dynamic input reflection coefficient revealed a moderately fixed position at lower drive levels, but relatively more substantial variation as drive power increased towards compressed device operation (Fig. 4.14). Depending on the design value chosen for

the input reflection coefficient, a corresponding characteristic gain profile is produced; i.e. matching to the device input reflection coefficient at low drive power will result in optimum-high gain at low drive levels, but increased gain compression towards high drive. The highest efficiency condition occurs at higher drive and where the impedance mis-match contributes more to the level of gain compression observed. Matching to the device input reflection coefficient at highest drive power will result in a gain profile of lesser small signal gain but reduced gain compression (possibly even expansion) towards higher drive levels as the input match improved. The latter gain profile could be considered 'flatter' and, with respect to pre-distortion applications, a more desirable feature for linearising a PA [13]. Fig. 4.15 illustrates these two examples of gain profile.

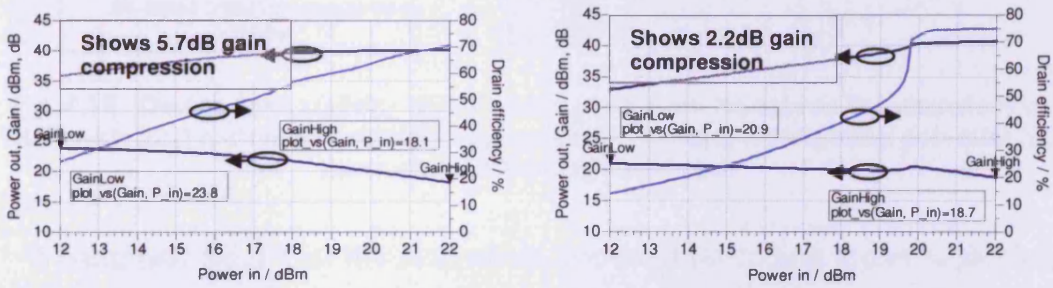

Fig. 4.15. (left) Simulated gain profile when matching to $Z_{in.opt}$ at low drive, compared with (right) gain profile observed when matching to $Z_{in.opt}$ at maximum drive.

Although Fig. 4.15 (left) shows improved efficiency across the dynamic range compared to that in Fig. 4.15 (right), it was decided that matching to the device $Z_{in.opt}$ measured at highest drive and efficiency would be most beneficial in this design case, thus obtaining maximum possible gain, and hence maximise PAE, of which this was a specific design goal. In doing this the process of PA linearisation may also be more easily applied as a result of the characteristic flatter dynamic gain profile [13]. This input match would be implemented via an open stub tuner, just as for matching the fundamental $Z_{out.opt}$.

With stabilisation also of key importance, simulating the proposed input and output networks with measured small-signal device S-parameters found that the device would be potentially unstable. This is indicated in Fig. 4.16 by the presence of regions of instability within the unity Smith chart in close proximity to the load matching network S-parameters.

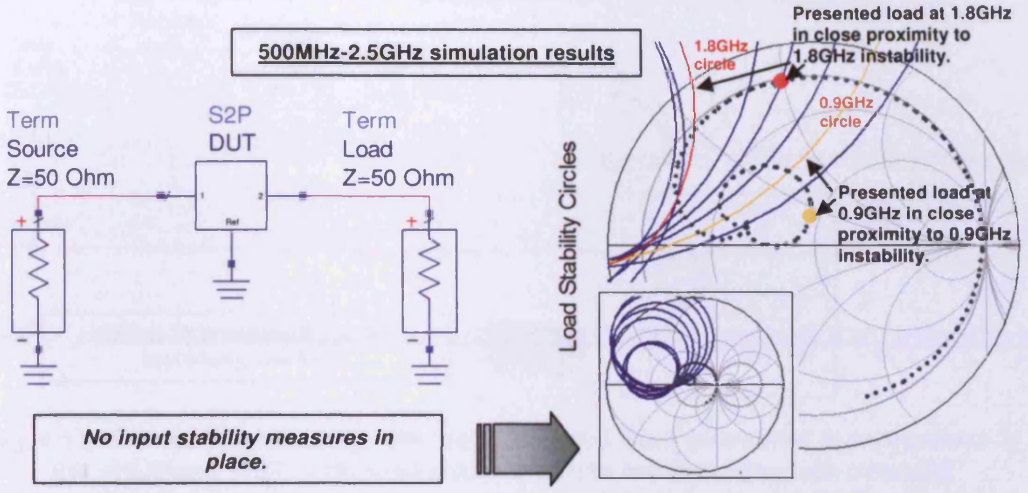

Fig. 4.16. Device load stability circles calculated from measured S-parameters of DUT, with load matching network S-parameters overlaid, highlighting potential for device instability and oscillation.

It becomes clear that the limitations imposed (including those regarding device stability) when realising the input and output networks meant that compromise in the small signal gain had to be made. Since the active load-pull measurement system provided an impedance environment of approximately 50Ohms at all frequencies with exception of those being load-pulled (i.e. 0.9, 1.8 and 2.7GHz), this design emulation could be completed without the need for prior device stabilisation. This is indicated in Fig. 4.16 where the optimum fundamental and second harmonic loads for this Class-F^{-1} design are located outside of the corresponding circles of instability. The same cannot be said however for several of the other impedances, at frequencies between the operating fundamental and second-harmonic, presented to the device by the

realised microstrip output network. For the prototype PA there is now the need for a series RF input resistance to move the load stability circles back outside of the Smith Chart in order to facilitate unconditional stability at all frequencies. This is demonstrated in Fig. 4.17.

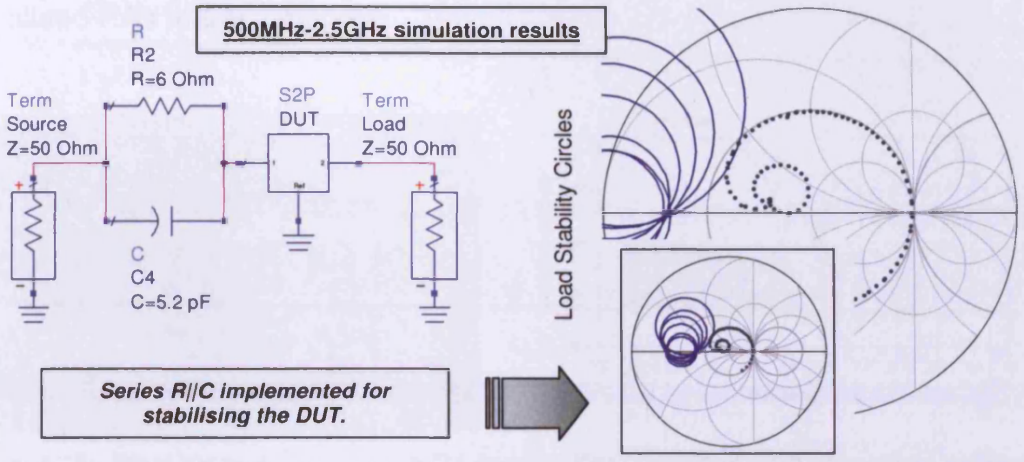

Fig. 4.17. Device load stability circles calculated from measured S-parameters of the stabilised DUT, with load matching network S-parameters overlaid, highlighting the removal of any potential for device instability.

The parallel combination of 6Ω resistance with 5.2pF capacitance was obtained through an optimiser S-parameter simulation of the network in Fig. 4.17, which gave the best compromise between low frequency stability whilst keeping the reduction in gain at the frequency of operation to a minimum. In fully stabilising the device this reduced slightly the maximum gain that could be achieved, however the process of intentionally mis-matching the device $Z_{in.opt}$ could still be applied.

The exact same matching network design method was repeated for the 2.1GHz class-F^{-1} PA design that had been load-pull emulated (**Chapter 3**). An input matching network for this second design example was also realised and designed once again for maximum device gain using the optimum input reflection coefficients obtained and measured at

the highest recorded drain-efficiency during the PA power sweep characterisation. Stability was ensured through simulation of previously measured bias-dependent device S-parameters. Both final realised PA prototypes are shown in Figs. 4.18 and 4.19 respectively. **Appendix A6** provides schematic details of the final circuit layouts for both of the realised PAs in this Chapter.

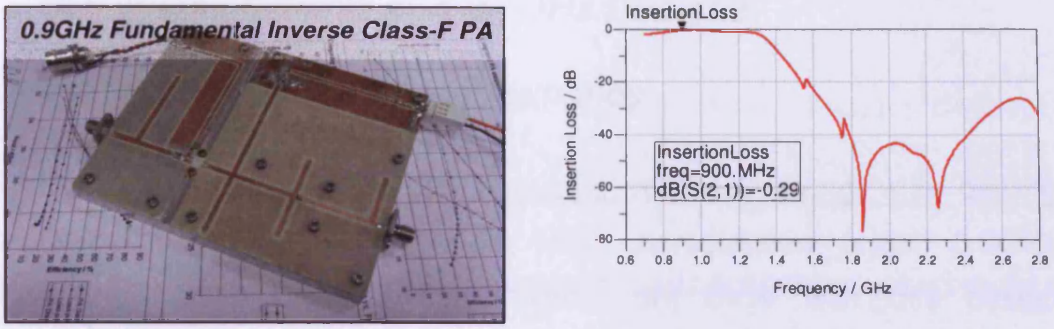

Fig. 4.18. Final class-F^{-1} prototype PA for 0.9GHz operation with measured output network insertion loss (right).

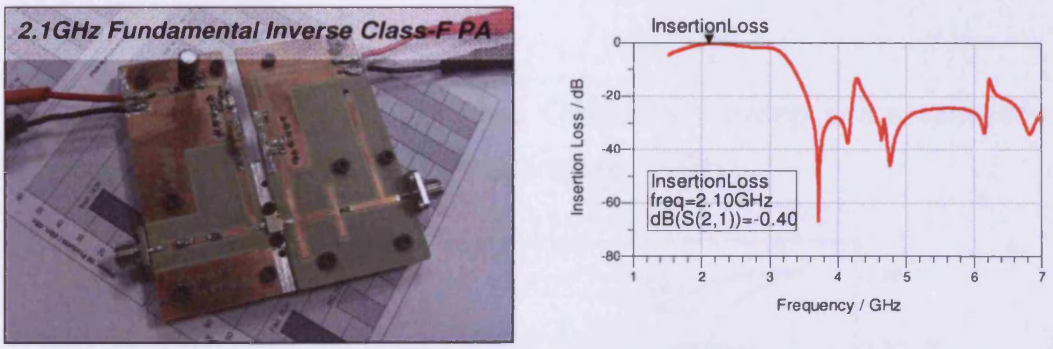

Fig. 4.19. Final high-efficiency prototype PA operating at 2.1GHz with measured output network insertion loss (right).

As a result of the higher frequency of operation, the 2.1GHz realised prototype PA (Fig. 4.19) provided a more challenging design consideration particularly in terms of the higher losses associated with the laminate compared to the 0.9GHz design. This would inherently lead to a reduction in the overall realisable efficiency of the PA as a whole. However for comparison purposes these losses could be taken into

account in both cases to directly compare with the initial PA load-pull emulations. It should also be noted that both of the 10W very high-efficiency power amplifiers realised here have been done so in relatively compact designs, giving rise to the added applicability in uses such as for unmanned aerial vehicles (UAVs).

4.4 Prototype PA Performance Characterisation and Analysis - 0.9GHz and 2.1GHz Designs

4.4.1 Initial results of PA performance

With the input and output networks realised, along with biasing networks, the PA performance was characterised under 0.9GHz frequency CW stimulus. In coming full circle with this design methodology, comparisons are made in section 4.4.2 between these results and the initial waveform-engineered measurements from which the PA was realised from.

Fig. 4.20 shows results from the CW power sweep characterisation, conducted at the fundamental frequency of 0.9GHz.

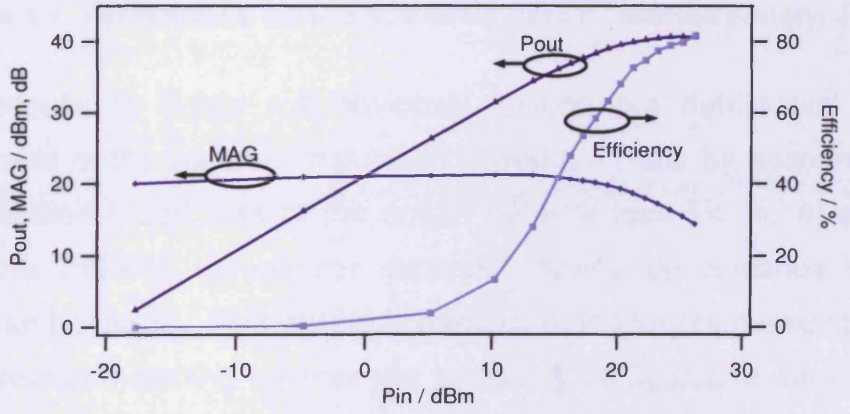

Fig. 4.20. Power sweep characterisation of realised 0.9GHz class-F^{-1} PA indicating Pout, gain and drain efficiency vs. Pin.

Fig. 4.20 demonstrates the very high peak drain efficiency achieved in

the realised 0.9GHz PA prototype, measured at 81.8%. This is obtained with the PA in a high state of compression, as it was during the design emulation. However the intended gain expansion at lower drive levels, although only in the region of 1.5dB, is present in the results of Fig. 4.20 showing a degree of success in the input match design objective of flattening the gain profile, as described in section 4.3.2.

4.4.2 Comparison between emulated design and realised PA

The peak performance figures obtained from the realised PA (summarised in **Table 4.4**) correspond very closely to those measured during the initial waveform-engineered PA emulation, detailed previously in **Table 4.2**.

Optimised Inverse Class-F Performance – Waveform Measurements	
Frequency:	***0.9GHz*** *fundamental frequency with second and third harmonic matching.*
Drain Voltage:	***28V*** *DC rail voltage (consistent for all drive conditions).*
Gate Voltage:	*Gate bias set to approx.* ***-1.8V*** *ensuring* I_{dsq} *(quiescent drain current) of* ***420mA*** *(mid A/B bias point).*
Power:	*Device* ***P3dB*** *output power of approximately* ***11.2W****.*
Gain:	*Maximum matched PA gain of* ***21.2dB****.*
Efficiency:	*Maximum drain efficiency of* ***81.8%*** *measured at* ***11.5W*** *output power.*

Table 4.4. Performance summary; 0.9GHz class-F^{-1} realised prototype PA.

The results in Table 4.4 obviously include the detrimental effects (i.e. losses) of the passive matching networks. Thus, by accounting for the measured 0.3dB loss of the output network (see Fig. 4.18) a closer and more realistic comparison between device performance in both cases can be made. Following this removal of the losses associated with the microstrip matching network the performance figures of the PA were adjusted, revealing further close agreement in device operation. This is summarised in Table 4.5, all of which giving further indication that the mode of operation emulated initially has now been replicated within this realised PA prototype.

One further comparative measure is shown in Fig. 4.21 in the form of a dynamic power sweep of the load-pull emulation and realised PA, minus output matching losses. Here, a much closer replication of the dynamic performance is obtained by the PA in relation to the comparison made between the NL device model PA simulation and the emulated results (Fig. 4.4), particularly in terms of the dynamic efficiency. This all provides strong evidence that the class-F^{-1} mode developed through the load-pull emulation procedure detailed in **Chapter 3** has been accurately and precisely replicated in this prototype PA at 0.9GHz.

Performance Measures	*Device Measurements (0.9GHz Fundamental)*	*Realised PA (0.9GHz Fundamental)*
P1dB Output Power	*38.6 dBm*	*38.1 dBm (38.4dBm at the dev.)*
P3dB Output Power	*40.6 dBm*	*40.4 dBm (40.7dBm at the dev.)*
Max. Avail. Gain at P1dB	*25.6 dB*	*24.2 dB (24.5dB at the dev.)*
Drain Efficiency at P3dB	*79.8 %*	*76.7 % (82.2% at the dev.)*

Table 4.5. Comparison between emulated class-F^{-1} and realised PA (0.9GHz).

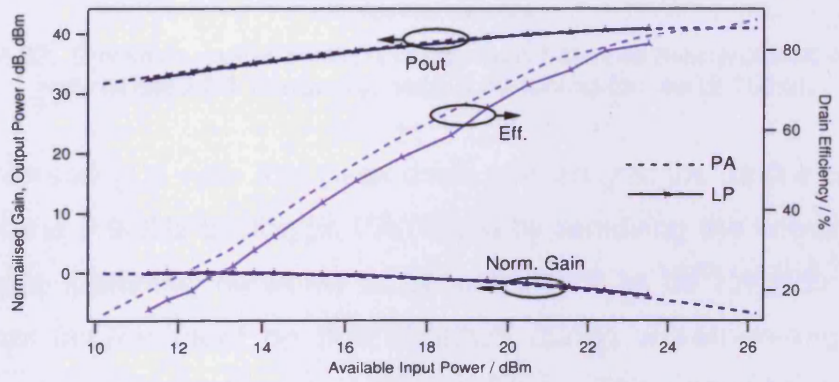

Fig. 4.21. Dynamic power sweep comparison between the emulated class-F^{-1} and realised PA minus the output matching losses (0.9GHz).

Similarly the 2.1GHz PA realisation yielded closely agreeing performance figures to those recorded during the design emulation stage. Table 4.6 and the dynamic power sweep comparison in Fig. 4.22 present

these results, which also includes performance that exists at the device package - found as a result of removing the 0.4dB loss associated with the output matching in this case (see Fig. 4.19).

Performance Measures	*Device Measurements (2.1GHz Fundamental)*	*Realised PA (2.1GHz Fundamental)*
P3dB Output Power	*40.0 dBm*	*39.4 dBm (39.8dBm at the dev.)*
Max. Avail. Gain at P1dB	*16.9 dB*	*15.7 dB (16.1dB at the dev.)*
Drain Efficiency at P3dB	*73.0 %*	*71.0 % (77.8% at the dev.)*

Table 4.6. Comparison between emulated class-F^{-1} and realised PA (2.1GHz).

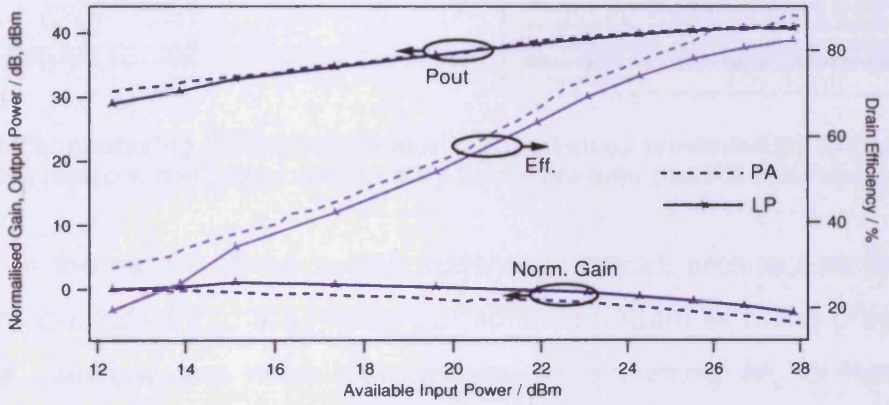

Fig. 4.22. Dynamic power sweep comparison between the emulated class-F^{-1} and realised PA minus the output matching losses (2.1GHz).

It is interesting to note that peak drain efficiency at the device package-plane of the 0.9GHz prototype PA (found by removing the known loss of the output matching network) is be calculated to be towards 87%, a significant improvement on that obtained during waveform-engineering the second and third harmonic terminations. This observation can be explained in Fig. 4.23, which shows, once again, the final optimised output matching network implemented for the 0.9GHz class-F^{-1} PA prototype. This time however, analysing it at higher frequencies than those considered during the design stage (i.e. beyond the 3rd harmonic

term), reveals - and also confirms - the advantage in this matching architecture for narrowband, high-efficiency PA designs.

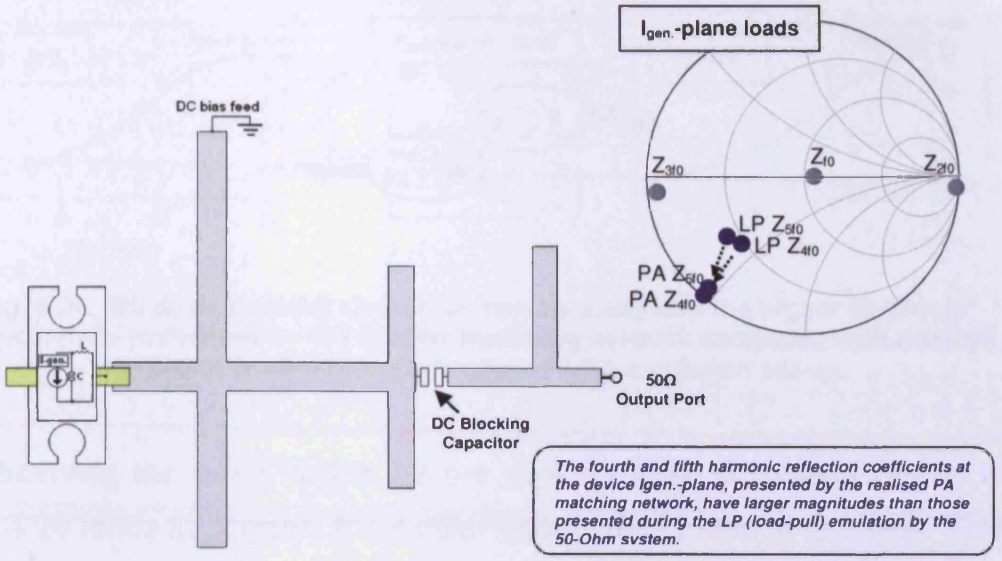

Fig. 4.23. Analysing the higher harmonic impedances presented by the 0.9GHz matching network compared with that by the active load-pull PA emulation set-up.

Due to the nature of the output matching network architecture [5, 9], it can be concluded that the higher harmonic impedances being presented by the network are more favourable for achieving higher-harmonic approximations of class-F^{-1} operation. This is in comparison to that obtained during the load-pull emulation, where the uncontrolled package-plane fourth and fifth harmonic impedances are 50Ω, by definition of the measurement system architecture [14]. Without load-pull acting at these higher harmonic terms during the design emulation, it is thus impossible to obtain the perfect Class-F^{-1} target waveforms and so a detriment in peak achievable device efficiency is observed when compared to the prototyped PA.

This observation is backed up by the device NL model simulation which up until now, in this design case, has already shown comparable trends with those seen from the device measurements themselves. Thus, it has

been used here to reinforce this observation seen in practice, with results of the simulation shown in Fig. 4.24.

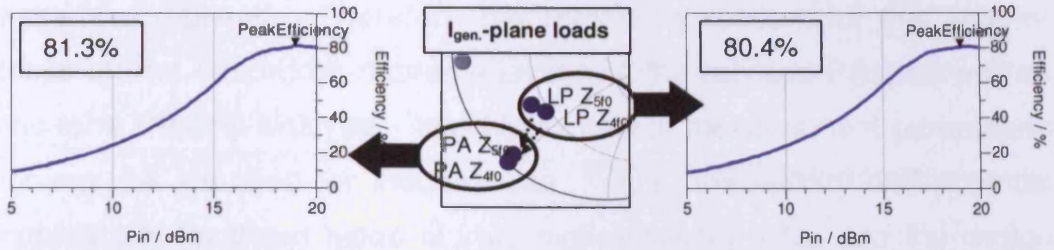

Fig. 4.24. NL device model simulation results analysing the higher harmonic impedances presented by the 0.9GHz matching network compared with that by the active load-pull 0.9GHz class-F^{-1} PA emulation set-up.

Observing the trend shown by the device model simulation results in Fig. 4.24 tends to suggest the similar observation found in practice. This backs up the claim that the higher harmonic impedances are more favourably terminated and hence leading to the observed increase in package-plane device efficiency within the realised PA.

4.4.3 Initial realisation conclusions

It has been seen already that successful replication of the class-F^{-1} mode PAs emulated and described in **Chapter 3** have been achieved through the realisation of two stand-alone PA prototypes at two independent operating frequencies. This direct implementation of the captured waveform measurement data for PA matching network design and realisation has been followed through and verified for the first time for a high-efficiency, multi-harmonic PA load-pull emulation. Strong potential has been shown from this direct fabrication, waveform-engineered design approach as an accurate and reliable PA design methodology.

It is recognised, however, that for implementation within a real-world

communications system, the high-efficiency-mode PAs designed and realised using the methodologies described in this chapter and in **Chapter 3**, require further analysis and characterisation outside of that already completed. Therefore the remaining sections of this chapter focus on the bandwidth characterisation of the realised PAs, as well as two-tone linearity analysis - two highly critical measurement parameters for any PA intended for industry use. Thus, the validity and potential applicability for these types of very high-efficiency PAs, and the design methodologies behind their fabrication, will be discussed further.

4.4.4 Efficiency-bandwidth of PA performance

Although commonly regarded (and for good reason [10, 15]) as an inherently 'narrowband' architecture, the class-F^{-1} PAs realised in this study have been characterised beyond their respective intended and designed-for centre-frequencies (CF). This analysis enabled a measure of 'efficiency-bandwidth[6]' for each of the designs. Figs. 4.25 and 4.26 show this performance characterisation result for the 0.9GHz and 2.1GHz realised PAs respectively, both set and fixed at the same bias conditions as for the intended CF of operation. Peak drain efficiency has been recorded in each measurement case.

The efficiency-bandwidth appears to become bandwidth-limited by the resulting frequency-dependent phase-rotation of the S-parameters presented by the output (and also input) matching network, compared with the phase rotation of the required harmonic impedances for class-F^{-1} at the device package-plane. Fig. 4.27 shows the extent to which the harmonic impedances presented by the output matching network shift with frequency, in comparison with the variation of the device package-plane impedances required for class-F^{-1}.

[6] '*Efficiency-bandwidth*' is used in the context here as a combined description of the level of efficiency that the PA operates, and how the efficiency level is maintained across a given frequency bandwidth.

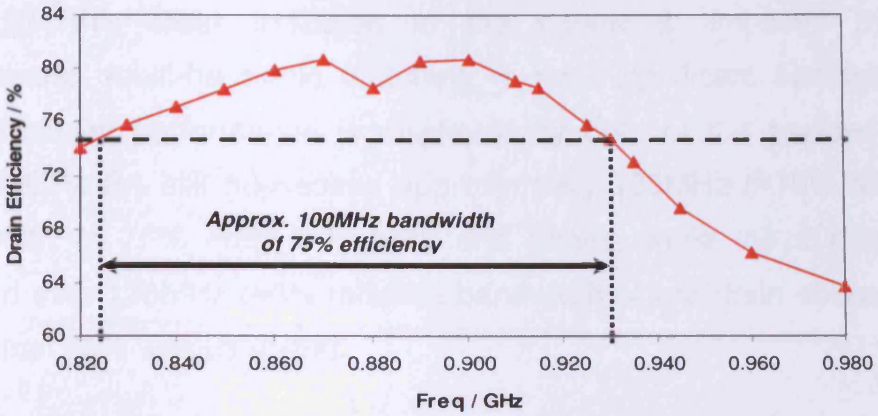

Fig. 4.25. Efficiency-bandwidth performance of 0.9GHz PA prototype.

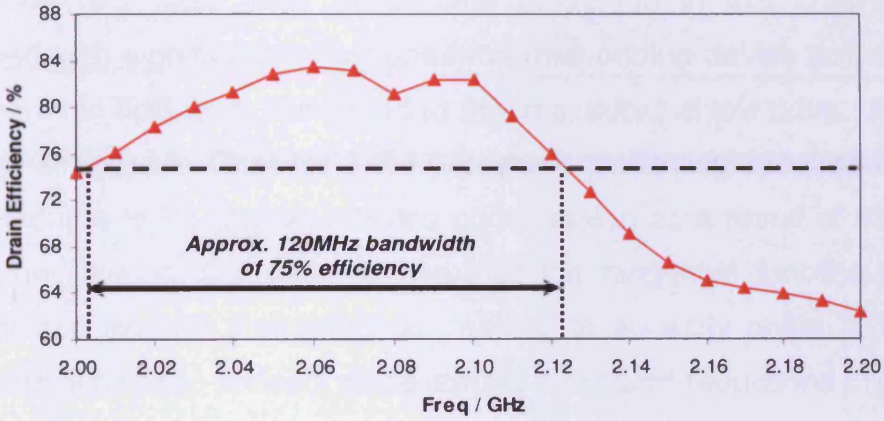

Fig. 4.26. Efficiency-bandwidth performance of 2.1GHz PA prototype.

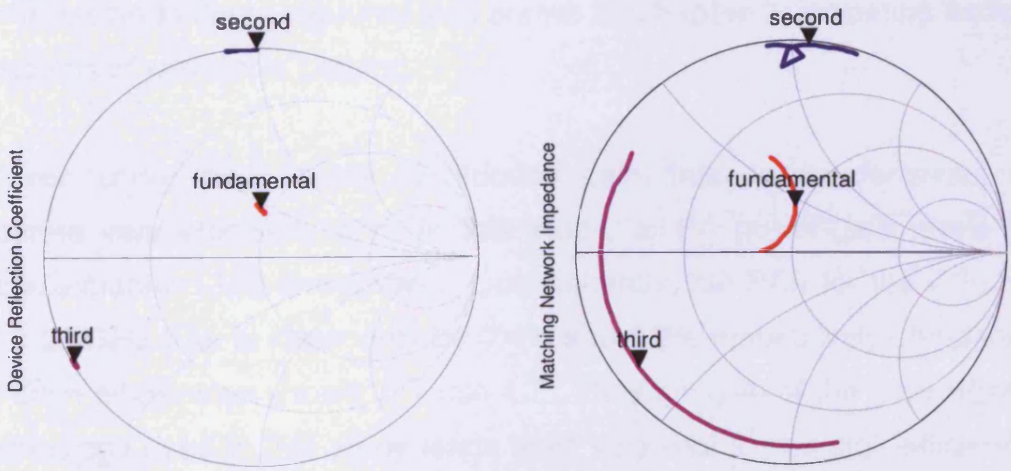

Fig. 4.27. Impedance traces for required class-F^{-1} at device package-plane (left) compared to those calculated from the output matching network S-parameters (right) with frequency.

Despite this clear limitation in the bandwidth imposed by the narrowband, multi-harmonic matching, a not-insignificant bandwidth of high-efficiency performance is displayed by both of the realised PAs. The 0.9GHz PA still possesses approximately 100MHz (≈10% relative) bandwidth of 75% drain efficiency and above, while the 2.1GHz PA showed over 120MHz (≈6% relative) bandwidth where drain efficiency of more than 75% was exhibited.

As in the design emulation from **Chapter 3**, it is important to note that all of the very high peak efficiencies presented in this chapter are observed with significant reductions in corresponding device power gain (between 4 to 5dB less) compared to that measured at low drive. As was similarly stressed in **Chapter 3** the processes facilitating this drop in gain is not thought to be physical device compression as a result of extreme waveform clipping, but partly a result of the tangential function of the 'real' device transfer characteristic, leading to an early onset of output waveform distortion. Indeed, since similar measured reductions in device gain have been observed in the prototype PAs dynamic characteristics as in the PA load-pull emulation, the output waveforms can be assumed comparable to those captured and shown in **Chapter 3**; indicating limited amounts of waveform clipping.

Even under such levels of reduced gain, this device continues to operate very efficiently and, in this study, at PA power-gain levels of approximately 13dB and above. Consequently, the PAE for the 0.9GHz and 2.1GHz PAs is lower only by 0.4% and 4.2% respectively compared to drain efficiencies shown in Table 4.7. The high gain of the GaN HEMT technology used in this study lends itself very well to this high-efficiency PA application.

Performance Measures	***Realised PA*** *(0.9GHz Fundamental)*	***Realised PA*** *(2.1GHz Fundamental)*
Peak PA Drain Eff.	*81.8 %*	*82.3%*
Power-gain at peak drain eff.	*23.0dB*	*12.9 dB*
Peak achievable PAE	*81.4%*	*77.6 %*

Table 4.7. $PAE_{max.}$ of realised input-matched PAs compared with drain efficiencies.

However it is important also to note that, in terms of linearity, this high level of device output distortion will be detrimental. Thus characterisation of this PA performance parameter was necessary in making a full judgement of this design methodology. This analysis follows in section 4.5.

4.5 Linearity characterisation and applicability to wireless communications systems

4.5.1 Two-tone linearity performance of realised very high-efficiency inverse class-F PA

Output frequency spectra are displayed in the following plots for the 0.9GHz amplifier under excitation by two frequency tones (900MHz and 910MHz) of the same power. The input stimulus was varied such that the amplifier was in P1dB state, P3dB state and its maximum efficiency state respectively. The spectra plots in Figs. 4.28 to 4.30 show the fundamental power out at one of the stimuli frequencies, as well as indicating dBc (power, with respect to the carrier power) levels of the measured worst-case IM (inter-modulation) products that were generated by the PA.

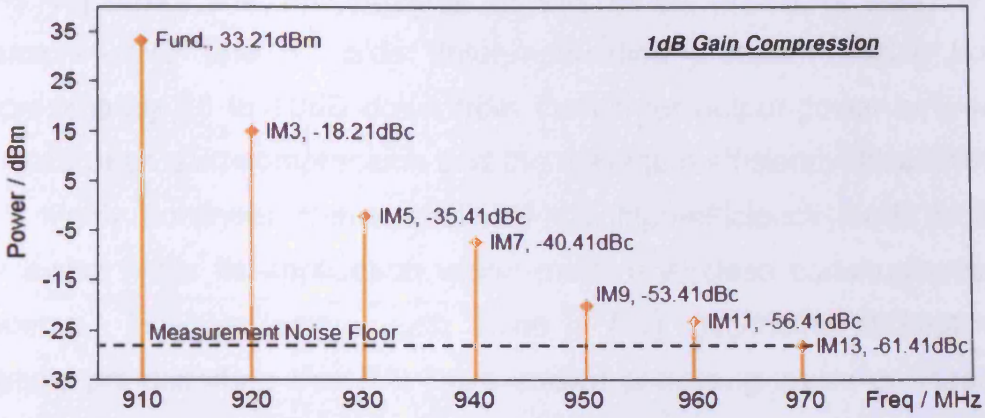

Fig. 4.28. IM products measured at PA output whilst under two-tone stimulus developing P1dB gain compression.

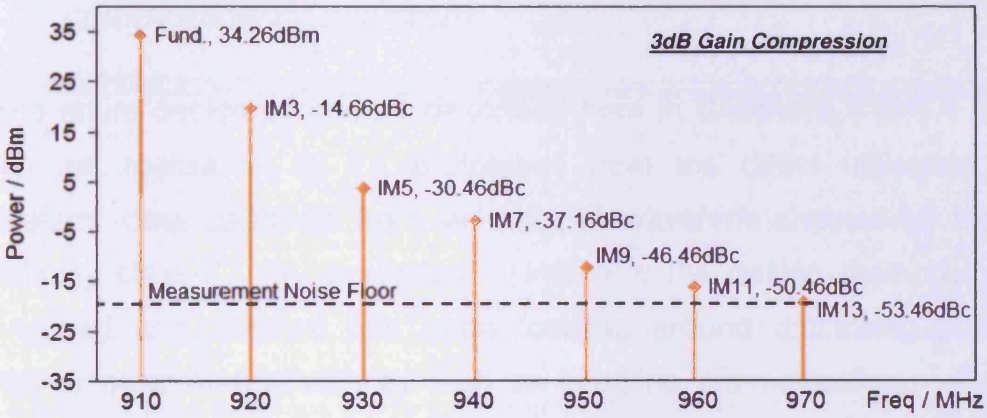

Fig. 4.29. IM products measured at PA output whilst under two-tone stimulus developing P3dB gain compression.

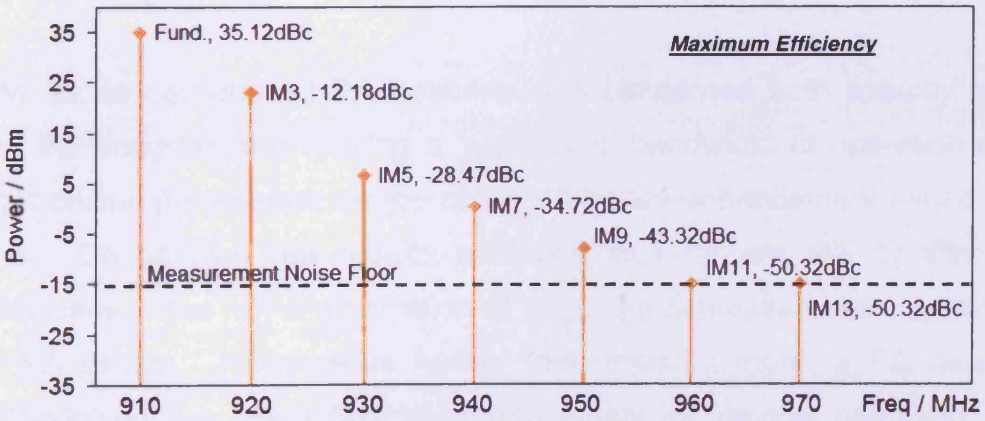

Fig. 4.30. IM products measured at PA output whilst under two-tone stimulus developing maximum efficiency (approx. 4.5dB gain compression).

As expected, the raw linearity of this mode of PA is poor, with measured IM3 (the 3rd order inter-modulation product) ranging from approximately 20 to 10dB down from the carrier output power between the 1dB peak gain compression and the maximum efficiency drive levels. This highly nonlinear characteristic of this high-efficiency mode of PA somewhat limits its application within modern wireless communications systems. However works such those in [16], describing attempts at digitally pre-distorting this PA, have shown promising levels of linearity enhancement.

4.5.2 Usefulness of design in a modern wireless communications system

The entire design procedure described here in **Chapters 3** and **4** has seen the realisation of PA prototypes from the direct utilisation of waveform data captured from an original waveform-engineered high-efficiency class-F^{-1} PA emulation. Until now the design methodology developed and detailed has been focused around optimising power amplifier performance with as high as possible drain-efficiency. As a result this prototype PAs realised are restricted in their usefulness within a real-world wireless communication system, namely in terms of linearity as demonstrated in section 4.5.1.

As far as commercial PA usefulness is concerned both linearity and also the importance of having a 'significant' bandwidth of operation are other crucial parameters on top of the efficiency-enhancement aimed-for here. On its own the results achieved thus far are still significant, particularly in the novel application of large-signal measurement systems for PA design. However to further this research more, a PA design methodology for the efficiency-enhancement of device operation, in combination with extending working operation of the PA across a broader

bandwidth and also whilst keeping linearity levels within 'reasonable' bounds, is to be investigated, with the aim of developing an optimised trade-off between each of the parameters described. Thus in **Chapter 5** a more greatly applicable PA for the modern wireless communication system aims to be designed and prototyped through waveform measurements and engineering alone, using techniques such as those having been demonstrated in the previous two chapters.

4.6 Chapter Summary

The first attempts at realising very high-efficiency, high-power amplifier designs directly from load-pull waveform emulation data have been demonstrated in this chapter. The very high-efficiency PA designs, developed from a novel design methodology described in **Chapter 3**, using a 10W GaN HEMT, have been prototyped following the direct translation of waveform measurement data carried out at 0.9GHz, and also 2.1GHz. The device performance, verified through the combination of high-power waveform measurements [14] and device package de-embedding [12], has been replicated after realisation of PA prototypes based around the commercially available 10W GaN HEMT with the use of a CAD environment and the direct import and utilisation of waveform measurement data, without the use of a NL device model, besides comparison. A microstrip output network, replicating (as closely as possible) the optimum three-harmonic package-plane impedances, has been realised along with a specifically designed input matching structure to engineer the shape of the final PA gain profile. Performance characterisation of the final class-F^{-1} prototype PAs has indicated strong replication of that obtained from the respective original PA load-pull emulation, suggesting that measurement data from a waveform-engineering-based design process can be implemented successfully for the prototyping of high-efficiency power amplifiers.

Two emulated high-efficiency amplifier designs have been realised as high-efficiency prototypes through direct utilisation of the measurement data captured using a high-power waveform measurement and characterisation system. Performance comparisons have been made at the two frequencies of operation investigated in this study (0.9GHz and 2.1GHz) and characterisation including PA efficiency across bandwidth has shown up to 10% relative bandwidth of very high-efficiency (75%+) operation.

4.7 References

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Chapter 5. Extending High-Efficiency, Waveform-Engineered PA Design Towards Broadband Applications

5.1 Introduction

PA design for wireless communication has, until recently, been focused on specified RF bandwidths of 5% or lower, due mainly to the very tight spectrum allocations. Future systems, including WiMax, 4G and beyond, will likely require larger bandwidths, not just due to wider spectral allocations, but the base bandwidth of the signals themselves which may well extend up to, and ultimately exceed, 100MHz. To date, other RFPA applications, such as radar and ECM (electronic counter measures) have not profited from advances in power and efficiency due to their much wider RF bandwidth requirements. Reported results on very high-efficiency PAs, typically operating above 75% efficiency, tend to rely heavily upon precise multi-harmonic impedance terminations at the DUT as well as very high levels of device gain-compression. Both of these factors lead to narrowband frequency performance limitations (less than 10%) and non-linear operation respectively. A newly presented, and much discussed, mode of operation - class-J [1] - has shown the theoretical potential of obtaining linear RFPAs that have the same efficiency and linearity as conventional Class-AB designs but do not require a band-limiting transmission-line harmonic short.

The class-J mode uses second harmonic voltage enhancement, as described by previous workers [1-5]. This technique poses an immediate problem inasmuch as the device absorbs, rather than generates, second harmonic power. Techniques such as current waveform clipping [2], or wave-shaping the input signal [3] have been proposed in an attempt to null the second harmonic component. The class-J approach utilises a phase shift between the output current and voltage waveforms to render the second harmonic termination into the purely reactive regime. This enables significant possibilities into the realisable bandwidth-efficiency performance of the class-J mode of PA using GaN HEMT power transistors.

This chapter describes the design and realisation of PA matching networks yielding a broadband amplifier operating at high-efficiency, implementing many of the waveform-engineering design techniques investigated and employed in **Chapters 3** and **4**, but now with the objective of designing and fabricating an optimised broadband class-J-mode PA. In addition, application of a new theory [5], from which a furthering of the novel broadband class-J design methodology has been made, is investigated and PA designs realised with high relative bandwidth-efficiency. This novel design methodology makes comprehensive use of active load-pull, or waveform-engineering techniques, and uses a novel design methodology to achieve predistortable linearity [6-7]. To knowledge, such a design has not before been attempted on an *a priori* basis.

The high power measurement and characterisation capability in [8] has been utilised in the development of this broadband PA design methodology, demonstrating a new practical approach to handling the second harmonic loading problem in broadband PA designs. Work such as in [9], which addresses multi-octave high-efficiency PA designs, use

resistive second harmonic loading within a portion of the specified bandwidth. Hence (and appropriately), only fundamental load optimisation is considered viable in such cases. This chapter of work presents a design methodology enabling a good compromise in efficiency across bandwidths below one octave.

Waveform and systematic load-pull measurement data has been used in the development stage of the design procedure, whilst also being used to analyse the extent to which optimum broadband high-efficiency operation has been achieved in this mode. Measurements have been focused around a target sub-octave bandwidth of 1.5-2.5GHz.

Device output parasitic de-embedding has been applied to the waveforms captured at the calibrated measurement plane of the device package in confirming class-J behaviour from the output voltage and current waveforms at the device plane [10].

5.2 Broadband High-Efficiency With Class-J Mode of PA

5.2.1 Class-J Harmonic Load Terminations

Cripps [1] (who acknowledges some earlier work by Raab [11]) has described class-J, defined as a mode in which the voltage has harmonic components which make it tend asymptotically towards a half-wave rectified sine-wave. This in practice can be usefully approximated by a suitably phased second harmonic component. The key difference between class-J and more familiar class-A, AB and F modes, is the requirement for a reactive component at the fundamental load. The differentiation between class-J and class-E has been explained in detail in [1] and cited elsewhere in [12], and can be considered the starting condition in each case. The starting point in class-J design methodology is the linear class-B (or 'deep' class-AB) mode, where the output current

waveform is a classical reduced conduction angle sinusoid. As such, the class-J amplifier can be expected to have the same linear performance as a class-AB amplifier operating at the same conduction angle. The starting point for a class-E mode (i.e. [13]), however, is to assume that the active device behaves as an ideal switch. Thus any practical implementation of a class-E design requires that the active device be 'forced' into behaving like a switch, and this usually involves the device being forced to clip on the supply rails for a part of the RF cycle. This leads to strongly nonlinear performance, albeit often with very high-efficiency.

The class-J voltage waveform is engineered by using appropriate passive fundamental and second harmonic terminations. In this way, a higher fundamental component can significantly outweigh the loss in power implied by the reactive load, a counter-intuitive result that has been discussed in detail elsewhere [1]. A class-J design thus displays approximate half-wave rectified sinusoidal output current and voltage waveforms, with a phase overlap between the two (Fig. 5.1). This mode of operation lends itself very well to the process of waveform-engineering, as described previously in [8, 14]. Independent bias and drive control, and active multi-harmonic load-pull are used to engineer the shape of the current and voltage waveforms respectively.

The class-J output voltage waveform - assuming two-harmonics - is specified in Table 5.1 [1]. From this the fundamental and second-harmonic impedances, as defined in equations (5.1) and (5.2), can be found, thus defining the matching criteria. In order to optimise efficiency, the GaN device requires some compromises in setting the design values for the fundamental ('load-line') resistance, due to the effect of the DC 'knee'-voltage offset [15].

Harmonic	Normalised voltage component
1	$1.41 \angle 45°$
2	$0.50 \angle -90°$

Table 5.1. Ideal class-J voltage waveform, assuming two harmonics.

$$Z_{f_0} = R_L + j \cdot R_L \tag{5.1}$$

$$Z_{2f_0} = 0 - j \cdot \frac{3\pi}{8} \cdot R_L \tag{5.2}$$

Ideal class-J theory assumes that there is no third-harmonic component present in the voltage waveform, and hence Z_{3f0} is assumed short. This required loading can usually be readily approximated through the effect of the device output capacitance within a PA matching network design, which thus has the tendency to provide a short to all of the higher harmonics. Fig. 5.1 illustrates measured waveforms with these harmonic terminations, however in this measurement the third harmonic load was allowed to be adjusted slightly in order to demonstrate optimum class-J waveforms and hence, high power and efficiency (as specified in Table 5.2). The bias point implemented here was deep class-AB (I_{dq}≈5% of I_{dss}).

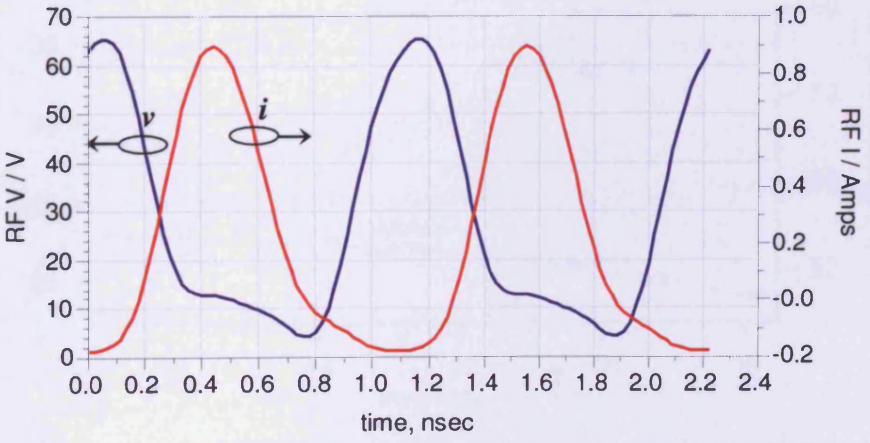

Fig. 5.1. Measured typical class-J waveforms on a 10W GaN HEMT.

Frequency	$I_{gen.}$-Plane Load Impedance
f_0	43.8 + j45.2 Ω
$2f_0$	1.6 – j52.0 Ω
$3f_0$	2.4 – j49.7 Ω

Table 5.2. Class-J $I_{gen.}$-plane load terminations.

5.2.2 Waveform-Engineering Very High-Efficiency Class-J Operation in a GaN HEMT

By applying the prescribed class-J impedance components up to $3f_0$, through active load-pull, very high-efficiency device operation has been measured at a fundamental frequency of 1.8GHz. The power sweep for this optimum emulated case is shown in Fig. 5.2. This shows the output performance of the DUT in a class-J loading configuration, operating with a bias point in class-C.

In this separate attempt to demonstrate the very high-efficiency potential of class-J, this condition saw the conduction angle reduced beyond the class-B starting point, to the detriment of the device output power.

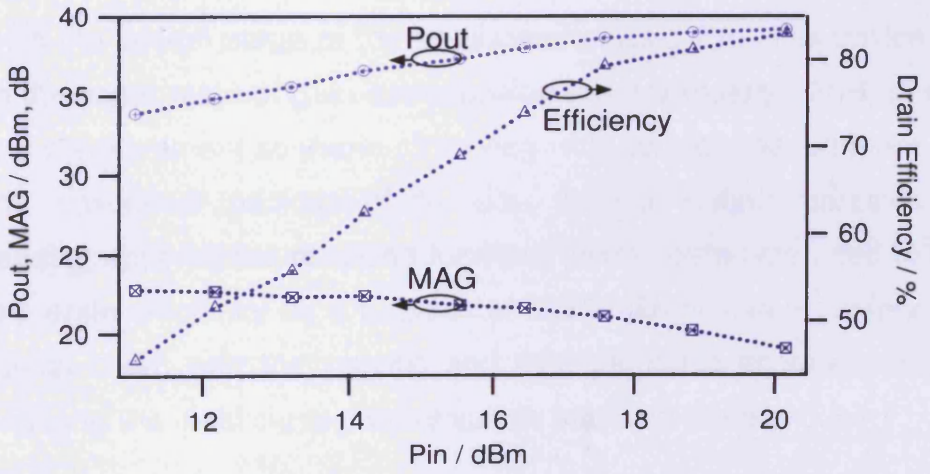

Fig. 5.2. Power sweep showing very high-efficiency class-J operation at 1.8GHz (input unmatched, maximum available gain (MAG) shown).

A peak drain efficiency of 83% has been measured in this state with just below 10W device output power and approximately 3.5dB of gain compression. Note that even at the 6dB power back-off point, the measured drain efficiency is still above 60%. Device output power is however slightly less than was observed for the same device type in an optimised class-F/class-F^{-1} PA mode, within the same boundary conditions [14].

Following this initial performance characterisation of the class-J mode, a linear 10W broadband PA design was initiated, with a goal of above 60% efficiency over the 50% bandwidth of 1.5-2.5GHz.

5.3 Broadband, Linear Class-J PA Design Using Waveform Measurements and Multi-Harmonic Active Load-Pull

5.3.1 Broadband Measurements and PA Realisation

Active harmonic load-pull was initiated on the GaN transistor to be used in the design, using the three-harmonic active load-pull set-up [8]. This was carried out at several frequencies between 1.5 and 2.3GHz in order to begin the design stage of the broadband class-J PA. The device was set in the same state of gain compression (approximately P2dB) in each class-J measurement scenario. Working with device measurement data at the calibrated package-plane (i.e. without output parasitic de-embedding applied) the resulting load-pull sweep data was used to map out the drain efficiency as a function of fundamental load impedance on the Smith chart, with the second and third harmonic impedances fixed according to the ideal class-J terminations stated in Section 5.2.1.

Fig. 5.3 shows the 70% drain efficiency contour obtained from each fundamental load sweep, indicating the movement of the optimum

fundamental load for efficiency at the device package-plane as a function of frequency. A corresponding output power contour plot was extracted following the load-pull sweep which provided a 'target region' of load impedances for which to aim a matching circuit design to provide a compromised class-J PA output power and drain efficiency.

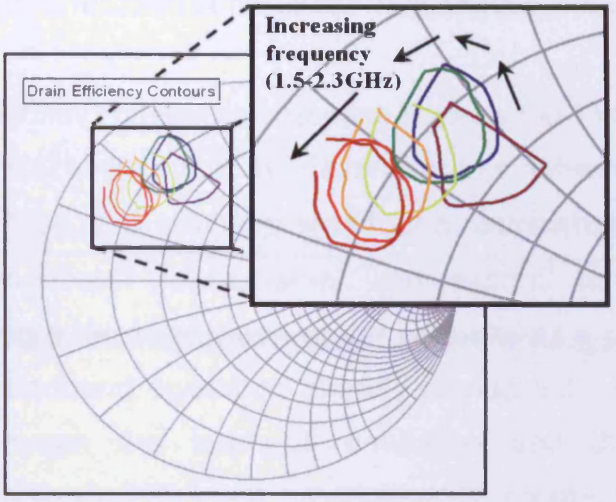

Fig. 5.3. Measured load-pull data for GaN HEMT indicating load impedance contour for 70% P2dB drain efficiency between 1.5-2.3GHz.

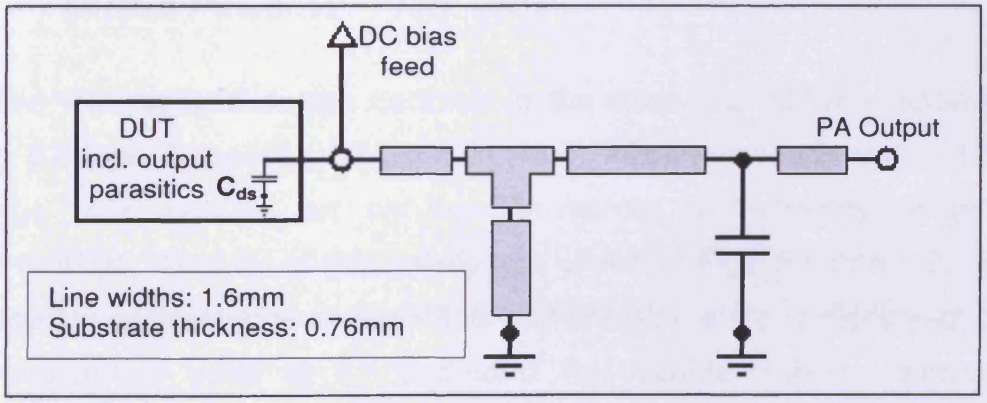

Fig. 5.4. Realised load matching network schematic [1].

The original target frequency band was 1.5-2.5GHz and in designing a suitable matching network over this extended bandwidth, some compromises have to be made. The initial strategy on the first design iteration (presented in this section) was to give higher priority to the

fundamental impedance and allow the second harmonic more latitude. This particular device has a low output capacitance (approximately 1.5pF) which at 2GHz is itself quite close to the optimum reactive termination at the second harmonic. Thus the network itself mainly synthesises the required fundamental load over the extended bandwidth, but through a shunt inductive stub increases the effective second harmonic capacitive reactance for lower frequencies.

The output matching network schematic is shown in Fig. 5.4. Although not a novel architecture in itself (variations of this network are analysed, for example, in [16]), this structure was found, somewhat empiracally, to provide the broadband fundamental and second harmonic loading required, enabling a demonstration of the potential as a prototype PA for the emulated broadband operation already carried out. For purposes of comparison between the load-pull emulation and the realised PA performance, the same 50Ω input impedance environment was used.

5.3.2 Realised Class-J Performance Results - Efficiency and Output Power vs. Frequency

The first realised design iteration of the class-J amplifier is shown in Fig. 5.5 (see **Appendix A7** for full circuit). Power sweeps over a 12dB range were carried out on the PA across a frequency range of 1.2-2.5GHz. Results of this sweep are shown in Figs. 5.6 and 5.7. The efficiency performance at the P2dB compression state is displayed; this is customarily used as an 'end-point' for useable high-end efficiency performance in high PAR (peak-to-average ratio) linear signal applications.

As seen in Fig. 5.6, the measured P2dB drain efficiency for the realised class-J amplifier is at a level of 60-70% between 1.35GHz and 2.25GHz;

a 50% bandwidth about a centre frequency of 1.8GHz. Within this bandwidth corresponding output power from the amplifier is between 9 and 11.5Watts.

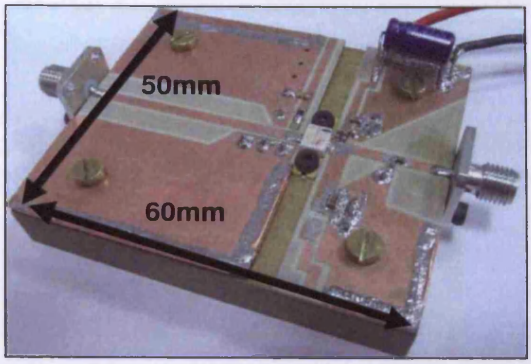

Fig. 5.5. Realised class-J amplifier - output matched only.

A comparison between the realised PA results and simulated efficiency from the nonlinear device model, set in the same impedance environment, is also shown in Fig. 5.6.

5.3.3 Analysis of Measured PA Performance

The results from this realised class-J design show a wide bandwidth of high-efficiency operation; however the optimum performance is not obtained all of the way to the top end of the initially desired 1.5-2.5GHz bandwidth, i.e. above 2.2GHz, efficiency and output power begin to roll off. Using the active harmonic load-pull test set-up to present the same impedance environment as the PA (up to the second harmonic), a verification of the expected performance could be ascertained, as in Fig. 5.6, allowing for further investigation into the reasons for the reduced performance, and hence indicate actions to take in order to improve the high-end performance.

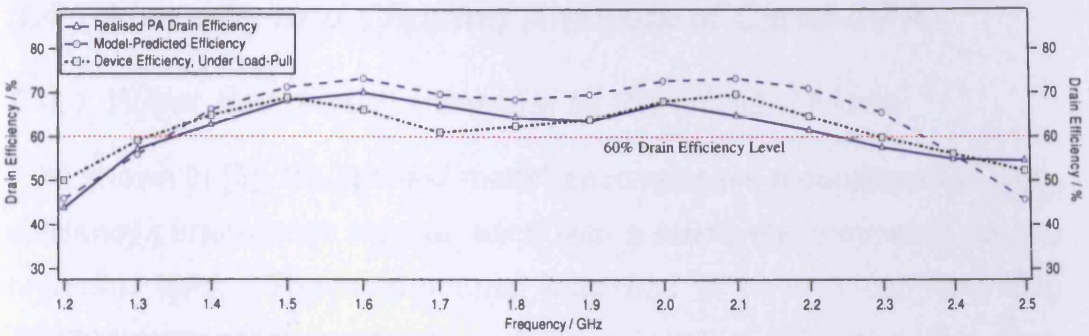

Fig. 5.6. P2dB drain efficiency for device under load-pull, device model-simulation and for the realised class-J PA (input unmatched) across a bandwidth of 1.2-2.5GHz.

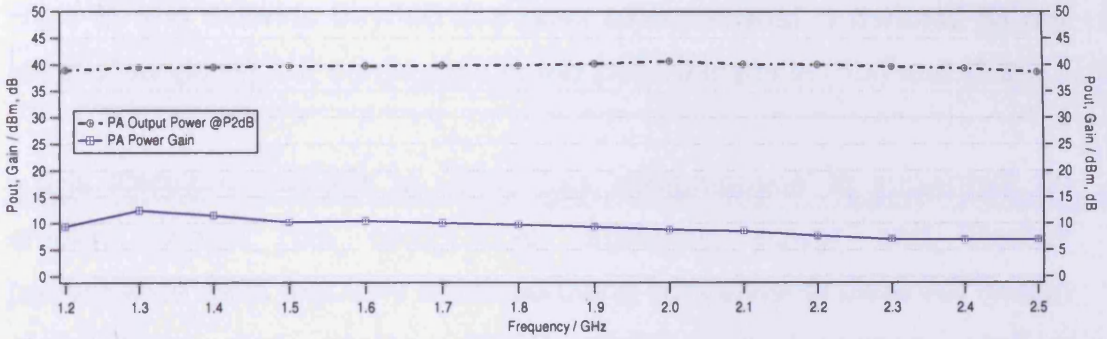

Fig. 5.7. Realised class-J PA output power and PA power gain (input unmatched, i.e. 50Ω) at P2dB across bandwidth of 1.2-2.5GHz.

The load-pull results - in which the fundamental and second harmonic load impedances were presented to the device - highlights the same trend in device drain efficiency, in particular the drop in efficiency above 2.2GHz.

By introducing refinements in the basic class-J theory [5] into the design approach, a new enhanced design was made, aimed not only at improving the high-end efficiency and output power, but also addressing linearity, and potentially, predistortability.

5.4 Linearity and Clipping Analysis of Class-J PA

5.4.1 Wider Bandwidth Potential of the Class-J Mode

As shown in [5], the 'class-J mode' encompasses a continuum of high-efficiency performance modes, each with a reactively terminated second harmonic load. The fundamental load has to have a corresponding reactive component in order to maintain a 'positive-definite', or non-zero-crossing voltage waveform. This continuum applies for second harmonic capacitive reactance terminations up to the short-circuit condition for class-B, and extends beyond this point towards what is denoted as the class-J* mode [5], i.e. conjugates of the class-J loads in (5.1) and (5.2).

It is therefore possible to utilise this 'design-space' to implement an amplifier which has comparable efficiency, power and linearity performance as is regularly obtained using conventional class-AB design methodology, but retains almost constant performance over a substantially extended bandwidth. To knowledge, such a design has never before been attempted on an *a priori* basis.

5.4.2 Use of 'Clipping Contours' for Quasi-Linear Design

The device output voltage, V_o, in a class-J PA can be written in the form [5];

$$V_o(\theta) = V_{dc} - V_{1r}\cos\theta + V_{1q}\sin\theta + \sum_n V_{nq}\sin(n\theta) \qquad (5.3)$$

$(\theta = \omega t)$

where in this case n = 2, and r and q denote the real and quadrature voltage components respectively.

If the minimum value of V_o approaches the device 'knee' (v_{min}) at any point in the RF cycle, the device current will start to 'clip', resulting in highly non-linear behaviour. Such clipping will clearly cause gain

compression, or AM-AM distortion, and if there is a significant phase angle between the fundamental components of current and voltage it is, in addition, a primary cause of AM-PM (amplitude-modulation-to-phase-modulation) distortion. These strongly non-linear effects not only cause spectral distortion but can also lead to increasing problems when attempting to linearise the device using input signal predistortion.

It is therefore of much relevance to examine the parametric dependency of the 'zero-crossing' behaviour of the voltage expression in (5.3). Even with the convenient approximation, $v_{min} = 0$, this is a mathematical problem of some complexity which has been analyzed in more detail elsewhere [5]. But for the present purpose it is possible to transform the clipping expression into a more simple graphical representation. If it is assume that the current waveform remains a classical reduced-conduction-angle class-AB form, the voltage parameters V_{1r}, V_{1q} and V_{2q} in (5.3) can be considered to be directly proportional to the corresponding impedances at the fundamental and second harmonic. With knowledge of the impedance environment, and the assumed current waveform, (5.3) can be evaluated to determine whether it has a positive or negative value. Figs. 5.8*(a)* and 5.8*(b)* show how this calculation can be plotted on an impedance plane; in this case the fundamental impedance (hence the V_{1r} and V_{1q} value) is varied across the entire Smith Chart plane, for specific fixed values of Z_{2f0} (hence V_{2q}). The shaded portions indicate the clipping regions where the voltage expression crosses zero at some point in the cycle.

The shaded regions, as shown in Figs. 5.8*(a)* and 5.8*(b)*, thus provide a design guide as to load conditions that should be avoided in the circuit design process. The line which delineates the clipping region is called the 'clipping contour'. This contour in effect shows the impedance conditions for which the voltage 'grazes' zero. However, the choice of

fundamental impedance will also determine the final power and efficiency.

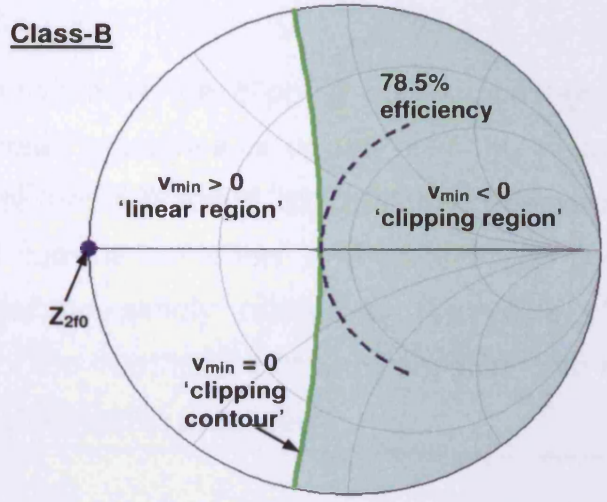

Fig. 5.8*(a)*. Class-B 'clipping contour' (solid trace) indicating fundamental loads for 'zero-grazing' v_{min} condition, with 'clipping region' shaded. 78.5% efficiency contour (dotted) also shown, indicating optimum load for linearity and efficiency.

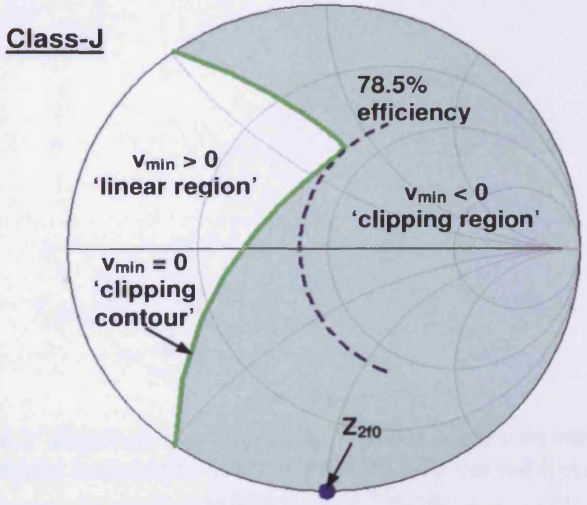

Fig. 5.8*(b)*. Class-J 'clipping contour' (solid trace) indicating fundamental loads for 'zero-grazing' v_{min} condition, shaded 'clipping region' and optimum load for class-J linearity and efficiency.

In principle, if the real part of the fundamental impedance is maintained at a constant value, equal to the device 'load-line' resistance, maximum power and efficiency will be maintained (corresponding to a fixed value of V_{1r} in (5.3)). This constant maximum efficiency contour is also plotted

(dotted traces) in Figs. 5.8*(a)* and 5.8*(b)*. In practice, of course, the only allowable maximum efficiency condition will be the one that sits on the 'clipping contour', which can be seen to be a singular point in each case.

Fig. 5.9 shows how the clipping contour changes as the value of second harmonic reactance is varied over the class-J range. It is of interest to note that in practice, although the clipping process will change the assumed current waveform, and as such the power and efficiency can no longer be simply related to the value of V_{1r} in (5.3), the continuation of the maximum efficiency condition into the 'clipping region' can often be observed in practice.

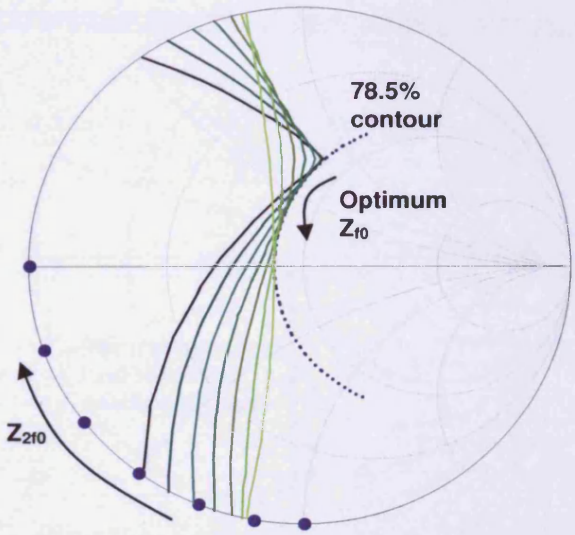

Fig. 5.9. $v_{min} = 0$ 'clipping contours' indicating optimum fundamental load for efficiency, as second harmonic load impedance is varied between the class-B and class-J conditions.

The plots in Figs. 5.8 and 5.9 define a design methodology for obtaining the best efficiency without forcing the device output voltage to 'graze' zero and thus display highly non-linear, clipped behaviour. To best knowledge, this is the first time such a methodology has been defined for high-efficiency RFPAs, and is proposed as an essential element in the design process for broader-band, high-efficiency PA design.

5.4.3 Practical Verification of Class-J Mode in High Power Devices - Effect of Second Harmonic (LP measurements)

Since for a broadband PA design - and especially PAs covering octave bandwidths - the high-end fundamental impedance tends towards the second harmonic impedance at the low-end of the band, it was necessary to observe the effect that a non-ideal (i.e. not purely reactive) second harmonic load impedance has on class-J efficiency [17]. This was carried out with a fixed fundamental load of 30+j30Ω ($I_{gen.}$-plane), fixed third harmonic impedance of 50Ω (package-plane) and for a fixed device bias condition of V_d=28V, I_{dsq}=100mA (deep AB, approximately 5% I_{dss}).

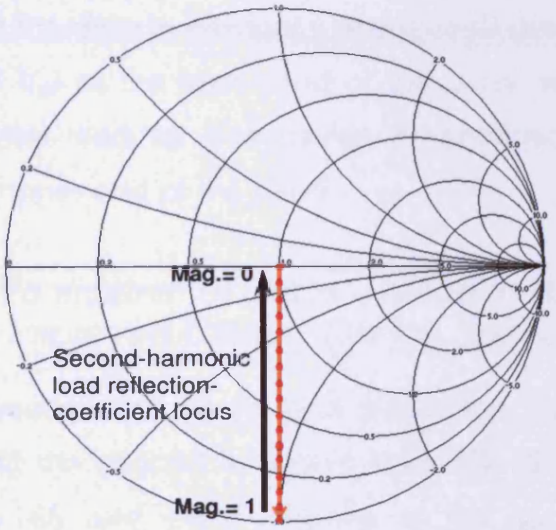

Fig. 5.10. Locus of second harmonic load reflection-coefficient variation.

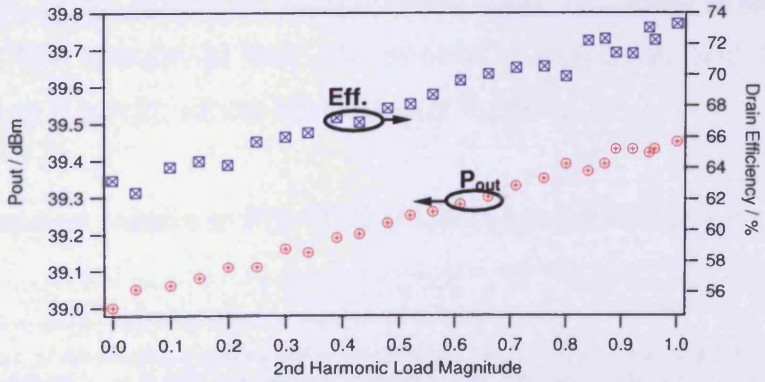

Fig. 5.11. Measured effect of the real component of second harmonic load on class-J output power and efficiency.

The results in Fig. 5.11 show a 10% decrease in efficiency, and almost 0.5dB reduction in output power[7] as the magnitude of the second harmonic load reflection-coefficient is varied from 1 to 0 at the $I_{gen.}$-plane. Fig. 5.10 indicates the locus of the second harmonic load during this test, indicating the fixed reflection coefficient angle was used in each of instance of the varied magnitude component. Although at first glance the result in Fig. 5.11 shows substantial degradation in performance, there is also the indication that the transition between the fundamental load and second harmonic load impedance across an octave bandwidth can be implemented in such a way as to not dramatically degrade the efficiency performance of a class-J PA operating across this frequency range, for example; a second harmonic load reflection-coefficient of magnitude 0.5 would suggest just 5% drop in efficiency and 0.25dB drop in output power (assuming a fixed V_d) at the lower end of the band, whilst still being a suitable fundamental load for this device if combined with a reactive component at the upper end of the band.

5.4.4 Practical Verification of Class-J Mode in High Power Devices - Improved Class-J Design Space LP Results

By following investigations in [5] and simulation findings in Section 5.4.2, the phase of the second harmonic load reflection coefficient was varied between +165 and −105 degrees at the $I_{gen.}$-plane (done so through applying output parasitic de-embedding), with magnitude 0.95 in each case. The optimum fundamental load for peak efficiency was targeted. The results of this are shown in Fig. 5.12, and have been carried out at a fundamental frequency of 1.8GHz.

The measured results in Fig. 5.12 show reasonable agreement with the

[7] This application, of developing a class-J-mode PA prototype, meant V_d was kept fixed at 28V for this test. Had V_d been allowed to vary with the second harmonic load reflection-coefficient P_{out} could have been expected to remain constant instead of degrading as the second harmonic reflection-coefficient magnitude was reduced, as in this case. For the purpose of analysing this design methodology for its potential for developing useable PAs, an appreciation was given to requirement of having a constant rail voltage level.

theoretical analysis of class-J and the proposed 'design space' for continuous high-efficiency performance, as the second harmonic and fundamental load impedances are allowed to vary away from the class-B case. Since the same theory can be applied to the 'complimentary' class-J* mode, corresponding to inductive second harmonic terminations, the potential for a broadband high-efficiency PA is clear.

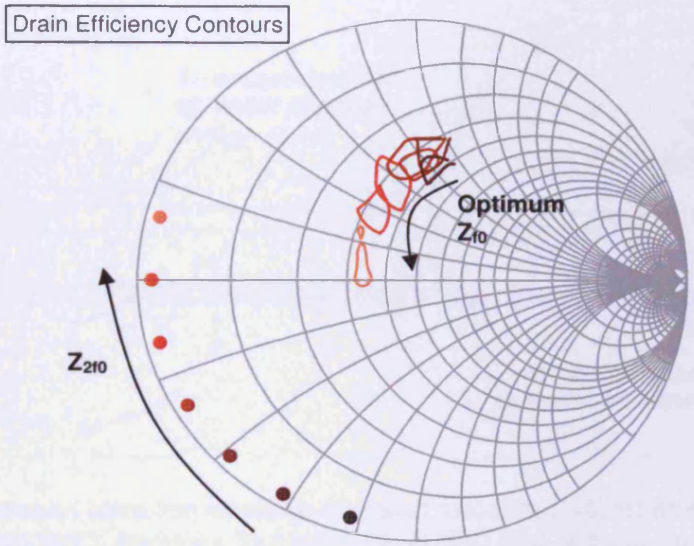

Fig. 5.12. Mapping the optimum (top 2%) efficiency contour as a function of changing second harmonic load impedance - $I_{gen.}$-plane impedances shown.

5.5 An Enhanced Design Following Extended Theory

5.5.1 Re-designing the Class-J Output Matching Network

Using the analysis found/developed in the previous section, an iteration of the initial matching network, using the same architecture as previous (Fig. 5.4), was made in line with the intention of 'moving' the fundamental loads that were encroaching on the 'clipping', or non-linear region of the Smith Chart, and more precise placement of the second harmonic load, in particular regards to the phase. This second design iteration is shown by the S-parameters of Fig. 5.13, giving a comparison with the first output matching design.

In the same way as previous, this improved design, following extended theoretical-based analysis, was used to predict the performance that could be expected from the PA by using active load-pull. These results showed improvement in efficiency at the higher frequency end of the bandwidth of operation as desired, above 2.2GHz, and as shown in Fig. 5.15.

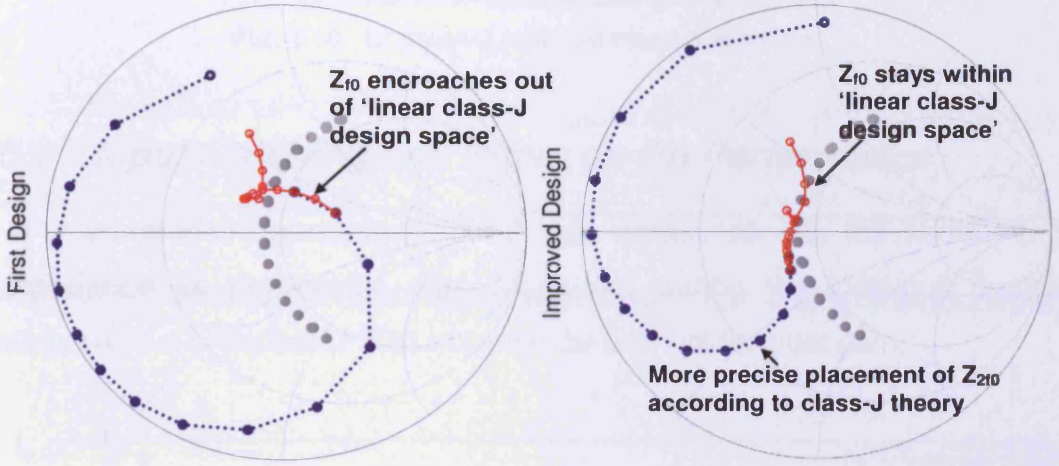

Fig. 5.13. Second iteration of class-J output matching (right) compared with first initial design (left), showing fundamental (solid) and second harmonic (dotted) load impedances between fundamental bandwidth of 1.2-2.6GHz.

5.5.2 Measured PA Performance following Improved Output Matching Network Design

In characterising the second realised PA, power sweeps were again conducted at 100MHz frequency spacing and the efficiency at P2dB (2dB gain compression point) was recorded, along with the output power and amplifier gain. These sets of results are displayed also in Fig. 5.15 and Fig. 5.16, along with the first design iteration results for comparison. Measured P2dB output power, as in Fig. 5.16, indicates the flat characteristic associated with this broadband design, at a value of 39.5 ± 0.5dBm (approximately 9-10W). The improvement in drain efficiency of the second iteration PA is evident in Fig. 5.15 between 2.3 and 2.6GHz, with up to 8% improvement obtained at 2.5GHz. Fig. 5.14 shows the improved class-J amplifier (see **Appendix A7** for full circuit).

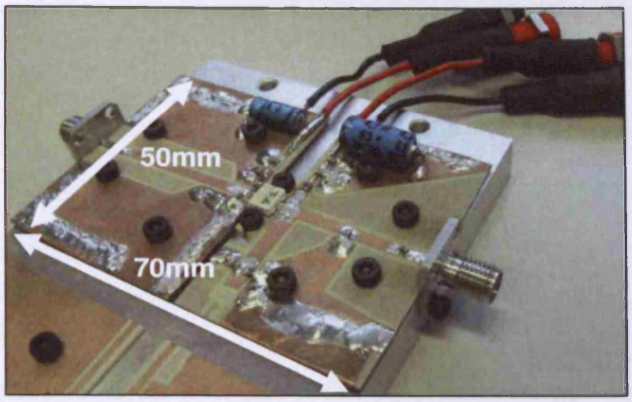

Fig. 5.14. Improved realised class-J amplifier.

5.6 *Input Matching and Effect on PA Performance*

For comparison purposes the PA was measured with the same input impedance as the device was measured during the load-pull design stage; with a broadband 50Ω impedance and not for best gain.

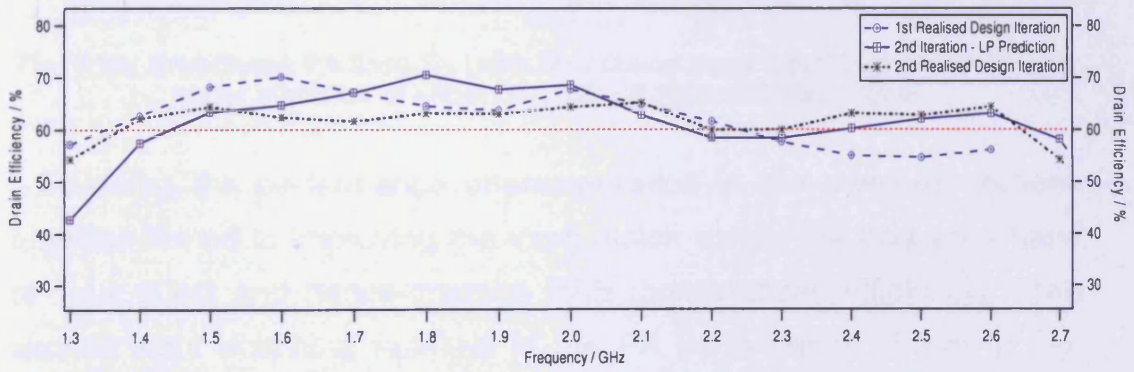

Fig. 5.15. Prediction and measurement of PA efficiency performance with enhanced output matching, compared with first class-J PA design performance.

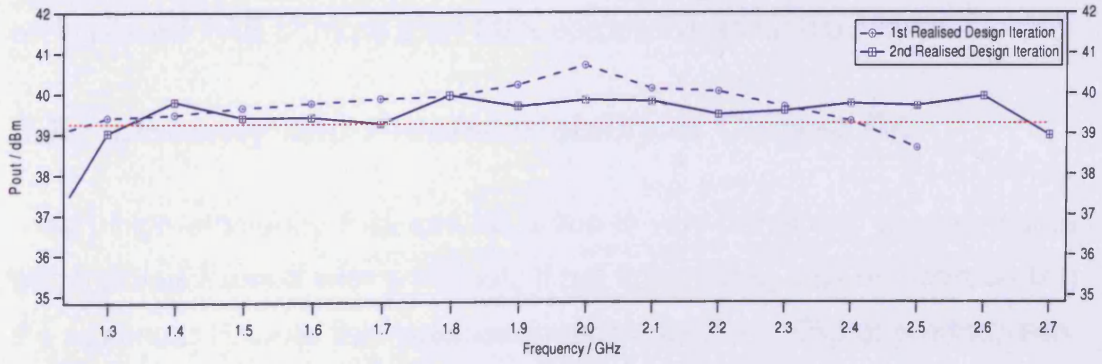

Fig. 5.16. Broadband measurement of PA output power performance with enhanced output matching, compared with first class-J PA design iteration

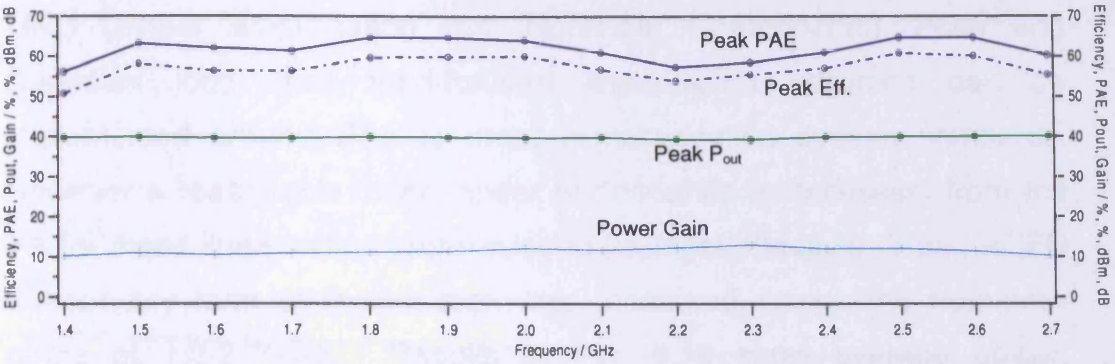

Fig. 5.17. Broadband measurement of PA performance with enhanced output matching, and broadband input matching

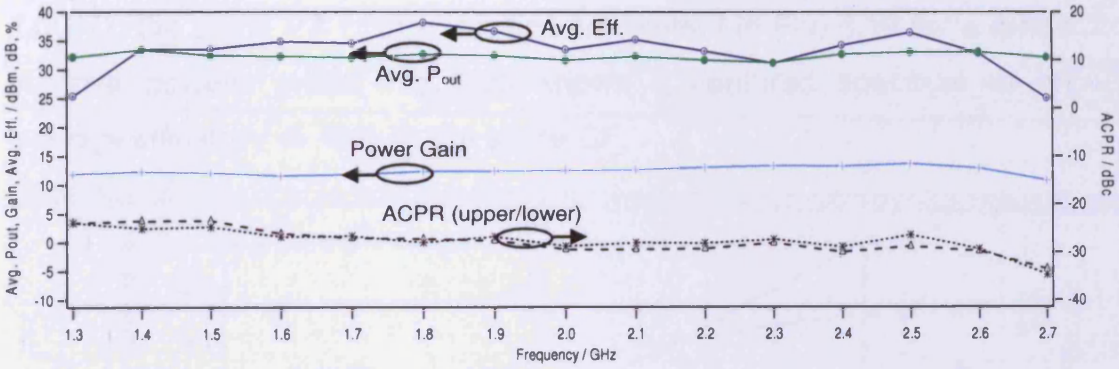

Fig. 5.18. Broadband PA linearity (with broadband input matching) characterised under stimulus of 5MHz BW, 8.51dB PAR, WCDMA signal

Following the performance characterisation in the previous sections attention turned to improving the input match across the frequency band of 1.4-2.6GHz and hence improve PAE (power-added efficiency). The applied input matching resulted in the PA performance shown in Fig. 5.17, including PAE. Here, gain of between 10.2-12.2dB across the bandwidth of 1.4-2.7GHz has been observed and hence has resulted in an improved PAE of more than 50% across the same bandwidth.

5.7 Linearity and Predistortability of Class-J PA

Very high-efficiency PAs can be prone to very non-linear characteristics which present users with a difficult, if not impossible, task of incorporating the nonlinear PA into the required linear transmitter. Digital predistortion,

LINC (LInear amplification with Nonlinear Components), Polar and Cartesian loop, and feed-forward linearisation schemes can be implemented around PAs to meet communication system standards. However a reasonable 'base' linear performance is necessary from the PA for these linearisation techniques to be most effective. Thus, ACPR without any form of linearisation was measured across the frequency range of 1.3-2.7GHz. Results in Fig. 5.18 show average power, efficiency and gain as well as worst-case upper and lower channel ACPR with drive power sufficient to cause 2dB peak compression. At a CF of 2.0GHz, the same PA characteristics are plotted in Fig. 5.19 for a range of drive powers, whilst Fig. 5.20 shows a captured spectrum at an average efficiency of 40% at the same CF.

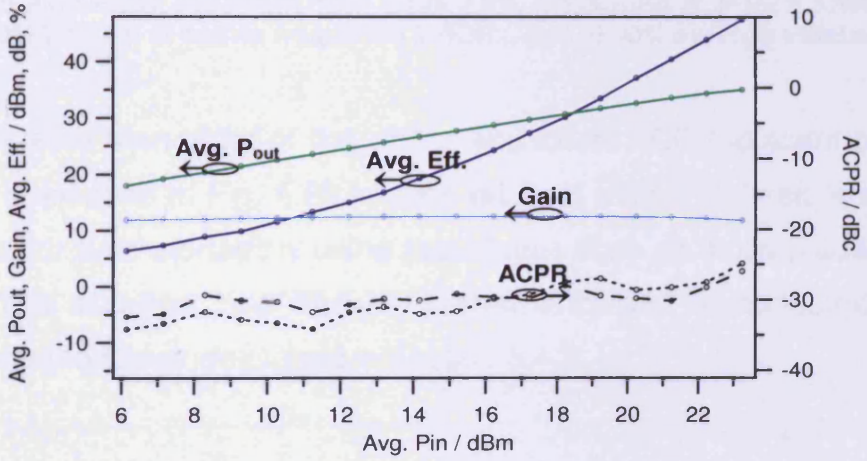

Fig. 5.19. Input matched class-J PA performance with a power-swept 5MHz BW, WCDMA signal at centre frequency of 2.0GHz.

The modulated signal applied, in order to characterise the PA linearity, was a WCDMA (wideband code division multiple access) signal of 3.84MHz signal bandwidth and 8.51dB PAR (peak-to-average ratio). The value of ACPR measured in these tests is defined as the integrated power across the adjacent 5MHz channel (upper or lower) as a ratio of the main 5MHz integrated channel power which the 3.84MHz incident signal occupies.

ACPR of close to –30dBc has been measured between 1.7-2.7GHz, decreasing to approximately –25dBc below 1.7GHz; this at the same time as the PA operating at more than 30% average efficiency.

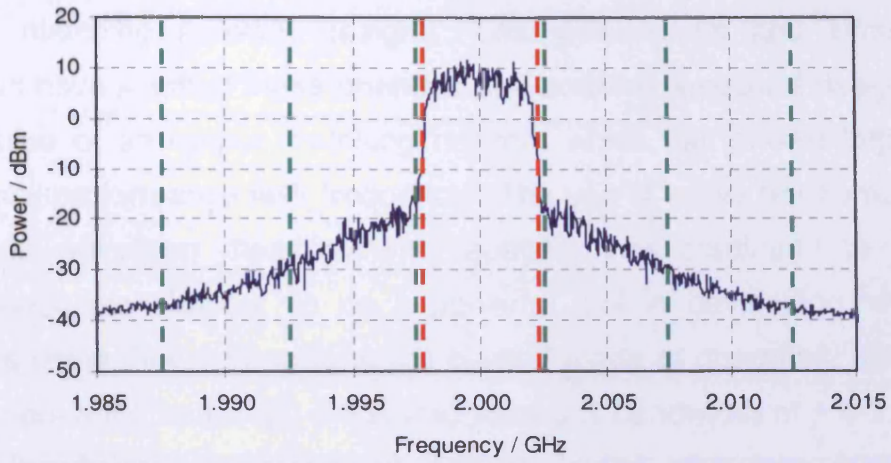

Fig. 5.20. Output spectrum from class-J PA, measuring ACP for a 3.84MHz WCDMA signal at centre frequency 2.0GHz, and at 40% average efficiency.

The relative symmetry of the upper and lower ACP (adjacent channel power) sidebands in Fig. 5.20 implies minimal memory effects and good potential for predistortability using techniques such as those presented in [6-7]. This excellent 'raw' linearity performance can be attributed to the design methodology described in section 5.4.2.

5.8 Chapter Summary

A fully realised class-J amplifier has demonstrated high-efficiency operation across a substantial bandwidth. Newly presented theory of class-J as a broadband mode has been applied in improving an initial output matching network design. Load-pull results and simulation analysis have justified these changes and enabled a second design and fabrication of an output matching network which has shown improved efficiency performance with frequency. The use of active harmonic load-pull and waveform measurement capability has continued to show, throughout this chapter, to be a powerful tool in developing real PA designs using theory specific to the class-J mode of operation. Efficient PA performance has been measured across a bandwidth of 1.4-2.6GHz (60% bandwidth, centered at 2GHz) whilst showing ACPR of approximately 25-30dBc across the entirety of this bandwidth at the measured P2dB compression level.

5.9 References

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Chapter 6. Conclusions

The research presented throughout this thesis has set out to find solutions to the ever-prominent requirement for enhancing the efficiency of wireless communications systems. This main objective of this research has been focused around the power amplifier stage, where improvements in efficiency here would make a significant impact to the overall efficiency of wireless communications as a whole.

In particular, attention has been turned to the use of nonlinear device characterisation systems with waveform measurement and active impedance environment control. With these types of nonlinear measurement capabilities only in their relative infancy, the ability to develop - and thus interest in - PA design methodologies which make novel use of the waveform-engineering technique is increasing. This work has demonstrated the advancement in developing such methodologies for obtaining efficiency enhanced PA modes of operation in packaged GaN HEMT power transistors.

The objective - of developing high-efficiency PA modes of operation in high power devices - tends to (certainly for single stage PAs) come hand-in-hand with the concept of multi-harmonic loading/matching requirements, thus often denoted by the term 'complex PA modes'. Complex modes of PA demand high attention to design detail when

considering the interaction between optimising device output power at the fundamental frequency whilst appropriately loading harmonic impedances. By implementing some of the highly advanced nonlinear waveform measurement techniques available, investigations into these complex modes of PA for efficiency enhancement have become more readily explored. Here, the class-F^{-1} and class-J modes have been investigated in detail, where three-harmonic and two-harmonic loading requirements respectively, have been actively implemented on a GaN HEMT. In unique combination with the ability to observe the current and voltage waveforms, synonymous in defining such modes of operation in theory, novel systematic design methodologies have been developed, and in both cases and for the first time, directly and fully utilised in the prototyping of several efficiency enhanced power amplifier units.

The importance of waveform measurements throughout this work has been demonstrated, not only during the course of the design and emulation of the PA modes, but also within analysing device operation through de-embedding measured package-plane waveforms to the device and current generator-planes, as well as right down to the final performance characterisation of the prototyped PAs, e.g. in terms of linearity and output spectral purity. However, it is the direct link that is provided between fundamental amplifier mode theory and practical implementation where these waveform-based design methodologies have revealed the strongest advantage over CAD-based designs using NL equation-based device models.

Chapters 3 and **4** detail a class-F^{-1} design methodology developed and initiated on a package higher power GaN HEMT device. Using the combined measurement tools of waveform capture and multi-harmonic active impedance environment control, the 81%+ drain-efficient PA emulations at 0.9 and 2.1GHz were also followed through fully to realised

prototype PAs operating at near-exact conditions. This is the first time that waveform measurement data obtained in this way has been used in the direct translation to a realisable working PA, with 'first-pass-success' also achieved in this design example.

Running parallel alongside the development of the design methodologies were CAD simulations making use of a nonlinear device model and simulated load-pull in an attempt to make comparisons between the optimised device operation obtained in reality and an equivalent PA design in CAD based around the model. With the additional harmonic impedance requirements adding a further dimension to the level of required accuracy of device model, comparisons between the realised 0.9GHz class-F^{-1} PA and NL model simulation (although in this case a more accurate model) did highlight some discrepancies in peak performance.

This same means of comparison was repeated when developing the class-J broadband high-efficiency PA design, detailed in **Chapter 5**. Following the realisation of this novel implementation of the newly discussed high-efficiency, but also more linear, class-J mode across almost an octave bandwidth, conclusions can start to be drawn as regards to the strong applicability of waveform measurement and engineering techniques in designing various modes of PA for use in modern wireless communication systems. This work has shown the practical implementation of waveform measurements and active multi-harmonic impedance control for two different modes of device operation within the same 10W GaN HEMT device. This has been demonstrated at multiple frequencies indicating clear potential for the development of design methodologies for use with nonlinear waveform-based measurement systems, such as the one used throughout this research, even for designed scaled (in frequency/power) beyond those values

presented here. And by characterising the intended device(s) prior to beginning the PA design, this enables a more measured means of selecting the most appropriate device for a particular application.

Overall, through the key application of waveform measurements and waveform-engineering, a means of improving the PA development cycle has been shown possible in response to the requirement to design more efficient PAs to enable next generation high data rate wireless communications schemes to become feasible. This both from a handset point of view, in terms of portability and the inherent draw on battery life with increased device functionality, but also base-station transmitters in terms of costs and reliability.

Chapter 7. Future Work

7.1 Future Work Extensions

The research described in this thesis has laid down a strong justification for the use of waveform-engineering in the performance-optimisation of the RFPA. Whilst the number of examples investigated through the course of this work is relatively modest, the concepts applied throughout all of these amplifier designs - whether high efficiency, very-high efficiency, narrowband or broadband - have proved to be more than satisfactory in achieving design and prototyping methodologies which have enhanced the PA development cycle.

The work here namely focuses around a 10W GaN packaged power transistor as the active DUT. Although the work has satisfied the initial targets set - that of developing waveform-engineering-based design methodologies beyond that previously described in literature - the viability of appropriately 'scaling' such techniques could potentially be further examined in future additions beyond this research.

The device utilised in many of the amplifier designs discussed in this thesis could be argued as having a natural optimum load tending towards the centre of a 50Ω Smith Chart, specifically favouring a broadband amplifier design, such as the one described in **Chapter 5**. This argument

in fact carries limited weight inasmuch as whatever fundamental load is being applied, all the design methodologies implemented make additional consideration for multi-harmonic loading criteria which most certainly is not close to a 50Ω optimum. However to further justify the claims made by the performance-optimisation processes developed in this research, future work would undoubtedly benefit from investigations into applying similar waveform-engineering design techniques on much higher power devices.

To date, such investigations have already begun [1], revealing highly promising results in a 45W GaN packaged HEMT, also manufactured by CREE. Fig. 7.1 shows results - although not fully optimised - of a class-F^{-1} mode. In this case the optimum fundamental load at the $I_{gen.}$-plane is far from 50Ω, yet the potential for optimised device performance remains clear from these initial investigations [1].

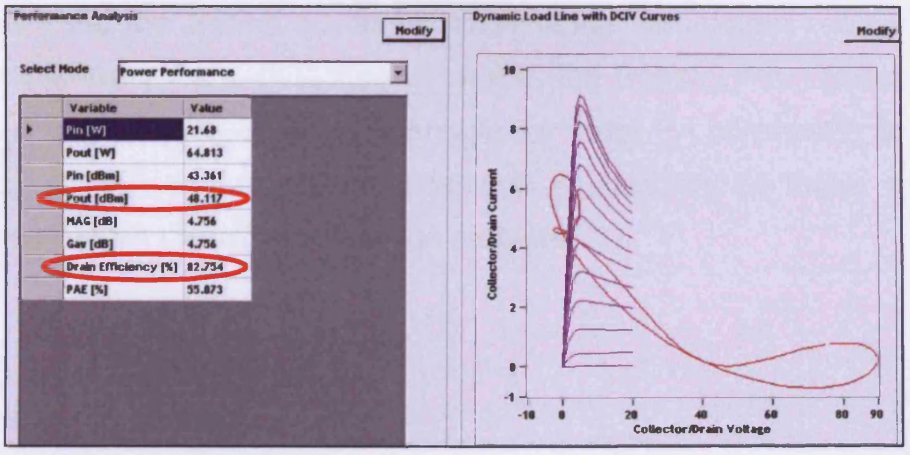

Fig. 7.1. Measured 'Class-F^{-1}-like' performance from a 45W GaN HEMT power transistor, including de-embedded dynamic load-line (right) [1].

Such high-power investigations have only recently become more easily pursuable within the Centre for High Frequency research group following enhancement of the measurement and active load-pull capabilities. Thus, extensions such as that in Fig. 7.1 [1] and also an injection PA

concept and envelope tracking analyses, reported in [2-3] respectively, are readily under investigation by current authors within the Centre for High Frequency Engineering research group.

Power amplifiers with "record high efficiency performance" are, and will continue to be published [4-5], each one 'beating' the previous by perhaps a couple of percentage points. However, many such types of work follow a less methodical approach in achieving an optimal PA design and show little novelty in the design concept utilised, often relying greatly on extreme device compression to the point of saturation. Where greater interest is arguably seen is in works such as [6], where - in this example - the PA mode theory for performance optimised modes is taken to the MMIC level.

Finally, benefits could potentially be seen from further work which investigates the implementation of efficiency/performance-optimised PA stages - via the use of waveform engineering techniques - within the current industry PA architecture of choice; the Doherty PA. Successful work in this area would arguably enable the wider PA community to gain further appreciation of the potential and applicability of these design practices within the wider PA design problem.

7.2 References

[1] Work carried out by J. Lees, Centre for High Frequency Engineering, Cardiff University, UK.

[2] A. Al-Muhaisen, P. Wright, J. Lees, P. J. Tasker, S. C. Cripps, J. Benedikt, "Novel Wide Band High-Efficiency Active Harmonic Injection Power Amplifier Concept," *2010 IEEE MTT-S International Microwave Symposium Digest*, Accepted for publication, June 2010.

[3] Z. Yusoff, S. Woodington, J. Lees, J. Benedikt, P. J. Tasker, S. Cripps, "Auxiliary Envelope Tracking as a Lineariser in Power Amplifier System," *Submitted to IET Electronics Letters*, 2010.

[4] M. Boers, A. Parker, N. Weste, "A GaN HEMT amplifier with 6-W output power and >85% power-added efficiency [Student Designs]," *IEEE Microwave Magazine,* Volume 9, Issue 2, pp. 106-110, April 2008.

[5] J. Kim, J. Moon, B. Kim, R. S. Pengelly, "A Saturated PA with High Efficiency [Technical Committee News]," *IEEE Microwave Magazine,* Volume 10, Issue 1, pp. 126-133, February 2009.

[6] S. Goto, T. Kunii, T. Oue, K. Izawa, A. Inoue, M. Kohno, T. Oku, T. Ishikawa, "A Low Distortion 25 W Class-F Power Amplifier Using Internally Harmonic Tuned FET Architecture for 3.5 GHz OFDM Applications," *IEEE MTT-S International Microwave Symposium Digest*, Volume, pp.1538-1541, June 2006.

Appendices

Appendix A1. CREE CGH40010F 10W gallium nitride HEMT datasheet.

CGH40010 Rev 1.4 Preliminary.

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Durham, NC 27703
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PRELIMINARY

CGH40010

10 W, RF Power GaN HEMT

Cree's CGH40010 is an unmatched, gallium nitride (GaN) high electron mobility transistor (HEMT). The CGH40010, operating from a 28 volt rail, offers a general purpose, broadband solution to a variety of RF and microwave applications. GaN HEMTs offer high efficiency, high gain and wide bandwidth capabilities making the CGH40010 ideal for linear and compressed amplifier circuits. The transistor is available in both screw-down, flange and solder-down, pill packages.

Package Types: 440166, & 440196
PN's: CGH40010F & CGH40010P

FEATURES

- Up to 4 GHz Operation
- 16 dB Small Signal Gain at 2.0 GHz
- 14 dB Small Signal Gain at 4.0 GHz
- 13 W typical P_{3dB}
- 65 % Efficiency at P3dB
- 28 V Operation

APPLICATIONS

- 2-Way Private Radio
- Broadband Amplifiers
- Cellular Infrastructure
- Test Instrumentation
- Class A, AB, Linear amplifiers suitable for OFDM, W-CDMA, EDGE, CDMA waveforms

RoHS COMPLIANT

Absolute Maximum Ratings (not simultaneous) at 25°C Case Temperature

Parameter	Symbol	Rating	Units
Drain-Source Voltage	V_{DSS}	84	Volts
Gate-to-Source Voltage	V_{GS}	-10, +2	Volts
Storage Temperature	T_{STG}	-55, +150	°C
Operating Junction Temperature	T_J	175	°C
Maximum Forward Gate Current	I_{GMAX}	4.0	mA
Soldering Temperature	T_S	245	°C
Thermal Resistance, Junction to Case [1]	$R_{\theta JC}$	5.0	°C/W

Note:
[1] Measured for the CGH40010F at P_{DISS} = 14 W.

Electrical Characteristics (T_C = 25°C)

Characteristics	Symbol	Min.	Typ.	Max.	Units	Conditions
DC Characteristics[4]						
Gate Threshold Voltage	$V_{GS(th)}$	-3.0	-2.5	-1.8	VDC	V_{DS} = 10 V, I_D = 3.6 mA
Gate Quiescent Voltage	$V_{GS(Q)}$	–	-2.0	–	VDC	V_{DS} = 28 V, I_D = 200 mA
Saturated Drain Current	I_{DS}	2.4	2.7	–	A	V_{DS} = 6.0 V, V_{GS} = 2.0 V
Drain-Source Breakdown Voltage	V_{BR}	84	100	–	VDC	V_{GS} = -8 V, I_D = 3.6 mA
Case Operating Temperature	T_C	-10	–	+105	°C	
Screw Torque	T	–	–	60	in-oz	Reference 440166 Package Revision 3
RF Characteristics (T_C = 25°C, F_0 = 3.7 GHz unless otherwise noted)						
Small Signal Gain	G_{SS}	13.5	14.5	–	dB	V_{DD} = 28 V, I_{DQ} = 200 mA
Power Output at 3 dB Compression	P_{3dB}	10	12.5	–	W	V_{DD} = 28 V, I_{DQ} = 200 mA
Drain Efficiency[1,2]	η	55	65	–	%	V_{DD} = 28 V, I_{DQ} = 200 mA, P_{3dB}
Output Mismatch Stress	VSWR	–	TBD	–	Ψ	No damage at all phase angles, V_{DD} = 28 V, I_{DQ} = 200 mA, P_{OUT} = 12 W CW
Dynamic Characteristics						
Input Capacitance	C_{GS}	–	5.00	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz
Output Capacitance	C_{DS}	–	1.32	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz
Feedback Capacitance	C_{GD}	–	0.43	–	pF	V_{DS} = 28 V, V_{gs} = -8 V, f = 1 MHz

Notes:
[1] Drain Efficiency = P_{OUT} / P_{DC}
[2] When tuned for best efficiency (see the applications chart in this data sheet).
[3] When tuned for best P_{1dB} (see the applications chart in this data sheet).
[4] Measured on wafer prior to packaging.

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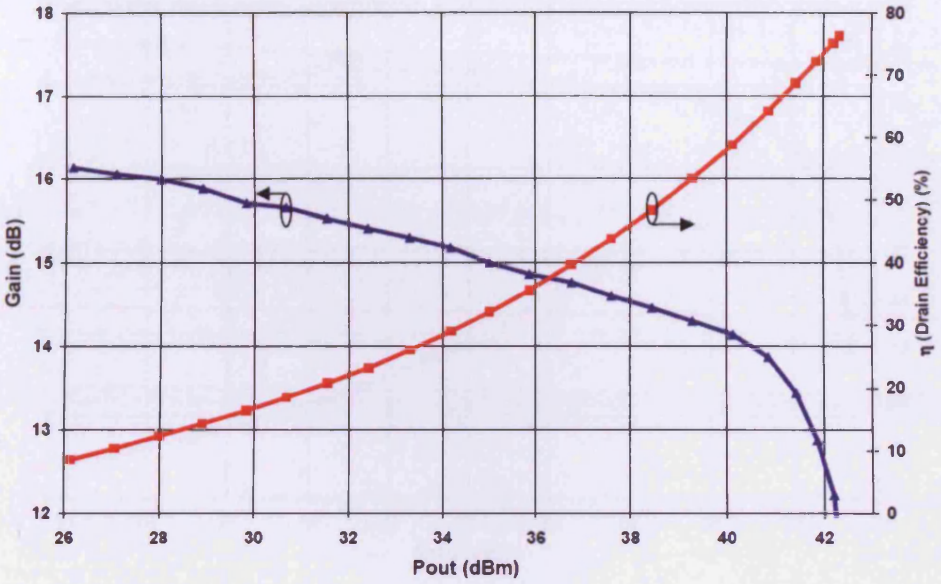
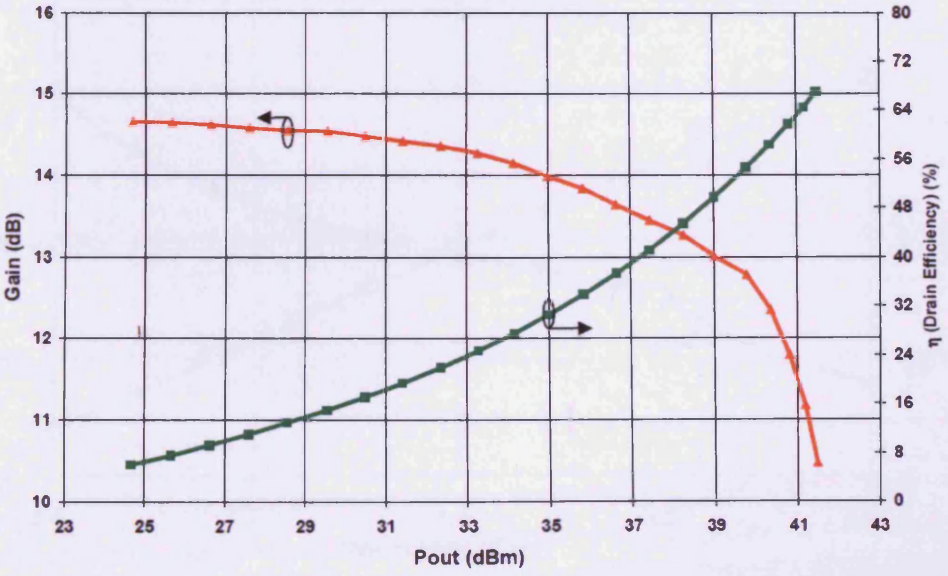
Typical Performance

Swept CW Data of CGH40010F vs. Output Power with Source and Load Impedances Optimized for Drain Efficiency at 2.0 GHz
V_{DD} = 28 V, I_{DQ} = 200 mA, Freq = 2.0 GHz



Swept CW Data of CGH40010F vs. Output Power with Source and Load Impedances Optimized for Drain Efficiency at 3.6 GHz
V_{DD} = 28 V, I_{DQ} = 200 mA, Freq = 3.6 GHz



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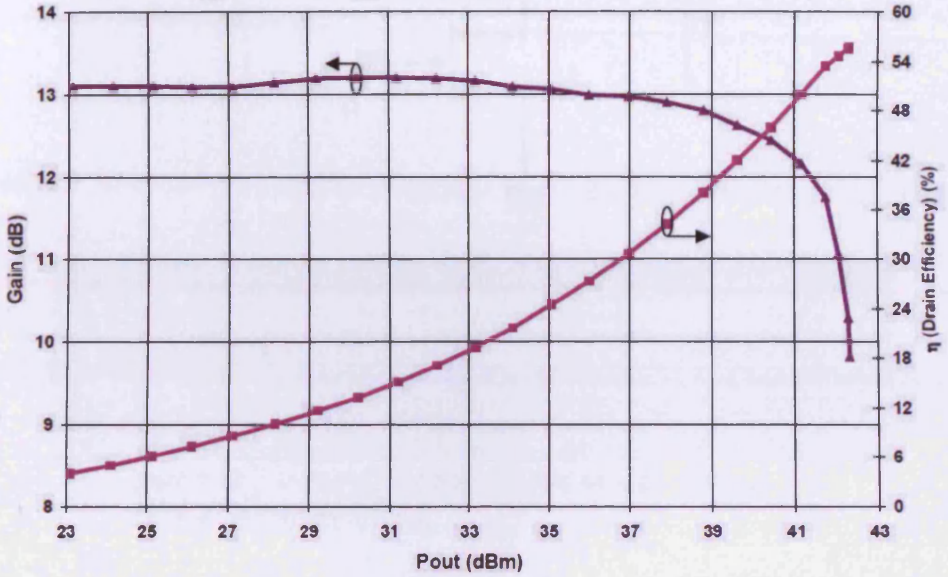
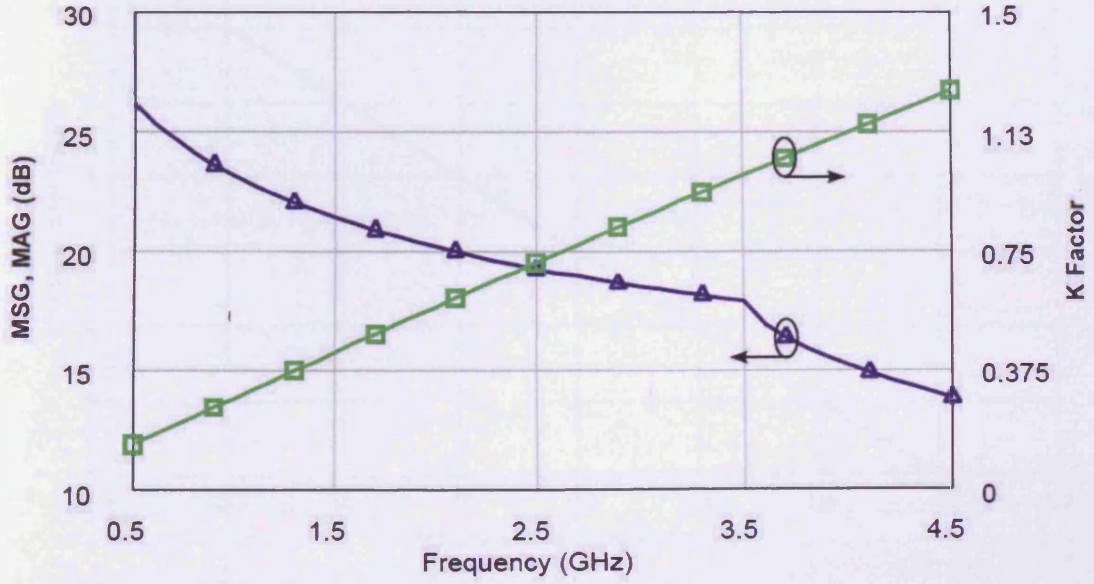
Typical Performance

Swept CW Data of CGH40010F vs. Output Power with Source and Load Impedances Optimized for P1 Power at 3.6 GHz
V_{DD} = 28 V, I_{DQ} = 200 mA, Freq = 3.6 GHz



Simulated Maximum Stable Gain, Maximum Available Gain and K Factor of the CGH40010F
V_{DD} = 28 V, I_{DQ} = 200 mA



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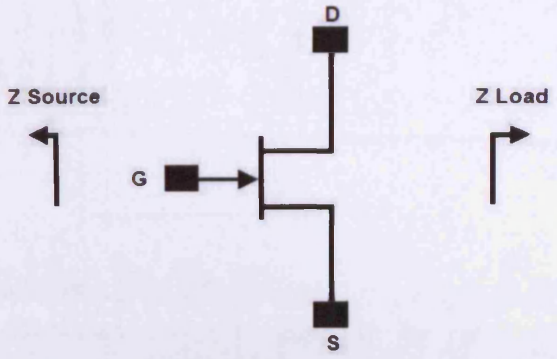
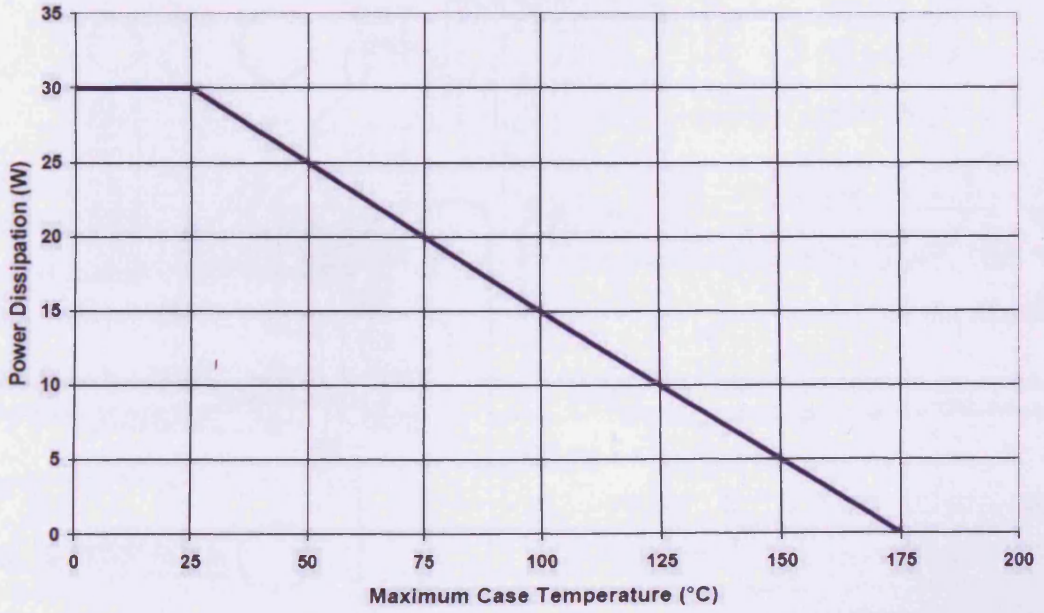
Source and Load Impedances



Frequency (MHz)	Z Source	Z Load
500	13.1 + j17	15.6 + j13.4
1000	9.2 + j10.7	12.96 + j8.25
1500	6.4 + j3.9	8.78 + j3.9
2500	4.0 - j4.0	6.37 - j0.1
3500	3.8 - j10.4	5.45 - j5.1

Note 1. V_{DD} = 28V, I_{DQ} = 200mA in the 440166 package.
Note 2. Optimized for P_{1dB}

CGH40010 Power Dissipation De-rating Curve



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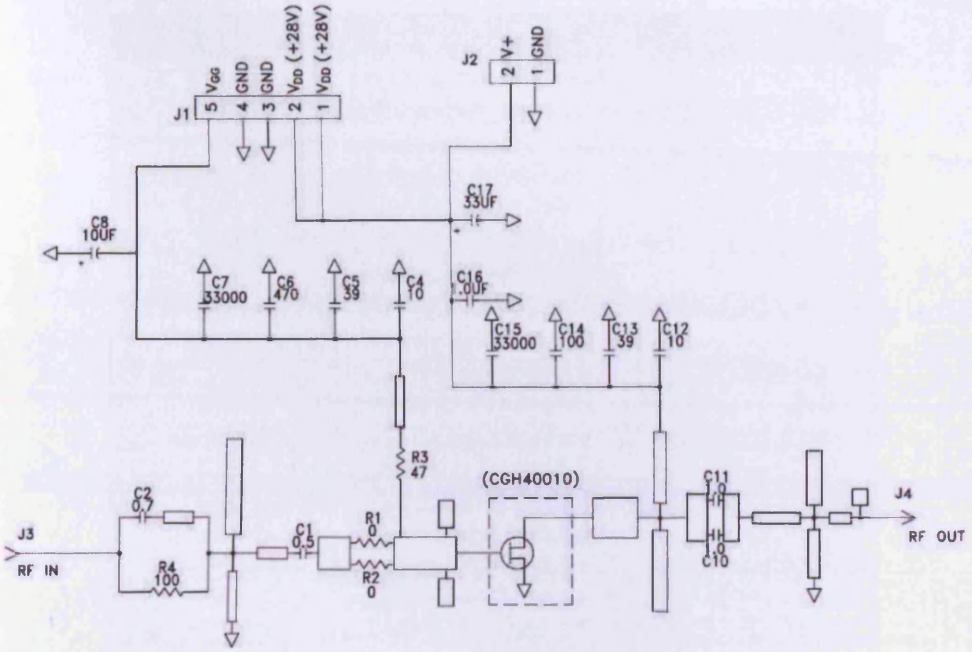
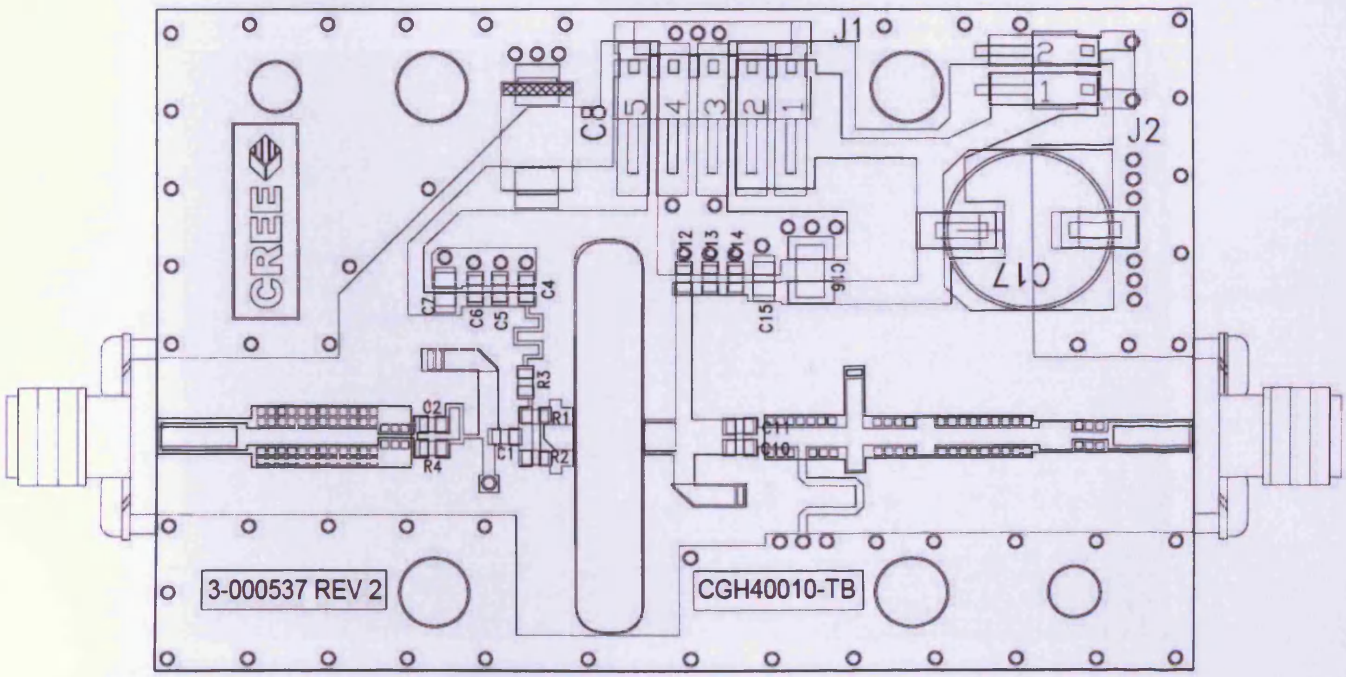
CGH40010-TB Demonstration Amplifier Circuit Schematic



CGH40010-TB Demonstration Amplifier Circuit Outline



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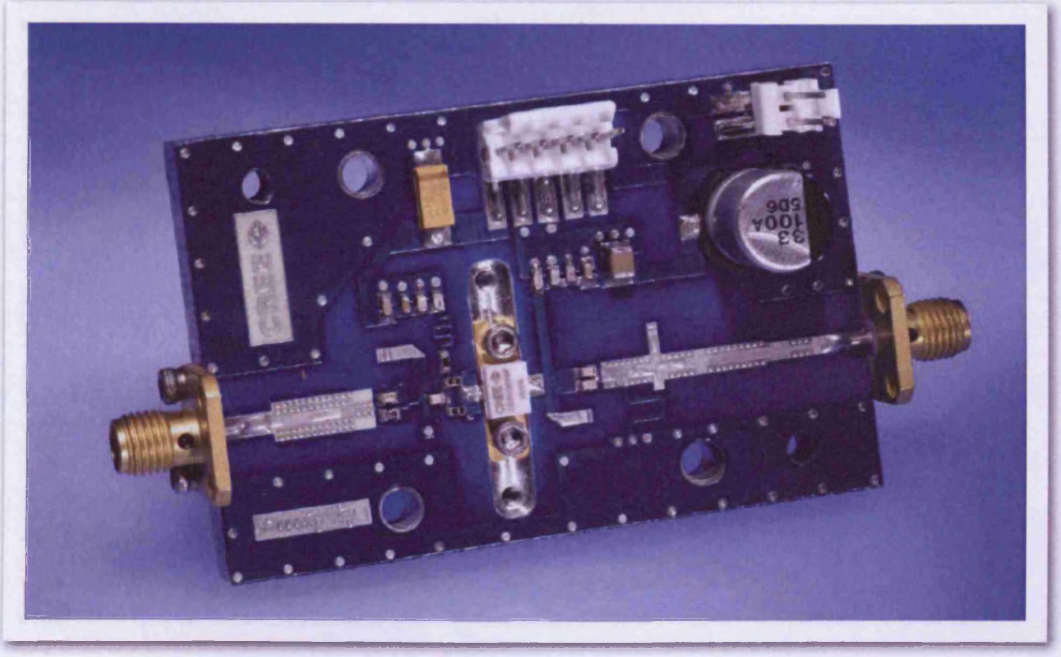
CGH40010-TB Demonstration Amplifier Circuit Bill of Materials

Designator	Description	Qty
R1,R2	RES,1/16W,0603,1%,0 OHMS	1
R3	RES,1/16W,0603,1%,47 OHMS	1
R4	RES,1/16W,0603,1%,100 OHMS	1
C6	CAP, 470PF, 5%,100V, 0603	1
C17	CAP, 33 UF, 20%, G CASE	1
C16	CAP, 1.0UF, 100V, 10%, X7R, 1210	1
C8	CAP 10UF 16V TANTALUM	1
C14	CAP, 100.0pF, +/-5%, 0603	1
C1	CAP, 0.5pF, +/-0.05pF, 0603	1
C2	CAP, 0.7pF, +/-0.1pF, 0603	1
C10,C11	CAP, 1.0pF, +/-0.1pF, 0603	2
C4,C12	CAP, 10.0pF,+/-5%, 0603	2
C5,C13	CAP, 39pF, +/-5%, 0603	2
C7,C15	CAP,33000PF, 0805,100V, X7R	2
J3,J4	CONN SMA STR PANEL JACK RECP	1
J2	HEADER RT>PLZ.1CEN LK 2 POS	1
J1	HEADER RT>PLZ .1CEN LK 5POS	1
Q1	CGH40010F or CGH40010P	1

CGH40010F-TB Demonstration Amplifier Circuit



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Typical Package S-Parameters for CGH40010F
(Small Signal, V_{DS} = 28 V, I_{DQ} = 100 mA, angle in degrees)

Frequency	Mag S11	Ang S11	Mag S21	Ang S21	Mag S12	Ang S12	Mag S22	Ang S22
500 MHz	0.8785	-143.68	12.55	101.09	0.0373	14.45	0.5687	-156.56
600 MHz	0.8740	-151.05	10.64	96.46	0.0380	10.48	0.5767	-161.57
700 MHz	0.8711	-156.75	9.22	92.62	0.0384	7.32	0.5817	-165.41
800 MHz	0.8690	-161.33	8.14	89.31	0.0386	4.68	0.5850	-168.51
900 MHz	0.8675	-165.16	7.27	86.35	0.0388	2.40	0.5872	-171.09
1.0 GHz	0.8664	-168.44	6.58	83.65	0.0390	0.38	0.5888	-173.31
1.1 GHz	0.8655	-171.33	6.00	81.14	0.0391	-1.46	0.5900	-175.27
1.2 GHz	0.8647	-173.91	5.52	78.77	0.0392	-3.15	0.5909	-177.04
1.3 GHz	0.8641	-176.25	5.12	76.51	0.0392	-4.73	0.5915	-178.65
1.4 GHz	0.8635	-178.42	4.77	74.33	0.0393	-6.23	0.5920	179.86
1.5 GHz	0.8630	179.56	4.46	72.22	0.0394	-7.65	0.5923	178.46
1.6 GHz	0.8625	177.66	4.20	70.17	0.0394	-9.02	0.5926	177.14
1.7 GHz	0.8620	175.86	3.96	68.15	0.0395	-10.35	0.5927	175.87
1.8 GHz	0.8615	174.13	3.75	66.18	0.0395	-11.63	0.5928	174.65
1.9 GHz	0.8610	172.47	3.57	64.23	0.0395	-12.89	0.5928	173.48
2.0 GHz	0.8606	170.86	3.40	62.31	0.0396	-14.11	0.5928	172.33
2.1 GHz	0.8601	169.29	3.25	60.41	0.0396	-15.32	0.5927	171.21
2.2 GHz	0.8597	167.76	3.11	58.53	0.0397	-16.50	0.5925	170.11
2.3 GHz	0.8592	166.26	2.99	56.66	0.0397	-17.67	0.5924	169.02
2.4 GHz	0.8587	164.79	2.87	54.80	0.0397	-18.83	0.5922	167.95
2.5 GHz	0.8582	163.33	2.77	52.94	0.0398	-19.97	0.5919	166.89
2.6 GHz	0.8577	161.89	2.67	51.10	0.0398	-21.10	0.5916	165.83
2.7 GHz	0.8571	160.46	2.58	49.26	0.0399	-22.23	0.5913	164.78
2.8 GHz	0.8566	159.04	2.50	47.42	0.0399	-23.35	0.5909	163.72
2.9 GHz	0.8560	157.62	2.42	45.58	0.0400	-24.46	0.5905	162.67
3.0 GHz	0.8555	156.21	2.35	43.74	0.0400	-25.57	0.5901	161.62
3.1 GHz	0.8549	154.80	2.29	41.91	0.0401	-26.68	0.5896	160.56
3.2 GHz	0.8542	153.38	2.23	40.07	0.0401	-27.79	0.5891	159.49
3.3 GHz	0.8536	151.97	2.17	38.23	0.0402	-28.89	0.5886	158.42
3.4 GHz	0.8529	150.54	2.12	36.38	0.0402	-29.99	0.5880	157.34
3.5 GHz	0.8523	149.11	2.07	34.53	0.0403	-31.10	0.5873	156.25
3.6 GHz	0.8516	147.68	2.02	32.68	0.0403	-32.20	0.5867	155.15
3.7 GHz	0.8508	146.23	1.98	30.81	0.0404	-33.31	0.5859	154.04
3.8 GHz	0.8501	144.77	1.94	28.95	0.0405	-34.41	0.5852	152.91
3.9 GHz	0.8493	143.30	1.90	27.07	0.0406	-35.52	0.5844	151.77
4.0 GHz	0.8486	141.81	1.86	25.18	0.0406	-36.64	0.5835	150.61
4.1 GHz	0.8478	140.31	1.83	23.29	0.0407	-37.76	0.5827	149.44
4.2 GHz	0.8469	138.79	1.79	21.38	0.0408	-38.88	0.5817	148.25
4.3 GHz	0.8461	137.25	1.76	19.46	0.0409	-40.01	0.5808	147.04
4.4 GHz	0.8452	135.70	1.73	17.53	0.0409	-41.15	0.5797	145.80
4.5 GHz	0.8443	134.12	1.71	15.59	0.0410	-42.29	0.5787	144.55

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(Small Signal, V_{DS} = 28 V, I_{DQ} = 200 mA, angle in degrees)

Frequency	Mag S11	Ang S11	Mag S21	Ang S21	Mag S12	Ang S12	Mag S22	Ang S22
500 MHz	0.884	-147.00	13.01	100.05	0.0316	14.05	0.6169	-163.03
600 MHz	0.881	-153.95	11.01	95.70	0.0320	10.50	0.6254	-167.20
700 MHz	0.878	-159.32	9.53	92.09	0.0323	7.70	0.6306	-170.47
800 MHz	0.877	-163.65	8.40	88.98	0.0326	5.39	0.6339	-173.14
900 MHz	0.875	-167.27	7.51	86.20	0.0327	3.41	0.6361	-175.43
1.0 GHz	0.874	-170.38	6.79	83.66	0.0328	1.67	0.6376	-177.42
1.1 GHz	0.873	-173.13	6.20	81.29	0.0329	0.11	0.6386	-179.22
1.2 GHz	0.873	-175.60	5.70	79.06	0.0330	-1.32	0.6393	179.14
1.3 GHz	0.872	-177.85	5.28	76.92	0.0331	-2.65	0.6397	177.62
1.4 GHz	0.872	-179.93	4.92	74.86	0.0332	-3.91	0.6398	176.19
1.5 GHz	0.871	178.12	4.61	72.86	0.0333	-5.10	0.6399	174.83
1.6 GHz	0.871	176.27	4.33	70.91	0.0334	-6.24	0.6398	173.53
1.7 GHz	0.870	174.52	4.09	69.00	0.0334	-7.33	0.6396	172.27
1.8 GHz	0.870	172.83	3.88	67.12	0.0335	-8.40	0.6393	171.05
1.9 GHz	0.869	171.21	3.69	65.27	0.0336	-9.43	0.6389	169.86
2.0 GHz	0.868	169.63	3.51	63.43	0.0337	-10.45	0.6385	168.70
2.1 GHz	0.868	168.09	3.36	61.62	0.0338	-11.44	0.6379	167.55
2.2 GHz	0.867	166.59	3.22	59.82	0.0339	-12.42	0.6374	166.42
2.3 GHz	0.867	165.11	3.09	58.03	0.0339	-13.39	0.6367	165.29
2.4 GHz	0.866	163.65	2.98	56.25	0.0340	-14.35	0.6360	164.18
2.5 GHz	0.866	162.21	2.87	54.47	0.0341	-15.30	0.6353	163.07
2.6 GHz	0.865	160.78	2.77	52.70	0.0342	-16.24	0.6345	161.97
2.7 GHz	0.864	159.36	2.68	50.93	0.0343	-17.18	0.6336	160.87
2.8 GHz	0.864	157.95	2.60	49.16	0.0345	-18.11	0.6327	159.76
2.9 GHz	0.863	156.54	2.52	47.39	0.0346	-19.05	0.6318	158.66
3.0 GHz	0.862	155.13	2.45	45.62	0.0347	-19.98	0.6308	157.55
3.1 GHz	0.862	153.73	2.38	43.84	0.0348	-20.91	0.6297	156.43
3.2 GHz	0.861	152.32	2.32	42.06	0.0349	-21.84	0.6286	155.31
3.3 GHz	0.860	150.91	2.26	40.28	0.0351	-22.78	0.6275	154.18
3.4 GHz	0.859	149.49	2.21	38.49	0.0352	-23.72	0.6263	153.04
3.5 GHz	0.859	148.06	2.16	36.70	0.0354	-24.66	0.6250	151.89
3.6 GHz	0.858	146.63	2.11	34.90	0.0355	-25.61	0.6237	150.73
3.7 GHz	0.857	145.18	2.07	33.09	0.0357	-26.56	0.6224	149.55
3.8 GHz	0.856	143.72	2.02	31.27	0.0358	-27.52	0.6210	148.37
3.9 GHz	0.855	142.25	1.98	29.44	0.0360	-28.48	0.6195	147.16
4.0 GHz	0.854	140.76	1.95	27.59	0.0361	-29.46	0.6181	145.94
4.1 GHz	0.853	139.26	1.91	25.74	0.0363	-30.44	0.6165	144.71
4.2 GHz	0.852	137.74	1.88	23.88	0.0365	-31.43	0.6150	143.46
4.3 GHz	0.851	136.20	1.85	22.00	0.0367	-32.44	0.6133	142.18
4.4 GHz	0.850	134.65	1.82	20.11	0.0369	-33.45	0.6117	140.89
4.5 GHz	0.849	133.07	1.79	18.21	0.0371	-34.47	0.6100	139.58

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Typical Package S-Parameters for CGH40010F
(Small Signal, V_{DS} = 28 V, I_{DQ} = 500 mA, angle in degrees)

Frequency	Mag S11	Ang S11	Mag S21	Ang S21	Mag S12	Ang S12	Mag S22	Ang S22
500 MHz	0.8907	-150.63	13.47	98.92	0.0258	13.90	0.6803	-168.90
600 MHz	0.8877	-157.10	11.37	94.88	0.0261	10.86	0.6882	-172.30
700 MHz	0.8858	-162.09	9.83	91.55	0.0264	8.52	0.6930	-175.03
800 MHz	0.8844	-166.13	8.66	88.67	0.0265	6.63	0.6960	-177.33
900 MHz	0.8834	-169.52	7.73	86.09	0.0267	5.05	0.6980	-179.33
1.0 GHz	0.8825	-172.46	6.99	83.72	0.0268	3.68	0.6992	178.87
1.1 GHz	0.8818	-175.05	6.38	81.52	0.0269	2.47	0.7000	177.23
1.2 GHz	0.8812	-177.40	5.87	79.43	0.0270	1.37	0.7004	175.70
1.3 GHz	0.8806	-179.54	5.44	77.43	0.0271	0.37	0.7006	174.26
1.4 GHz	0.8801	178.46	5.07	75.51	0.0272	-0.57	0.7006	172.89
1.5 GHz	0.8795	176.58	4.74	73.63	0.0274	-1.45	0.7004	171.56
1.6 GHz	0.8790	174.80	4.46	71.81	0.0275	-2.29	0.7001	170.28
1.7 GHz	0.8785	173.10	4.22	70.01	0.0276	-3.10	0.6996	169.03
1.8 GHz	0.8779	171.47	4.00	68.24	0.0277	-3.88	0.6991	167.81
1.9 GHz	0.8774	169.88	3.80	66.50	0.0278	-4.64	0.6984	166.61
2.0 GHz	0.8768	168.34	3.63	64.77	0.0280	-5.38	0.6977	165.42
2.1 GHz	0.8762	166.83	3.47	63.06	0.0281	-6.11	0.6969	164.24
2.2 GHz	0.8756	165.35	3.33	61.36	0.0283	-6.83	0.6961	163.07
2.3 GHz	0.8750	163.89	3.20	59.66	0.0284	-7.55	0.6952	161.91
2.4 GHz	0.8743	162.45	3.08	57.97	0.0286	-8.26	0.6942	160.75
2.5 GHz	0.8737	161.03	2.97	56.28	0.0288	-8.96	0.6931	159.60
2.6 GHz	0.8730	159.62	2.87	54.60	0.0289	-9.67	0.6920	158.44
2.7 GHz	0.8723	158.21	2.78	52.92	0.0291	-10.38	0.6908	157.28
2.8 GHz	0.8715	156.81	2.69	51.23	0.0293	-11.10	0.6896	156.12
2.9 GHz	0.8708	155.41	2.61	49.54	0.0295	-11.81	0.6883	154.95
3.0 GHz	0.8700	154.01	2.54	47.85	0.0297	-12.54	0.6869	153.78
3.1 GHz	0.8692	152.61	2.47	46.15	0.0299	-13.27	0.6855	152.60
3.2 GHz	0.8683	151.21	2.41	44.45	0.0301	-14.00	0.6840	151.41
3.3 GHz	0.8674	149.80	2.35	42.74	0.0304	-14.75	0.6825	150.21
3.4 GHz	0.8665	148.38	2.30	41.02	0.0306	-15.51	0.6809	149.00
3.5 GHz	0.8656	146.96	2.25	39.30	0.0309	-16.27	0.6793	147.78
3.6 GHz	0.8647	145.53	2.20	37.56	0.0311	-17.06	0.6776	146.54
3.7 GHz	0.8637	144.08	2.15	35.81	0.0314	-17.85	0.6758	145.29
3.8 GHz	0.8627	142.62	2.11	34.06	0.0316	-18.65	0.6740	144.03
3.9 GHz	0.8617	141.15	2.07	32.29	0.0319	-19.47	0.6722	142.75
4.0 GHz	0.8606	139.66	2.04	30.50	0.0322	-20.31	0.6703	141.46
4.1 GHz	0.8595	138.16	2.00	28.71	0.0325	-21.16	0.6683	140.14
4.2 GHz	0.8584	136.63	1.97	26.90	0.0328	-22.03	0.6663	138.81
4.3 GHz	0.8573	135.09	1.94	25.07	0.0331	-22.92	0.6643	137.46
4.4 GHz	0.8562	133.53	1.91	23.23	0.0334	-23.82	0.6622	136.09
4.5 GHz	0.8550	131.95	1.88	21.38	0.0338	-24.75	0.6600	134.69

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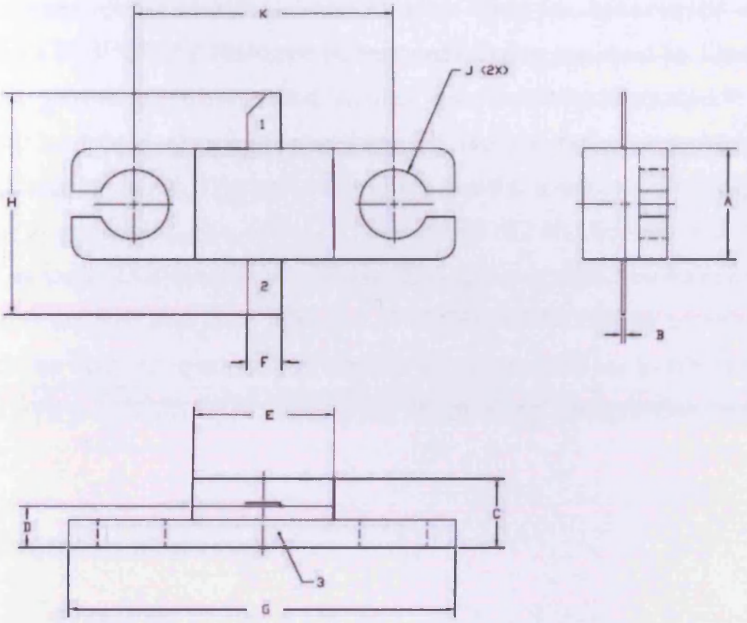
Product Dimensions CGH40010F (Package Type — 440166)



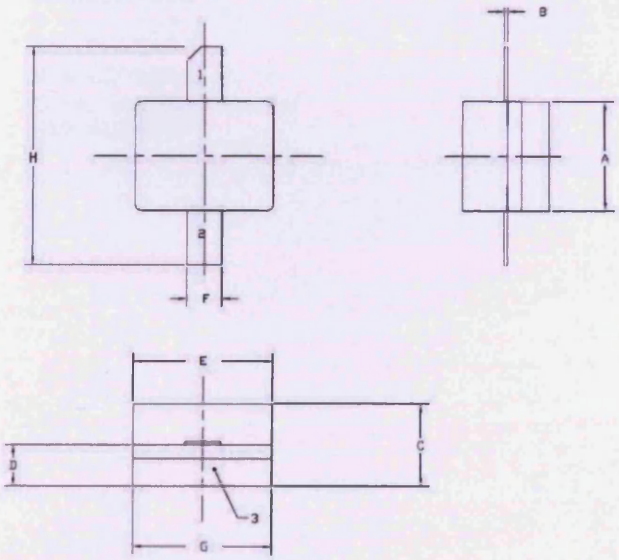
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. ADHESIVE FROM LID MAY EXTEND A MAXIMUM OF 0.020" BEYOND EDGE OF LID.
4. LID MAY BE MISALIGNED TO THE BODY OF THE PACKAGE BY A MAXIMUM OF 0.008" IN ANY DIRECTION.
5. ALL PLATED SURFACES ARE NI/AU

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.155	0.165	3.94	4.19
B	0.004	0.006	0.10	0.15
C	0.115	0.135	2.92	3.43
D	0.057	0.067	1.45	1.70
E	0.195	0.205	4.95	5.21
F	0.045	0.055	1.14	1.40
G	0.545	0.555	13.84	14.09
H	0.280	0.360	7.87	8.38
J	ø .100		2.54	
K	0.375		9.53	

PIN 1. GATE
PIN 2. DRAIN
PIN 3. SOURCE

Product Dimensions CGH40010P (Package Type — 440196)



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
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5. ALL PLATED SURFACES ARE NI/AU

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.155	0.165	3.94	4.19
B	0.003	0.006	0.10	0.15
C	0.115	0.135	2.92	3.17
D	0.057	0.067	1.45	1.70
E	0.195	0.205	4.95	5.21
F	0.045	0.055	1.14	1.40
G	0.195	0.205	4.95	5.21
H	0.280	0.360	7.112	9.114

PIN 1. GATE
PIN 2. DRAIN
PIN 3. SOURCE

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Appendix A2. TRL calibration notes.

Design and use of TRL calibration standards for RF power transistor characterisation.

Design and use of TRL calibration standards for RF power transistor characterisation.

A device fixture was developed with the intention of physically accommodating the packaged GaN HEMT device - used throughout this work - whilst maintaining a broadband 50Ω passive impedance environment at the device terminals. In order to enable a measurement reference plane to be defined at the input and output interfaces of the device package, a calibration routine is required that will remove the magnitude and phase effects of the fixture lines and connectors. This requires three TRL (thru-reflect-line) calibration standards to be made to very specific requirements: a shorted 'reflect' standard of physical phase length the same as that of one half of the device fixture; a 'thru' standard, equal to the phase length of the two fixture halves placed end-to-end; and a 'line' standard of a specified phase length (on top of the phase length of the thru standard) between 20 and 160° across the measurement frequency range required.

Fig. A2.1 shows the set of calibration standards made, along with the fixture to which the standards refer. Each standard and half of the fixture has its own set of SMA connectors which, for the purpose of the calibration, are assumed (but with due caution) to be identical.

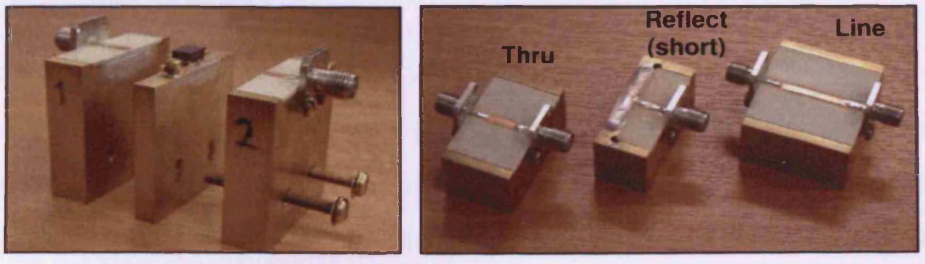


Fig. A2.1. Device fixture (left) and TRL calibration standards for use in measuring the DUT (CGH40010F)

A thermoset microwave laminate from Rogers' TMM® range was selected which, when designing a 50Ω impedance transmission line, resulted in a line width of similar dimensions to that of the DUT tab. This would minimise the effect of any impedance mismatch between interfaces allowing for a clearer definition of the transitional planes. Fig. A2.2 shows a screen shot of the ADS 'LineCalc' tool which was used in the design of the dimensions of the microstrip transmission line width, and line-standard length.

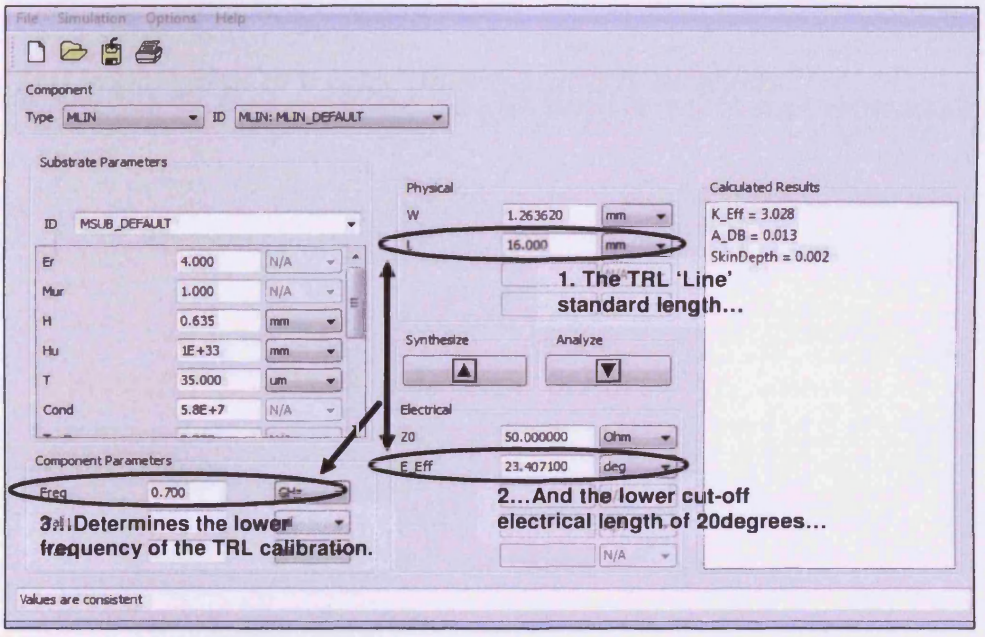


Fig. A2.2. Using ADS 'LineCalc' to design the fixture and calibration standard microstrip lines on Rogers TMM® microwave laminate.

With the standards complete, and by measuring each of the calibration standards in turn to perform the TRL calibration, there is enough information for the measurement system utilised in this research to generate a set of error coefficients which will define the input and output halves of the fixture in which the DUT will sit, and thus provide a measurement reference plane at the device package interface.

Appendix A3. Device stability analysis procedures directly from waveform-measurement-based S-parameter capture.

The importance of a prior device stability analysis.

The Importance of a Prior Device Stability Analysis

Device stability analysis is a considerable part of the device characterisation process. Since high gain GaN devices are being investigated in this research, problems with oscillations can, and have, occurred with every device utilised. As a result it was imperative that a means of finding the root cause of any oscillation, as well as investigating how to eliminate them, was carried out prior to any amplifier designs.

By measuring S-parameters for a device at the bias conditions intended for use, simulations could be performed on the device S-parameter model in ADS. This way any stability issues could be highlighted and possible solutions implemented. In the example here the DUT bias point is set to V_{ds}=28V and I_{dsq}=225mA and full two-port S-parameter measurements between 0.5 and 6GHz (step size 0.05GHz) were taken using a small-signal RF input. The data obtained was then used to model the devices small signal behaviour and look at stability across the 0.5 to 6GHz frequency range. The simulation schematic is shown in Fig. A3.1

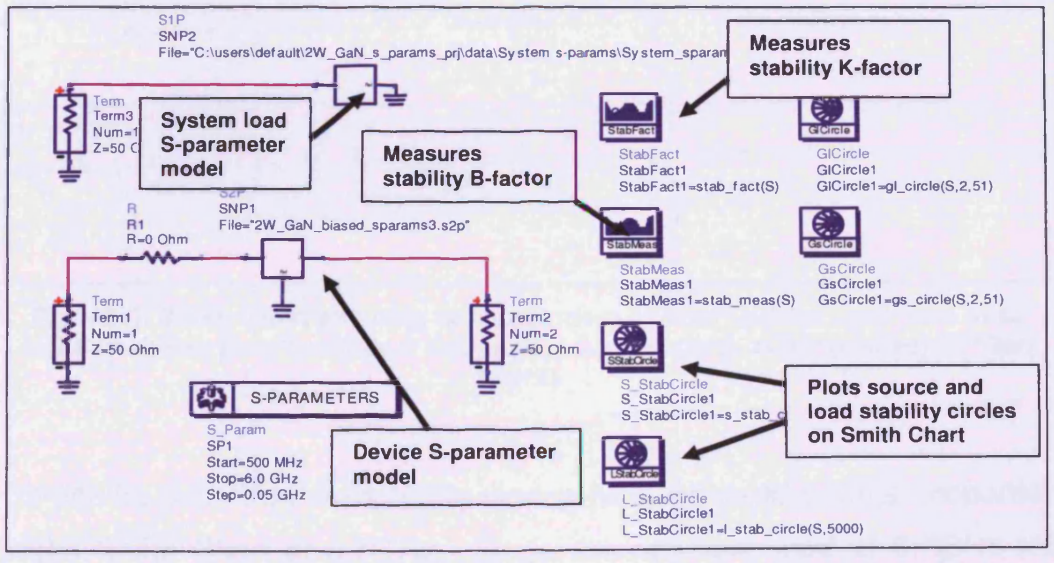


Fig. A3.1. ADS schematic used to simulate the DUT and look at stability.

Results of the stability analysis on the DUT show that stability becomes an issue for this device when operating at just below 2GHz. This is indicated in the plot of the stability 'K'-factor in Fig. A3.2, where it drops below 1 at approximately 1.8GHz.

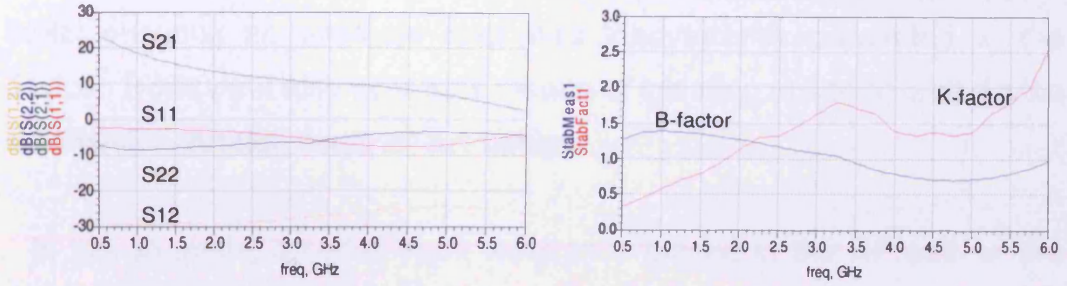


Fig. A3.2. Plot showing 2-port S-parameters (left) and plot of the K- and B-factors (right) across 0.5 to 6GHz for the DUT.

Having found this result, the DUT S-parameter model was looked at for different frequencies (0.7, 1.0 and 2.1GHz) and in particular the encroachment of the source and load stability circles onto the Smith chart. This is shown in Fig. A3.3.

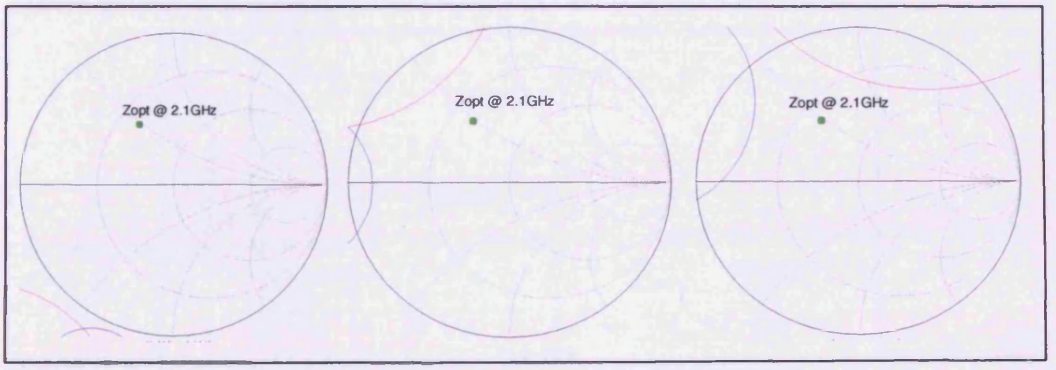


Fig. A3.3. Smith Chart showing encroachment of source (blue) and load (red) stability circles as a function of frequency; 2.1GHz (left), 1GHz (centre), 0.7GHz (right).

It can be seen that the stability circles have covered a large proportion of the Smith Chart at 0.7GHz. Since the optimum load at 0.7GHz will have moved from the position of that at 2.1GHz, it may well be that the

optimum load at 0.7GHz lies within an unstable region of the Smith Chart.

Overall the simulations provide an indication and means of guidance as to possible stability issues that may arise. Using this information it enabled subsequent large-signal device characterisation to be carried out whilst ensuring no unstable load was inadvertently presented to the device. However it also acts as a means of initiating unconditional device stabilisation through linear circuit design.

In this example, a series-input resistance placed in the RF path of the device (see Fig. A3.1) was added to the S-parameter simulation and its value varied in order to look at the effect on the placement of the stability circles. From this simulation it was found that a 15Ω resistance was sufficient to keep the stability circles outside of the unity Smith Chart between 0.5 and 6GHz, with the inherent downside of a 1.6dB reduction in device small-signal gain (S21). The traces of the K- and B-factors for this stabilised case are shown in Fig. A3.4.

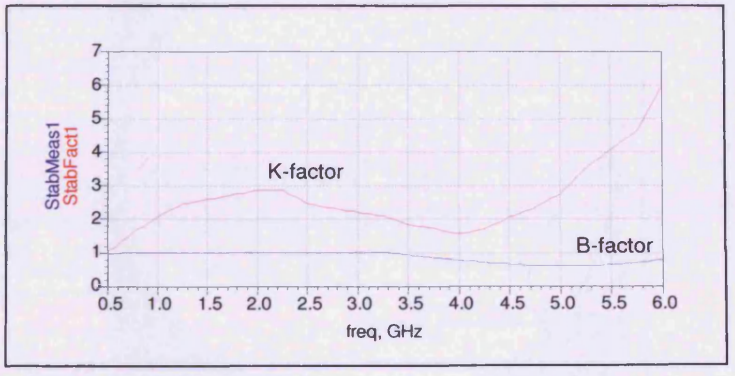


Fig. A3.4. Plot of K-factor & B-factor after stabilising.

In another example, feedback and input stabilisation methods were investigated enabling each method's design suitability to be compared.

Fig. A3.5 shows the schematic views of two stabilising techniques. The

series resistor in parallel with a capacitor was chosen for implementation in the design since this arrangement (once optimised) had the greater effect on ensuring unconditional stability whilst having the least effect on the device gain around the intended band of operation.

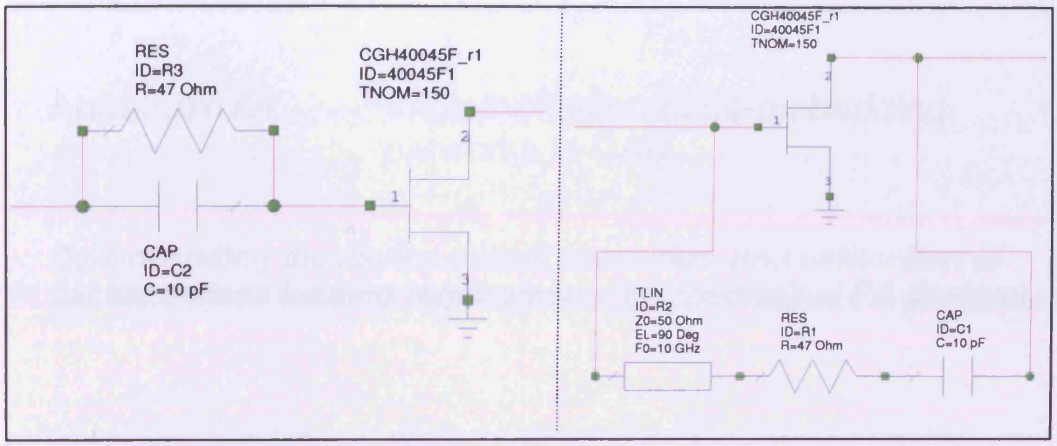


Fig. A3.5. Series-input stabilising (left) and feedback stabilisation (right).

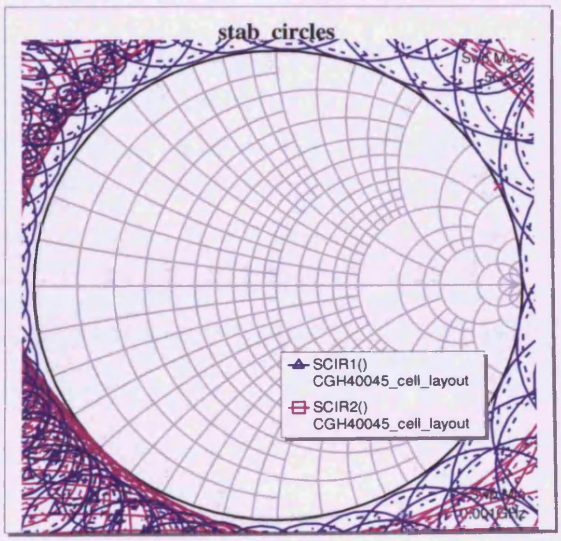


Fig. A3.6. Smith Chart shows unconditional stability with series input stabilisation.

Appendix A4. Implementation of de-embedding networks in CAD.

De-embedding the device output parasitics, and estimation of package-plane loading requirements for theoretical PA designs.

De-embedding the device output parasitics, and estimation of package-plane loading requirements for theoretical PA designs

The objective of modelling the output parasitic elements of a packaged RF transistor is to ultimately enable a means of negating the effect of these parasitics and thus derive a reference plane as close as possible to the 'ideal current-generator' of the real device. As well as this, the 'negative version' of the parasitic model enables the transformation of the ideal or 'textbook' loading requirements - defined for specific PA modes of operation - backwards from the current-generator plane to the more-easy-to-calibrate DUT-package reference plane.

Taking the example of the class-F^{-1} mode investigated in this thesis, a simple S-parameter simulation can be performed which, for example, can quickly predict - prior to any load-pull investigation - the reflection coefficients required at the DUT package-plane for an 'open' termination at $2f_0$ and a 'short' termination at $3f_0$ at the current generator plane respectively.

Fig. A4.1 shows the parasitic model determined for the DUT (CREE's CGH40010F), modelled intrinsically (e.g. output capacitance C_{ds}) and also extrinsically (e.g. bonding wires). By introducing an open circuit at port-1 of the negated version (i.e. all element values are "–ve") of this parasitic model, and analysing the impedance with a 50Ω reference terminal from port-2, the 'seen impedance' from the package-plane is thus the required reflection coefficient to establish the second harmonic open termination. The same procedure can be carried out for determining the package-plane impedance needed to facilitate the short termination at the third harmonic.

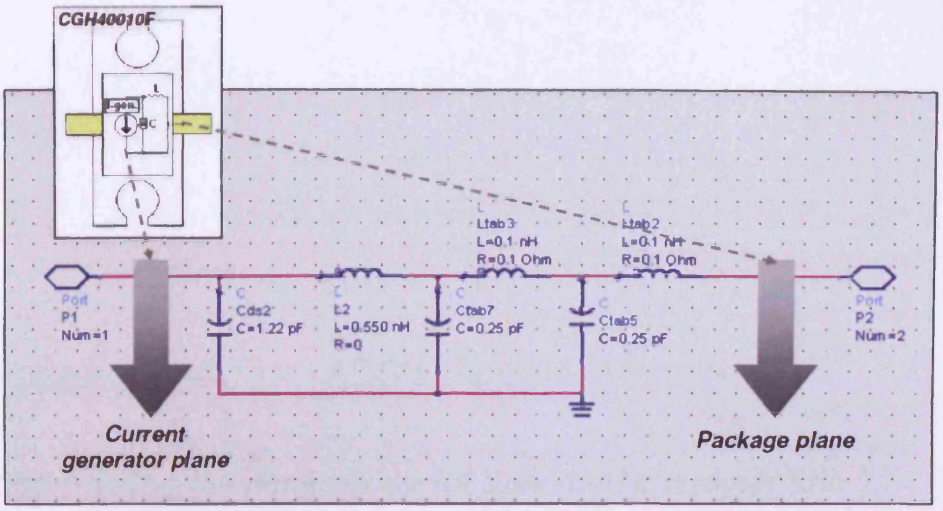


Fig. A4.1: Approximated device parasitic model for CGH40010F.

The simulation provided the load impedances which would become the starting points for the first iteration of the harmonic loading during the load-pull investigation. This intermediate step eliminates the requirement for more extensive sweeps of the second and third harmonic impedances during the load-pull phase of the design process, dramatically speeding up the design procedure as a whole.

Appendix A5. ADS Line Calc. example.

Determining the dimensions for specified characteristic impedances and eiectricai lengths of microstrip transmission lines.

Determining the dimensions for specified characteristic impedances and electrical lengths of microstrip transmission lines

Line Calc. is a tool for microstrip transmission-line-based matching network design. Implementing a user-defined microstrip substrate (denoted as "MSUB" in the 'ID' block in Fig. A5.1), the tool enables the frequency-dependant synthesis or analysis of a physical microstrip line or width, W, and length, L.

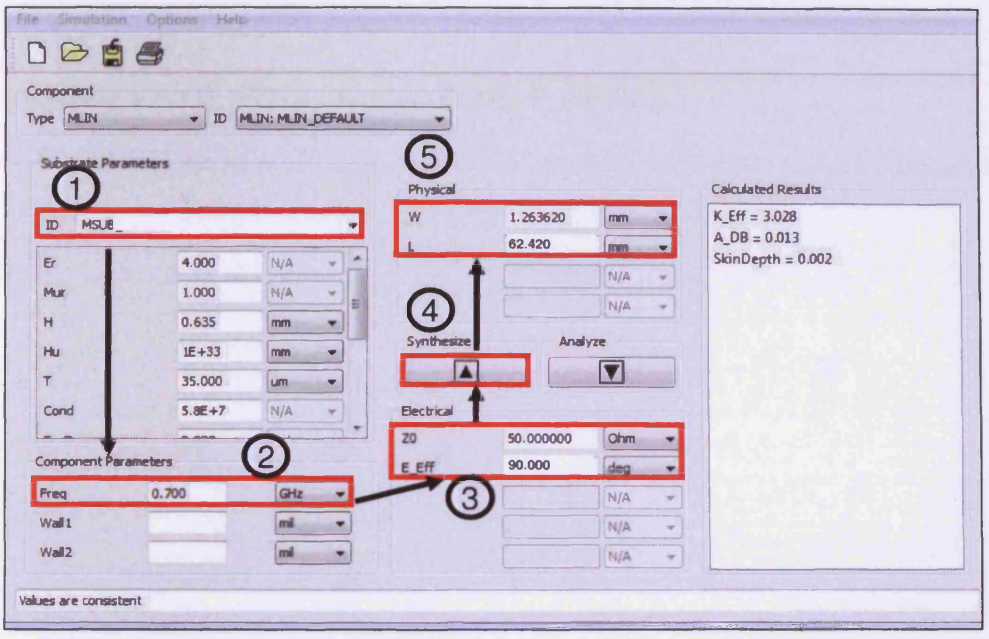


Fig. A5.1. ADS LineCalc. tool macro screenshot, and process of synthesising a quarter-wavelength microstrip transmission line.

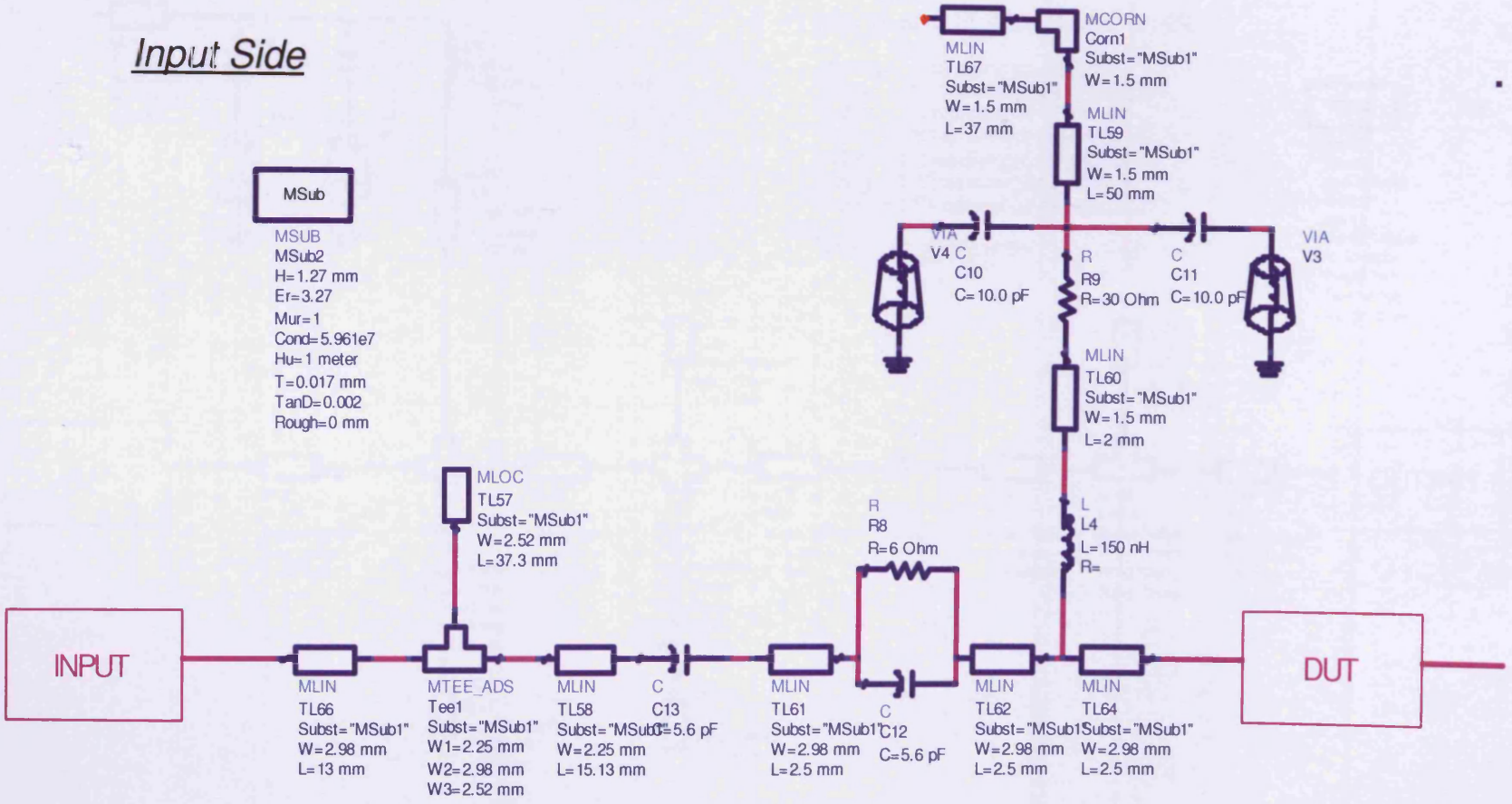
One use of this tool was to determine the required physical length of a microstrip transmission line to synthesise a quarter-wavelength stub as part of the harmonic-matching design of the Class-F^{-1} matching network. In this case under the 'Electrical' block in Fig. A5.1, the characteristic impedance, 'Z0', is entered as "50Ohms", whilst the effective electrical length, 'E_Eff', is entered as "90degs". By running 'Synthesise' the LineCalc. tool calculates the required physical length of microstrip line - on the user-defined substrate - that will facilitate the quarter wavelength required in the matching design.

Appendix A6. Final PA schematics, circuit layouts and components (inverse class-F).

0.9GHz and 2.1GHz inverse class-F RFPAs.

0.9GHz Inverse Class-F RFPA

Input Side



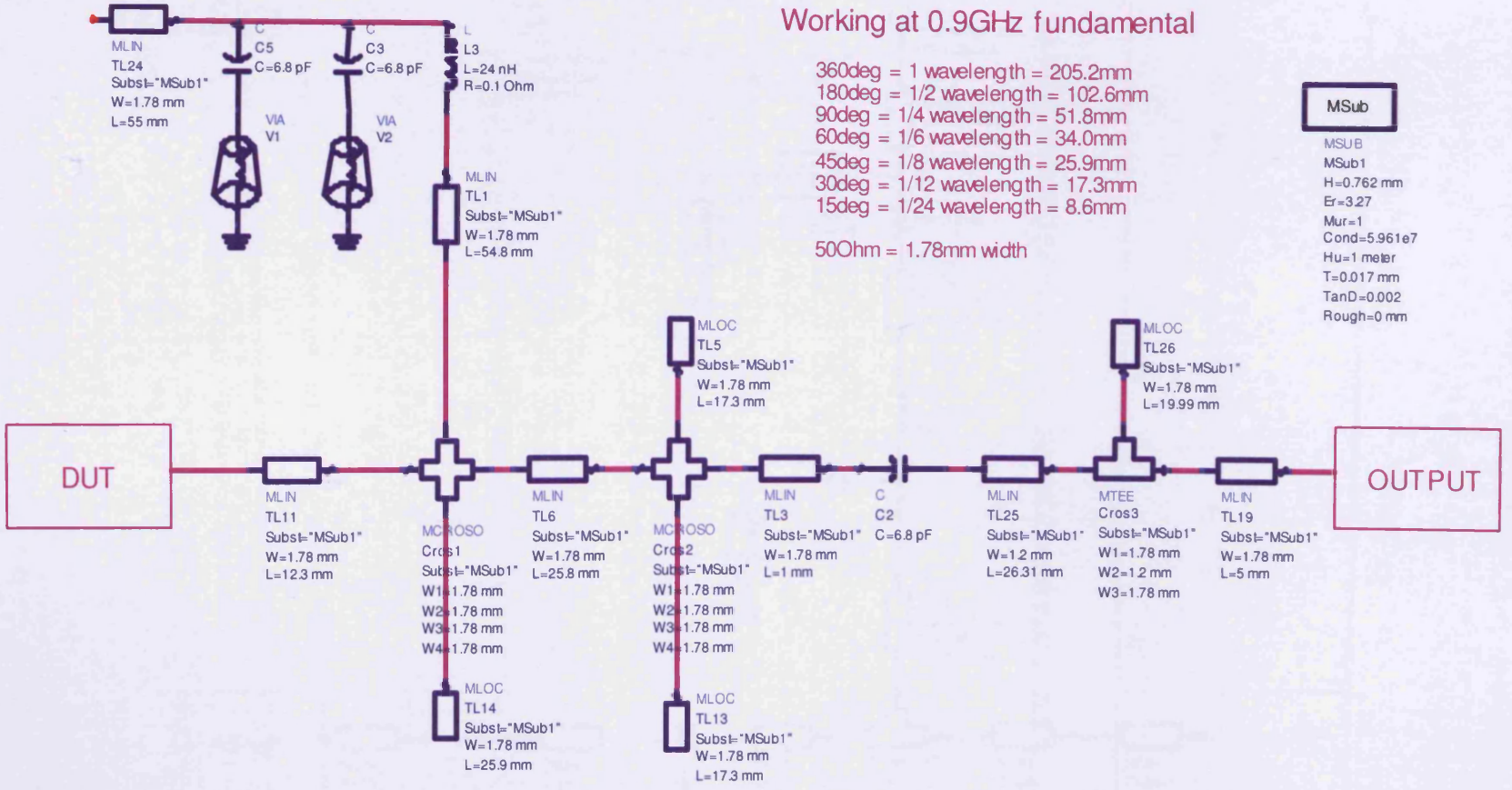
0.9GHz Inverse Class-F RFPA

Output Side

Working at 0.9GHz fundamental

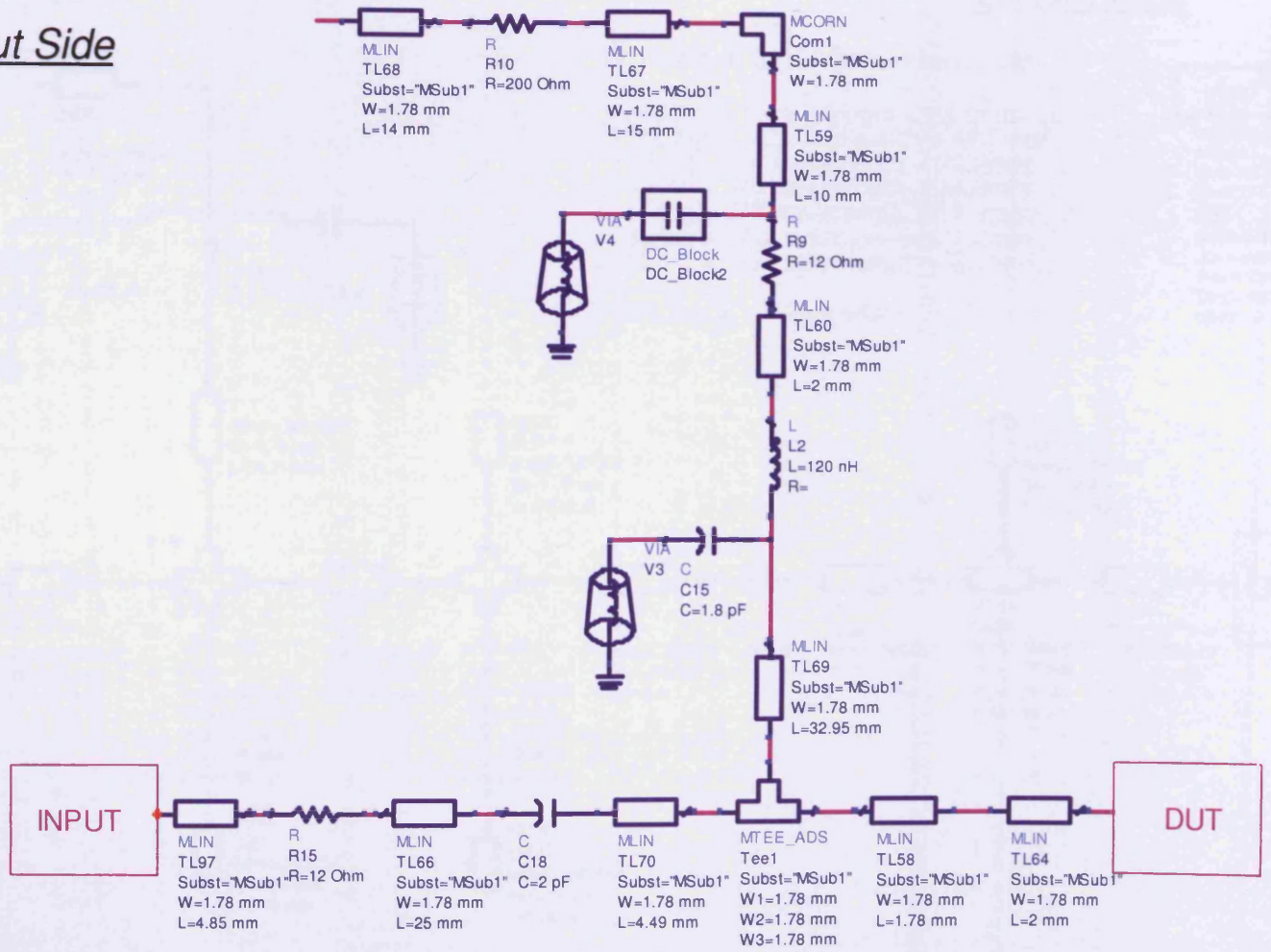
360deg = 1 wavelength = 205.2mm
180deg = 1/2 wavelength = 102.6mm
90deg = 1/4 wavelength = 51.8mm
60deg = 1/6 wavelength = 34.0mm
45deg = 1/8 wavelength = 25.9mm
30deg = 1/12 wavelength = 17.3mm
15deg = 1/24 wavelength = 8.6mm

50Ohm = 1.78mm width



2.1GHz Inverse Class-F RFPA

Input Side



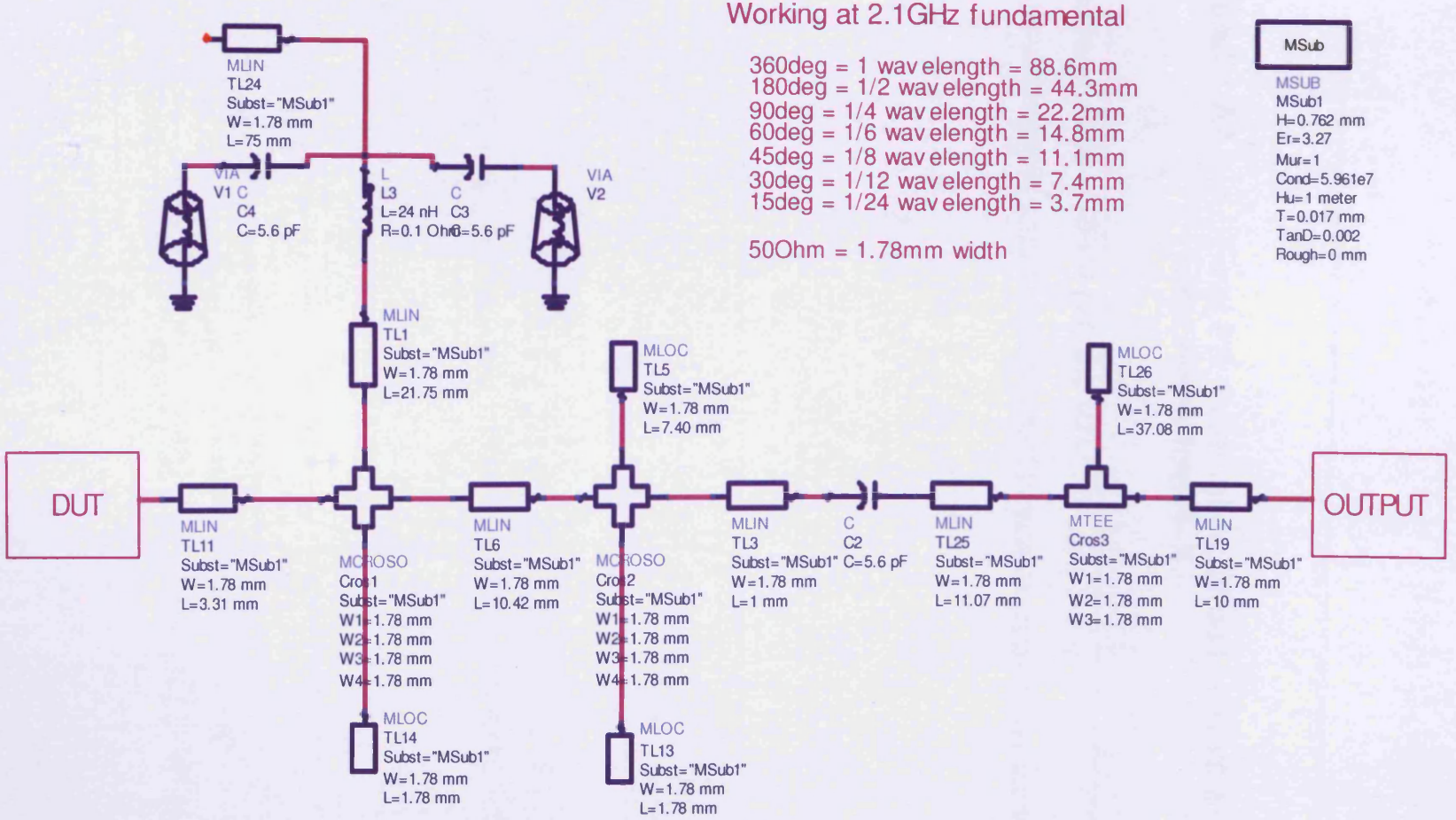
2.1GHz Inverse Class-F RFPA

Output Side

Working at 2.1GHz fundamental

360deg = 1 wavelength = 88.6mm
180deg = 1/2 wavelength = 44.3mm
90deg = 1/4 wavelength = 22.2mm
60deg = 1/6 wavelength = 14.8mm
45deg = 1/8 wavelength = 11.1mm
30deg = 1/12 wavelength = 7.4mm
15deg = 1/24 wavelength = 3.7mm

50Ohm = 1.78mm width

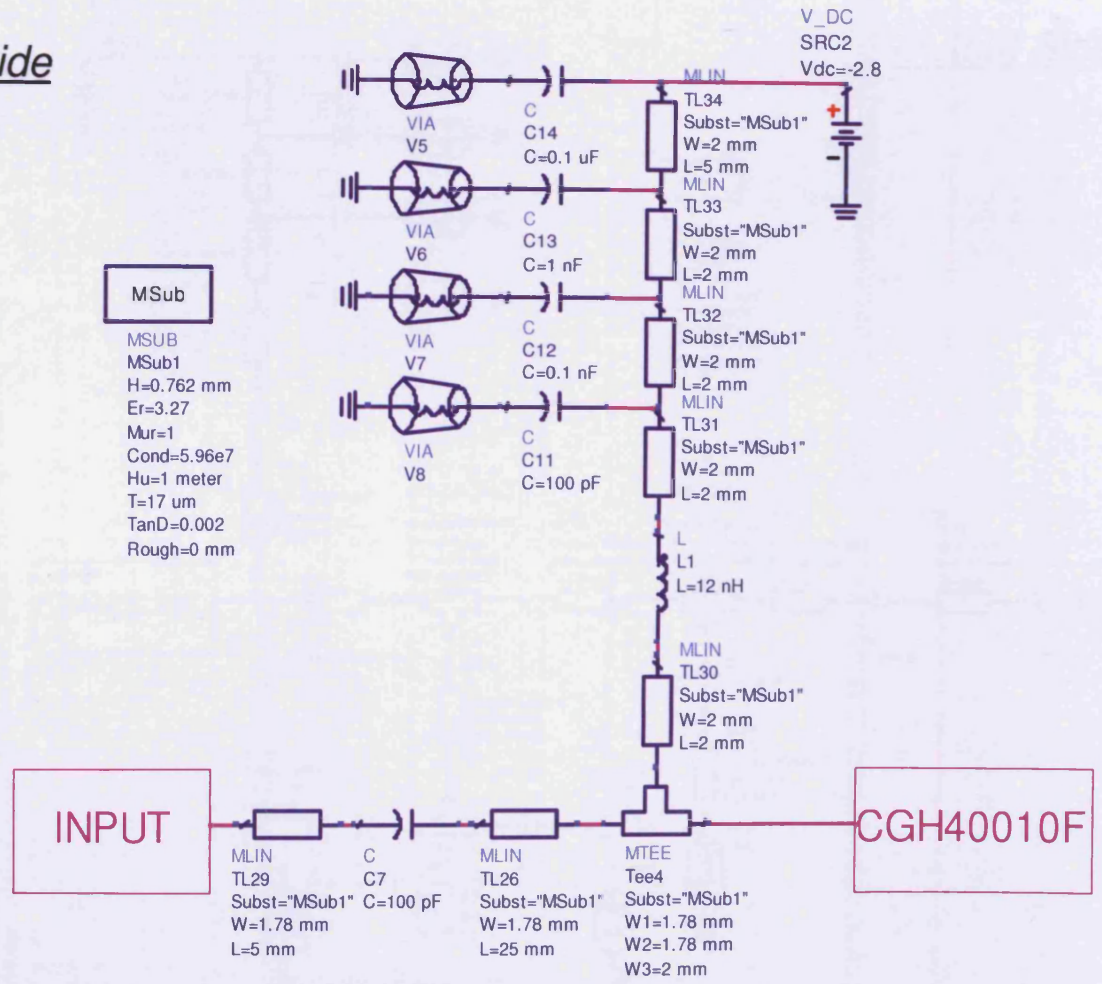


Appendix A7. Final PA schematics, circuit layouts and components (class-J).

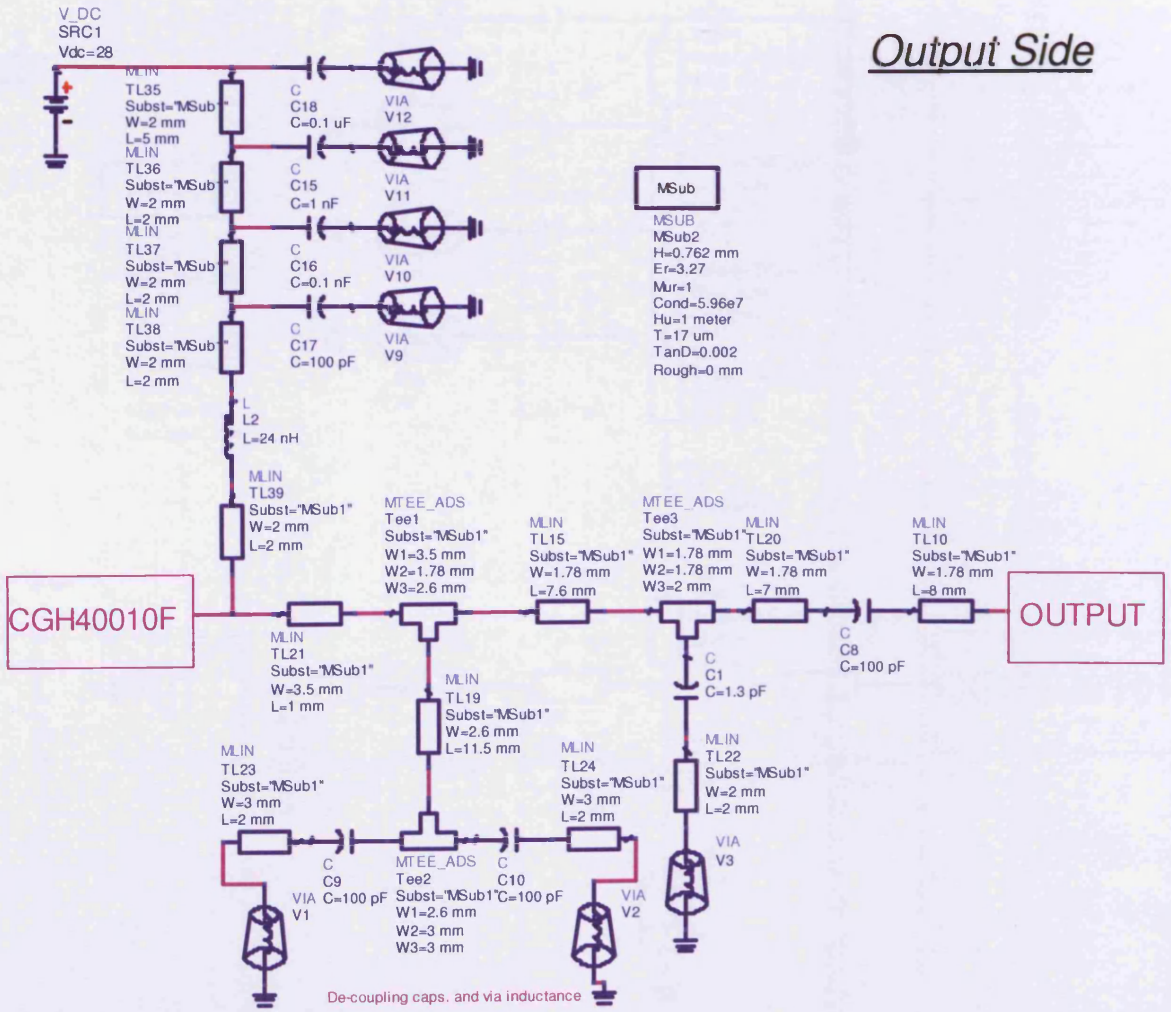
Broadband class-J RFPA (v1 and v2).

Broadband Class-J RFPA (v1)

Input Side

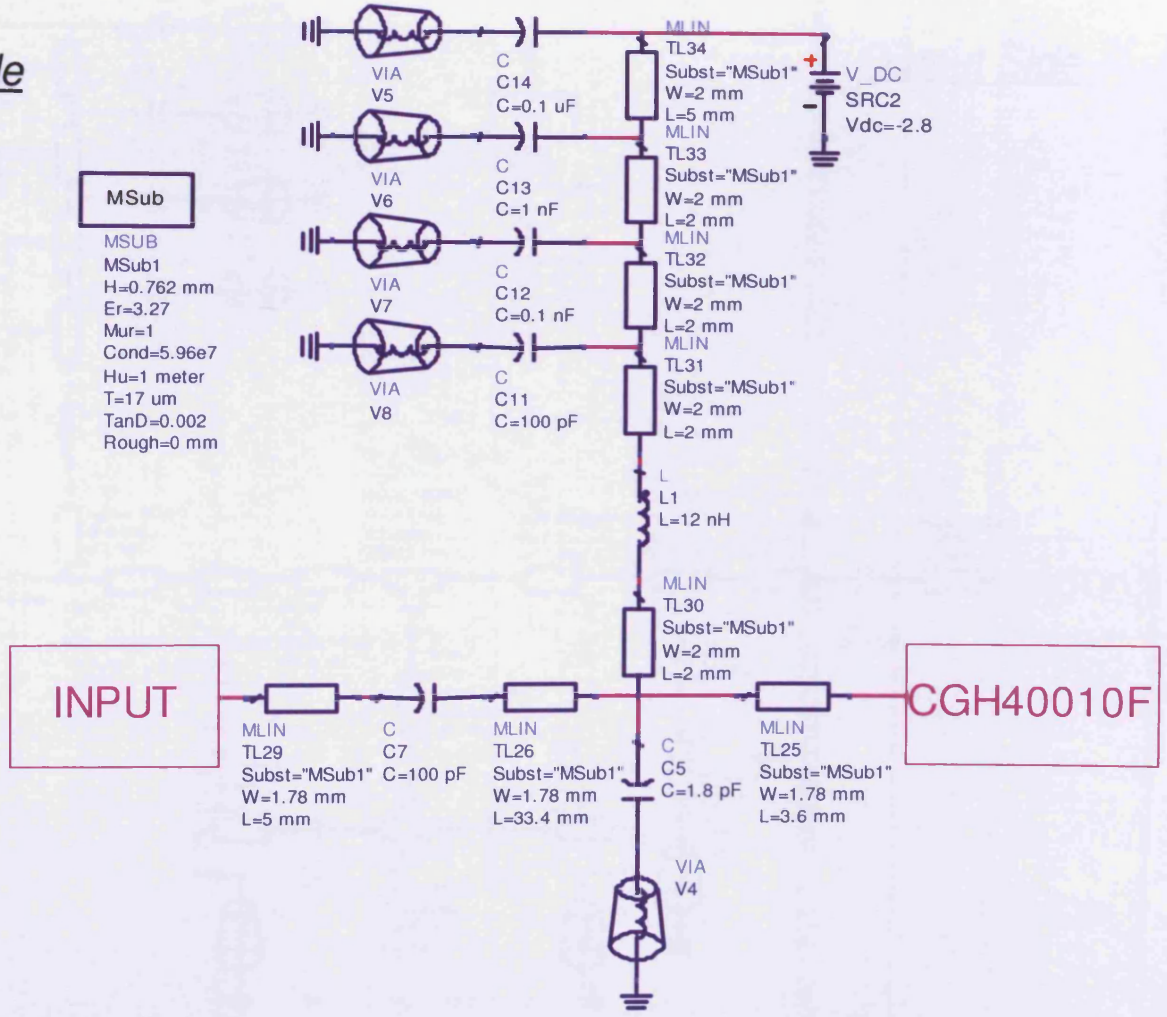


Broadband Class-J RFPA (v1)

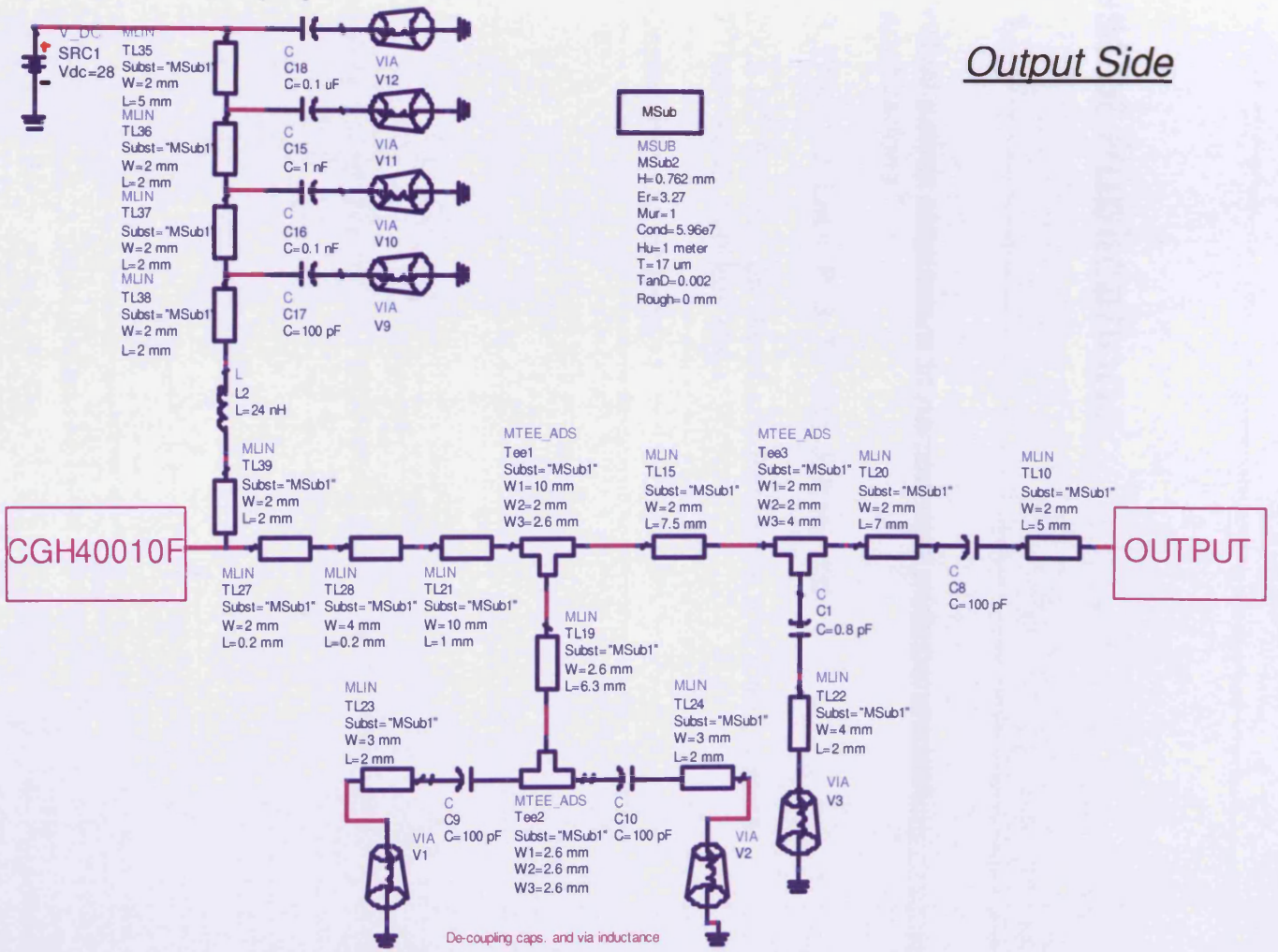


Broadband Class-J RFPA (v2)

Input Side



Broadband Class-J RFPA (v2)



List of Publications

1.

"GaN power transistors in narrow and wide bandwidth applications"

P. Wright, J. Lees, P. J. Tasker, J. Benedikt

2008 IET Seminar on Wideband Receivers and Components
7th May 2008, London, UK,

Conference Digest Page: 1

Narrow and Wide Bandwidth Performance of GaN Power Transistors

Peter Wright, P. J. Tasker and J. Benedikt.

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Abstract — **An active load-pull based investigation was conducted on a 10W gallium nitride (GaN) HEMT at a range of frequencies. It was found that a minimum efficiency of 40% was obtained over a broad bandwidth with a constant output power of 10W with the device in a class-AB mode. In a high efficiency, narrow-band mode very high efficiency performance has been achieved at 0.9GHz delivering 12W fundamental output power at 81% PAE. Benefits in terms of the versatility of GaN have been demonstrated.**

Overview

The wide-band gap GaN HEMT device used in this study allows for large rail voltages to become feasible, hence allowing for power amplifiers in a high efficiency inverse class-F mode can be realised. The high output voltage swing is key to the high power and high efficiencies achievable in this mode of operation, can often be difficult to realise with many current device technologies (e.g. LDMOS, GaAs) due to the limitations induced by device breakdown voltages.

With very high broadband gain also a key characteristic of this device technology, enabling high power and good power added efficiency (PAE) to be obtained across a wide bandwidth in a class-A to AB mode.

In this study a 10W GaN HEMT was used. Waveform measurements have been carried out at fundamental frequencies of 0.9, 2.1, 3.2 and 4.0GHz using the active load-pull waveform measurement system developed at Cardiff University [1]. Fundamental load-pull sweeps have been conducted allowing a trace of the optimum fundamental load for maximum P1dB output power to be made, with the device in a class-AB bias. To obtain the high efficiency inverse class-F mode, active three-harmonic load pull was implemented along with package de-embedding techniques [2].

Wide bandwidth optimisation

Following an analysis of the device stability from S-parameter measurements fundamental active load-pull waveform measurements were performed. A bias point of V_{ds}=28V and I_{dsq}=850mA was selected. Active fundamental load-pull was implemented to obtain an optimum output reflection coefficient for maximised P1dB output power. Waveform measurements were conducted at 0.9. 2.1, 3.2 and 4.0GHz which enabled a trace of the optimum package-plane load impedance, for maximised P1dB output power, to be made on the Smith Chart. In doing this analysis was made into the complexity of broadband matching to obtain the optimised device performance in a possible prototype design. Gain and drain efficiency were also measured across the wide bandwidth with 12.5dB gain measured at 4.0GHz and efficiency, at approximately 1dB gain compression, of more than 40% measured at each frequency, as shown in Table-I.

Freq. GHz	Maximum Values / (Corresponding Load Impedance Ω)				
	P_{out} (P1dB) dBm	$\Gamma_{in,opt}$ Mag./Phase	$\Gamma_{out,opt}$ Mag./Phase	G1dB dB	η_{drain} (P1dB) %
0.9	**40.4** (29.0+j12.6)	**0.94 / -163**	**0.31 / 141**	**26.4**	**47.3**
2.1	**40.1** (17.9+j7.1)	**0.92 / 172**	**0.48 / 160**	**18.8**	**43.2**
3.2	**40.2** (17.5+j4.3)	**0.90 / 154**	**0.49 / 168**	**14.9**	**43.6**
4.0	**40.0** (17.2-j0.7)	**0.87 / 143**	**0.49 / -178**	**12.5**	**40.0**

Table-I: Summary of device performance with frequency

Narrowband harmonic optimisation

A procedure developed for optimising class-F operation for on-wafer devices in [3] has been adapted in the development of an inverse class-F design procedure for optimising efficiency of packaged high power devices. The implemented de-embedding process [2] allows for analysis and engineering of the RF waveforms that exist at the device current-generator plane ($I_{gen.}$-plane) and is essential for enabling RF waveform engineering as it allows for correlation between the measured dynamic I-Vs and the device DCIV plane, which defines the boundaries of the device performance. In reality this ideal performance is compromised by DC offsets, and the ability to generate perfect harmonic terminations required.

A systematic methodology using high-power waveform measurements and device package de-embedding is used to achieve optimised efficiencies in a practical inverse class-F amplifier design. Very high efficiencies obtained in this study are achieved at a high extent of gain compression. However, PAE is also very good due to the high gain of this GaN device. The maximum efficiency achieved was 81.5%, at a gain compression of 4.5dB and 40.9dBm fundamental output power.

Conclusions

Using waveform measurements combined with active load-pull, this study implements two modes of operation in which a GaN HEMT provides narrowband very high efficiency operation, and efficient broadband performance.

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2.

"RF power amplifier design for high efficiency applications"

P. Wright, C. Roff, T. Williams, J. Lees, J. Benedikt, P. J. Tasker

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RF Power Amplifier Design for High Efficiency Applications

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ABSTRACT

In this paper a time domain waveform measurement system with active harmonic load-pull has been used to enhance the design cycle of RF power amplifiers (PAs). Wave-shaping (waveform engineering) techniques using Cardiff University's high power waveform measurement system have yielded optimum device conditions enabling a rapid PA realisation with a first-pass success. The resulting inverse class-F design, based on a 10W GaN HEMT device, is operating at 0.9GHz, and achieving 81.5% drain efficiency in both the load-pull emulated state and also in the directly realised PA. The value of measured waveforms, and the ability to engineer optimum waveforms to a specific amplifier mode, is demonstrated in this study.

Keywords: Active Load-pull, High Efficiency, Power Amplifiers.

1. INTRODUCTION

In mobile military applications, both airborne and ground based, there has been a significant demand for smaller, lighter weight and improved energy efficiency in all areas of communication and EMC systems. In this application space the RF power amplifier in the transmit module often dominates the system energy consumption. As a result, designing higher efficiency RF PAs can yield enormous benefits to system power requirements as well as reduced size of heat dissipation apparatus. Improved efficiency will also increase the lifetime durability of components. Alternatively, the increased efficiency can be used to create headroom for larger RF output powers to be achieved, boosting operating range and capabilities.

In the majority of RF transmitters the PA usually operates below a 50% conversion of DC to RF energy [1]. The system total efficiency will be further reduced by dealing with the DC energy not converted to RF energy, but dissipated as heat. This situation persists despite the large number of known PA architectures [2][3] capable of significantly higher average efficiencies. However, these enhanced PA modes of operation rely on an intricate interaction between the fundamental output power and harmonic loading making their design challenging as no design solutions currently exist that allow for this fully.

There is a direct need for device waveforms in order to establish procedures for designing and analysing complex PA modes. This therefore includes the need for multi-harmonic and broadband measurement capability in order to look at device interaction through the use of dynamic load-lines.

This paper utilises a novel design approach, based on a large-signal measurement system capable of measuring RF current and voltage waveforms above 40GHz, enabling the accurate determination of the nonlinear device performance for the present drive, bias, fundamental and harmonic impedance environment. For straightforward harmonic impedance control the waveform measurement capability is combined with a multi-harmonic active load-pull setup allowing engineering of the current and voltage waveforms at the terminals of the active device. This novel approach to high frequency circuit design can be used to rapidly emulate circuit environments, using the real device directly in the design cycle. The result of this direct design capability is enhanced performance, especially when using cutting edge transistor technologies whose CAD modeling support is often unavailable or less advanced.

Previous work has demonstrated the capability of the measurement system for boosting the efficiency of RF PAs, which has been shown by the authors to achieve efficiencies greater than 80% [4]. To achieve such increases in efficiency, selecting the optimum bias point and load impedance conditions are key in maximising efficient performance. Processes

have been developed to pin-point such conditions using the waveform measurement system at Cardiff University [4][5], however, no designs that are directly based on these measurements have been realised so far.

For the first time, this paper presents results from a realised PA that has directly utilised the time-domain data, captured from high power waveform measurements during design emulation.

1.1 Time Domain Measurement System

The waveform measurement system (shown in Fig. 1) operates using a Tektronics DSA sampling oscilloscope, which allows input and output voltage waveforms to be sampled. A sweeper at the source provides input power at the fundamental frequency whilst a multi-harmonic active load-pull system is used to present the device under test with a range of RF load impedances.

RF probes can be used to allow on-wafer measurements. However the capability of characterising high power packaged devices, combined with accurate parasitic de-embedding, also exists enabling waveform engineering design techniques to be used at high power levels (above 100W). The whole system is computer controlled. This waveform measurement system lends itself well to high efficiency design procedures which have been implemented to facilitate very high efficiency device performance [6].

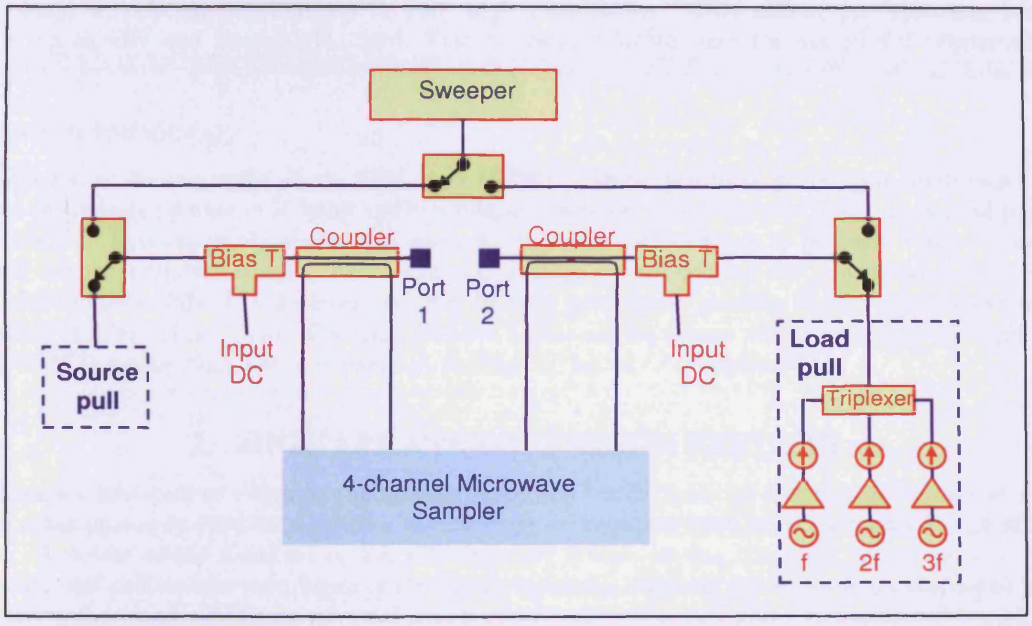

Fig. 1. Time-domain waveform measurement system schematic shown with three-harmonic active load-pull capability.

The system configuration that was used in this study integrated high power waveform measurement capability with fully computer-controlled three-harmonic active load-pull. Fundamental frequency of operation is at 0.9GHz. Load-pull and power sweeps could be conducted, together with bias voltage sweeps in order to obtain optimum three-harmonic-tuned inverse class-F device operation.

1.2 High efficiency operating modes

High efficiency PA modes such as class-F, inverse class-F or Doherty achieve high efficiency performance by wave-shaping the output current and voltage waveforms. All of these modes have attracted attention due to their ability to deliver high RF output power and efficiencies [1]. In the case of the ideal class-F, a half-rectified output current waveform and a square-wave output voltage waveform must be engineered. In the inverse case the output current and voltage wave shapes are opposite. In both cases high power and high efficiency are achieved by minimising overlap between the current and voltage waveforms and thus reducing dissipated energy [5].

Since for the inverse class-F mode the voltage waveform is engineered to be half rectified, the maximum incurred fundamental output voltage ($V_{max.}$) can be obtained from Eq. 1, given a known DC drain bias voltage (V_{DC}) and voltage offset (V_{knee}).

$$V_{max.} = \pi \cdot (V_{DC} - V_{knee}) \qquad (1)$$

Working at a 28V DC drain voltage bias level, and using Eq. 1, it can be quickly seen that large voltage swing maxima can be associated with inverse class-F operation with high power devices. This is key to the high power and high efficiencies achievable in this mode of operation, but can often be difficult to realise with current device technologies such as LDMOS due device breakdown voltage limits. Only with advancements in wide band-gap semiconductor technologies, like the GaN HEMT used in this study, can high efficiency and high power (through high RF voltage swings) become feasible.

The inverse class-F wave shaping is achieved in circuit realisations by presenting appropriate harmonic terminations and selecting an appropriate bias condition. However, in standard design approaches where reliable waveform data is unavailable, it becomes extremely difficult to design with *a priori* knowledge of where the optimum bias point and circuit terminations exist to correctly engineer for high efficiency.

The high-power waveform measurement capability combined with active load-pull makes shaping or engineering of the current and voltage waveforms possible, up to very high frequencies. This allows for optimum bias and circuit terminations to be rapidly and precisely located. This provides reliable data for successful implementations to be designed.

1.3 GaN transistor technology

The design approach is demonstrated for a 10W GaN HEMT. These are next generation wide band-gap transistor devices that can potentially operate in X-band and can tolerate extremely high electric fields compared to previous solid state technologies [7]. This capability allows for increased operating rail voltages to be used which in turn allow much higher peak RF output voltage swings. The increased voltage swing allows for improved power and efficiency performance. Additionally GaN HEMTs have excellent thermal properties, yielding further system advantages in terms of reduced cooling requirements. These characteristics are highly advantageous when designing for high efficiency and therefore GaN HEMTs are an ideal device technology for high efficiency PA applications.

2. HIGH EFFICIENCY DESIGN RESULTS

Using three-harmonic load-pull to isolate optimum load reflection coefficients, in terms of efficiency and output power, combined with other processes used in [4], 80%+ device drain efficiencies have been measured for an emulated inverse class-F design. A power sweep recorded on the measurement system in this condition is shown in Fig.2a, while the captured output current and voltage waveforms at the device-optimum efficient power level are displayed in Fig.2b.

Following device performance optimisation, measurement data such as input and output reflection coefficients, and bias-dependant s-parameter data can then be transported into a CAD environment. Once the data is in an appropriate CAD package, input and output network designs can be modeled to replicate the optimum device impedance environment found following waveform engineering. Fig. 3 shows a PA that has been realised successfully reproducing the same high efficiency and high power performance measured during the waveform engineering design stage.

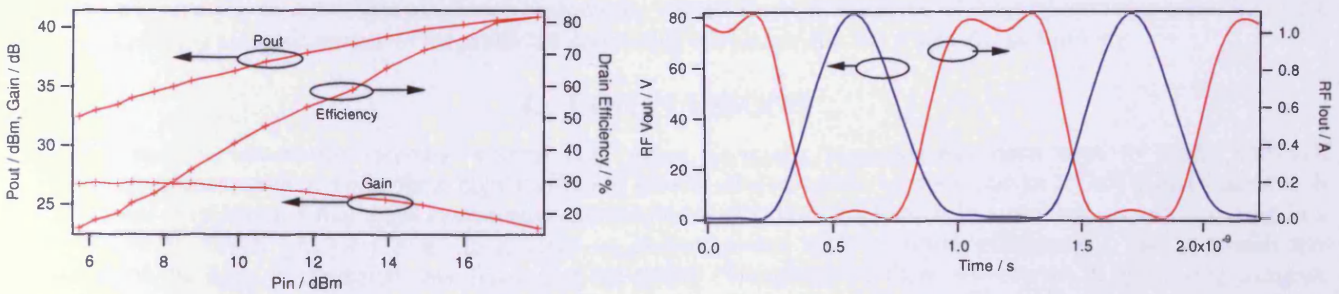

Fig. 2. (a) Inverse class-F power sweep. (b) Measured 81.5% efficient RF current (red) and voltage waveforms at peak efficiency.

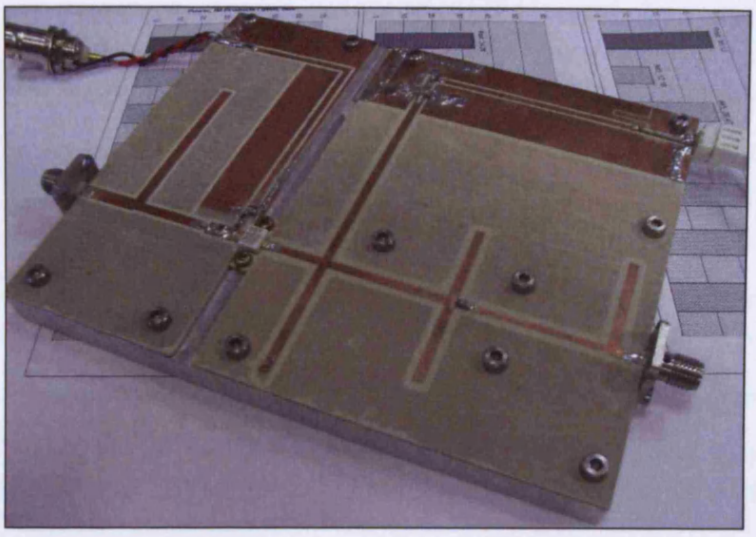

Fig. 3. Realised highly efficient inverse class-F PA from captured waveform data.

Table I summarises the performance measures of the emulated inverse class-F operation following the waveform engineering design process, as well as the measured PA performance following realisation of input and output matching networks directly from captured waveform data. Comparative device performance for both cases can be made by removing the effect of the 0.3dB of loss associated with the realised microstrip output matching network.

Performance Measures	Device Measurements	Realised PA
P1dB Output Power	38.6 dBm	38.1 dBm **(38.4dBm at the dev.)**
P3dB Output Power	40.6 dBm	40.4 dBm **(40.7dBm at the dev.)**
Max. Avail. Gain at P1dB	25.6 dB	24.2 dB **(24.5dB at the dev.)**
Drain Efficiency at P3dB	79.8 %	76.7 % **(82.2% at the dev.)**

Table I. Comparative measures between the emulated inverse class-F PA design and the realised high efficiency PA.

3. DISCUSSION

The design approach has generated high efficiency performance, but not the 100% efficiency predicted for ideal operation. The reduced efficiency is primarily due to three factors, the limited bandwidth of the output matching circuit, losses in the matching circuit and non-idealities of the active device. Device non-idealities bring about DC offsets, which, combined with the lossy nature of real world circuits and ability to generate the ideal harmonic impedance terminations, give rise to maximum efficiency limitations. Given these limitations, efficiency values greater than 80% represent results in close alignment to the predicted achievable efficiency for this transistor technology.

4. CONCLUSIONS

A time domain waveform measurement system with active harmonic load-pull has been used to locate optimum operating conditions, such as those for a highly efficient inverse class-F mode of operation in a GaN HEMT device. It has also been demonstrated that these operating conditions have also been replicated in a realised circuit, resulting in a power amplifier which produces more than 10W of output power at 81% drain efficiency. The approach has demonstrated the value of measured waveforms and the ability of engineering these waveforms in optimising complex PA designs.

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3.

"Highly efficient operation modes in GaN power transistors delivering upwards of 81% efficiency and 12W output power"

P. Wright, A. Sheikh, C. Roff, P. J. Tasker, J. Benedikt

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14^{th}-19^{th} June 2008, Atlanta, GA, USA

Symposium Digest Pages: 1147-1150

Highly Efficient Operation Modes in GaN Power Transistors Delivering Upwards of 81% Efficiency and 12W Output Power

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Abstract — **This paper investigates the development of an inverse class-F design procedure for obtaining very high efficiency performance at high power levels. RF waveform engineering was used to obtain high efficiency inverse class-F waveforms at the device current-generator plane. Drain efficiencies above 81% have been achieved at 0.9 and 2.1GHz for a wide band-gap gallium nitride (GaN) HEMT transistor and 12W fundamental output power. Investigations into improvements in drain efficiency through increases in drain bias voltage have yielded drain efficiencies of up to 84% at 2.1GHz. To the author's knowledge, the efficiencies presented in this study are the highest published, measured efficiencies of a high power GaN HEMT at these frequencies.**

Index Terms — **MODFETs, power amplifiers.**

I. Introduction

High power, high efficiency amplifiers are of great importance in the current climate of energy conservation which demands high efficiency communication systems. A previous inverse class-F design study has shown that higher theoretical efficiencies can be obtained compared to class-F amplifiers when considering 'on-resistance' effects [1]. The large voltage swing associated with inverse class-F operation, that is key to the high power and high efficiencies achievable in this mode of operation, can often be difficult to realise with many current device technologies (e.g. LDMOS, GaAs) due to the limitations induced by device breakdown voltages.

However, with advancements in wide band-gap semiconductor technologies (GaN, SiC), large rail voltages become feasible, hence allowing for power amplifiers with very high efficiency performance to be realised. For the case of the device output power being held constant, an additional advantage arises in that the maximum drain current swing can be reduced to minimise any knee-walkout effect [2-3].

In this study a 10W GaN HEMT was used. Measurements were carried out at two fundamental frequencies of 0.9GHz and 2.1GHz (two of the major communication frequencies) using the active harmonic load-pull waveform measurement system developed at Cardiff University [4]. A procedure developed for optimising class-F operation for on-wafer devices in [5] has been adapted in the development of an inverse class-F design procedure for optimising efficiency of packaged high power devices. The implemented de-embedding process [6] allows for analysis and engineering of the RF waveforms that exist at the device current-generator plane ($I_{gen.}$-plane).

II. Package Parasitic Modeling & De-embedding

Generating an equivalent circuit model for the parasitic effects of the device package allows predictions for the required open and short terminations at the package-plane to be made. The utilised TRL calibration generates a measurement reference-plane at the device package and not, as is the case for on-wafer measurements, close to the device $I_{gen.}$-plane. Thus, the approximated package network provides a means of predicting and analysing operation at the $I_{gen.}$-plane during the design process. This process is essential for enabling RF waveform engineering as it allows for correlation between the measured dynamic I-Vs and the device DCIV plane, which defines the boundaries of the device performance.

The complex loads at the package-plane can be calculated from ideal load values through S-parameter simulations of the parasitic model. Table-I presents the reflection coefficients required, at both the current generator and package reference planes, to establish inverse class-F operation, whilst operating at a drain voltage of 28V at 0.9GHz and also for 2.1GHz.

Frequency	$I_{gen.}$-Plane	Package-Plane 0.9GHz	Package-Plane 2.1GHz
f_0	$0.13 \angle 0°$	$0.26 \angle 82°$	$0.47 \angle 126°$
$2f_0$	$1 \angle 0°$	$1 \angle 99°$	$1 \angle 169°$
$3f_0$	$1 \angle 180°$	$1 \angle -145°$	$1 \angle -72°$

Table-I. Inverse class-F terminations at current generator & package planes for 28V drain voltage at 0.9GHz and 2.1GHz.

III. GaN HEMT in Inverse Class-F Mode

A. Inverse Class-F Theoretical Efficiencies

The ideal inverse class-F output waveforms of half-wave rectified voltage and square current represent a perfectly functioning, 100% efficient inverse class-F amplifier. In reality this ideal performance is compromised by DC offsets, as well as the ability to generate the perfect harmonic terminations required. Assuming terminations up to the fifth harmonic in the current waveform (through hitting the current boundary conditions), and up to the second harmonic in the voltage waveform (through active

harmonic load pull waveform engineering), a bandwidth limitation factor is applicable to the ideal drain efficiency [1,7]. Using the equation for drain efficiency (η_{drain}) in [1], the theoretical efficiency for a three-harmonically controlled inverse class-F amplifier design with offset, V_{knee}, becomes that shown in Eq. 2.

$$\eta_{voltage} \cdot \eta_{current} = 1.000 \times 0.854 = 0.854 \quad (1)$$

$$\eta_{drain} = 100 \times \frac{V_{DC} - V_{knee}}{V_{DC}} \times 0.854 \quad (2)$$

B. Initial gate bias sweeps at 0.9GHz

Processes implemented in [5] for obtaining highly efficient class-F designs were adapted in order to begin developing a procedure for obtaining an optimised inverse class-F design. This included a sweep of gate bias voltage to identify an optimum bias point which was conducted with the necessary fundamental and harmonic terminations, as stated in Table-I, in place. The drive level during the sweep was such that output compression was approximately -3dB.

Once package-plane measurements were obtained the equivalent circuit model for the output parasitics and device package was utilised to de-embed to, and reveal, the $I_{gen.}$-plane current and voltage waveforms [6]. It was then possible to select a gate voltage which would allow a squared output current and half-rectified output voltage waveform to be obtained. To achieve this, both the ratio of the second harmonic voltage to the fundamental voltage, and the ratio of the third harmonic current to the fundamental current, was selected in accordance with inverse class-F theory. Due to the limited number of harmonic terminations employed, the optimum harmonic current and voltage ratios required were less than those for the ideal design; approximately 0.18 and 0.29 respectively.

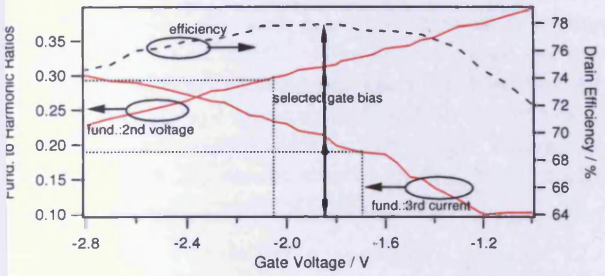

Fig. 1. Gate sweep at 28V drain voltage bias condition at 0.9GHz.

Tradeoffs between both of these ratios were necessary as the required voltage and current ratios did not occur at the same point in the gate voltage sweep. Therefore, at 0.9GHz, the final gate bias of -1.85V was selected at the efficiency peak, as shown in Fig. 1.

C. Optimisation of load impedances and results at 0.9GHz

Following the selection of the gate bias, the predicted load impedances in Table-I were optimised. In a first step the fundamental load impedance at the I_{gen}-plane was swept between 60Ω and 70Ω. Once the optimum for the fundamental impedance was determined the phase of the second harmonic was swept by ±10° of the figure in Table-I to compensate for any small errors in the approximated package model. The same sweep was then applied to the third harmonic phase. The resulting optimised impedance values at the I_{gen}-plane are given in Table-II.

Frequency	$I_{gen.}$-Plane	Package-Plane
f_0	0.14 ∠ 0°	0.27 ∠ 86°
$2f_0$	1 ∠ -6°	1 ∠ 91°
$3f_0$	1 ∠ -174°	1∠ -142°

Table-II. Optimum terminations for Vds=28V at 0.9GHz.

A power sweep was conducted with the optimised gate bias, fundamental load and harmonic impedances. The results at 0.9GHz are shown in Fig. 2. The maximum efficiency achieved was 81.5%, at a gain compression of 4.5dB and 40.9dBm fundamental output power.

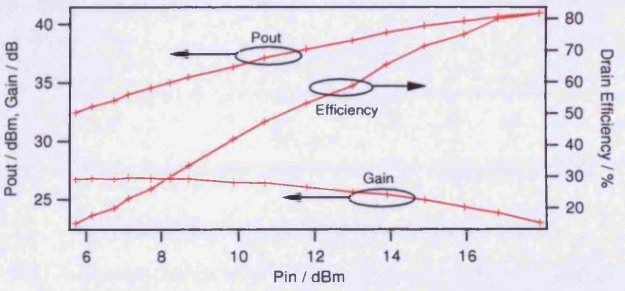

Fig. 2. Power sweep at 28V drain voltage bias condition at 0.9GHz.

All waveforms measured were imported into Agilent's ADS simulation environment and, were de-embedded to the current generator plane using the previously discussed package parasitic model. Fig. 3 shows the de-embedded output current and voltage waveforms obtained at the drive level delivering maximum efficiency of 81.5%. Fig. 4 shows the comparison between the package-plane and de-embedded $I_{gen.}$-plane RF load lines.

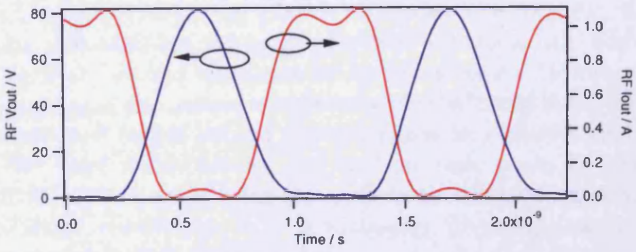

Fig. 3. Measured 81.5% efficient RF waveforms, de-embedded to the $I_{gen.}$-plane at Vds=28V and 0.9GHz.

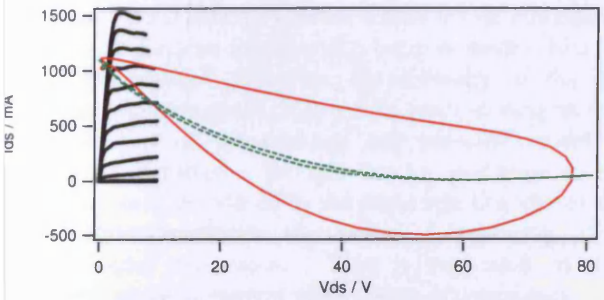

Fig. 4. Measured package-plane RF load-line (solid) and de-mbedded RF load-line (dotted) at Vds=28V, 81.5% efficiency.

In conclusion, the waveforms in Figs. 3 and 4 not only ıow that high efficiency inverse class-F operation has been :hieved at 0.9GHz, but also that the package model has :en verified as accurate at least up to 2.7GHz through de-mbedding of the waveforms to the $I_{gen.}$-plane.

IV. Design Towards High Efficiency at 2.1GHz

. Inverse class-F scaled to 2.1GHz at 28V

With the successful waveform optimisation for inverse ass-F at 0.9GHz completed, performance scalability to ıgher frequencies was investigated. For this purpose the ıte bias sweep was repeated at 2.1GHz, this time :livering an optimum of V_{gs}=-2.5V.

However, by applying the predicted load impedances in able-I for 2.1GHz, and performing a power sweep, it was ınd that a disappointing 69.3% drain efficiency was ɔtained with 40.9dBm fundamental output power at 28V ain voltage. To gain a further optimised performance, the ıases of the harmonic loads were now swept across a ider range of angle than the previous ±10°, with the aim of ɔtaining an optimum efficient mode of operation. ɔllowing the optimisation of the harmonic impedances a gh density sweep of the fundamental load was conducted sulting in an optimised $I_{gen.}$-plane load with a more ıbstantial complex offset. The final optimised package-ane and de-embedded harmonic loads are listed in Table-I for a drain voltage bias condition of 28V. Utilising these ılues a power sweep with a 28V drain voltage was ɔnducted, with the results display in Fig. 5 indicating a aximum drain efficiency of 82.3%.

Inverse class-F scaled up to V_{ds} of 40V

The high voltage breakdown nature of the wide band-gap aN device technology proves ideal in securing the very gh voltage swings required for high power inverse class-F ɔeration. This combined with the very low knee voltage, herent with this GaN HEMT device technology, offers the ɔssibility of reaching very high levels of drain efficiency ıilst operating at these high power levels.

With the design procedure scaled to 2.1GHz an vestigation was made on its scalability towards higher drain bias voltages. For this purpose the drain bias voltage was increased above 28V to 35 and 40V, respectively.

The same GaN HEMT device was used with output power and compression kept approximately constant for each of the DC drain voltage levels. As DC drain voltage was increased, an appropriate reduction of the output current swing as a result of the increased voltage swing was therefore required. During the scaling of the drain voltage the same gate bias of V_{gs}=-2.5V and harmonic load impedances, according to Table-III, were maintained.

The obtained results at a 35V drain voltage bias condition saw the drain efficiency improve up to 82.8% whilst with a 40V bias condition 84.0% drain efficiency was measured.

Frequency	$I_{gen.}$-Plane	Package-Plane
f_0	0.14 ∠ 39°	0.52 ∠ 129°
$2f_0$	1 ∠ -75°	1 ∠ 129°
$3f_0$	1 ∠ -170°	1∠ -69°

Table-III. Optimum terminations for Vds=28V at 2.1GHz.

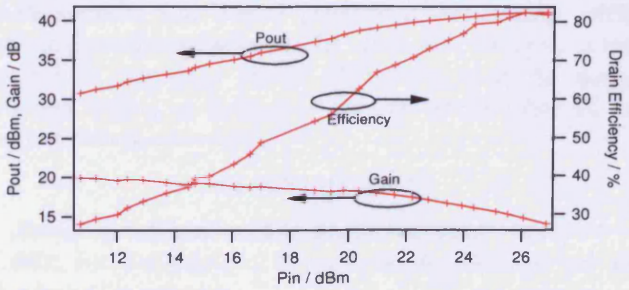

Fig. 5. Power sweep at 28V drain voltage bias condition at 2.1GHz

V. Waveforms & Performance Analysis

Fig. 6 shows the de-embedded output current and voltage waveforms present at the I_{gen}-plane at maximum drain efficiency of 82.3% at V_{ds}=28V. As can be seen, with decreasing current swing the de-embedded current and voltage waveforms were beginning to extend beyond the defined DCIV boundaries of the device. This was due to the inaccuracies in the package model becoming more apparent at the higher harmonic operating frequencies, as well as the increased effects from the weakly non-linear output capacitance. Nevertheless, these de-embedded waveforms are still effectively indicating the performance of the device at the $I_{gen.}$-plane. As can be seen from Fig. 6, the de-embedded voltage waveform maintains the half-rectified sinusoid indicative of inverse class-F. However, squaring of the current waveform is also indicated in the de-embedded output current waveform, but to a lesser extent. The same measurements and analysis were made for the 35V and 40V drain voltage conditions showing almost ideal voltage waveforms, but continuously diverging current waveforms away from the ideal.

This can be explained by errors within the de-embedding package and parasitic model which become more critical at higher frequencies. However, the accuracy of the de-embedded waveforms at 0.9GHz does seem to suggest that the linear part of the package and parasitic model is accurate. It is therefore thought that the distortion in the output current is introduced by the slight non-linearity of the device output capacitance, C_{ds}, having an increasing effect towards higher freqencies. This is supported by the observed increase in current distortion as V_{ds} increases.

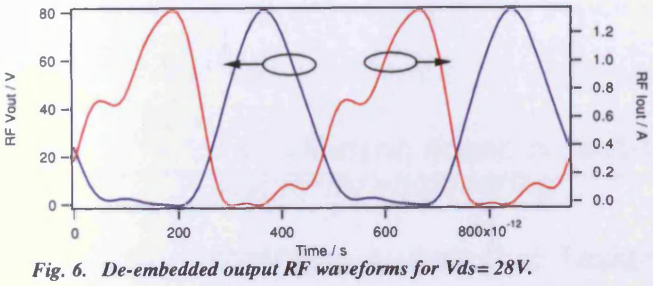

Fig. 6. De-embedded output RF waveforms for Vds= 28V.

It is also interesting to note that the maximum incurred voltages at the $I_{gen.}$-plane did scale very well with increasing rail voltages. The maximum incurred output voltages ($V_{max.}$) for the 28V, 35V and 40V drain bias conditions are 82V, 102V and 121V respectively, and very closely replicate the theoretical values for inverse class-F obtained from Eq. 3 below.

$$V_{max.} = \pi \cdot (V_{DC} - V_{knee}) \qquad (3)$$

Fig. 7 shows a comparison between the measured and theoretical relationship between the maximum measured RF output voltage and the DC drain voltage bias condition. The measured relationship shows a good conformance to that calculated using Eq. 3. The voltage offset, of approximately 3V observable at each drain bias voltage, can be accounted for by the smaller fundamental-to-second-harmonic voltage ratio being implemented due to trade-offs in the gate bias voltage chosen. Conclusively, the utilised GaN technologies did not indicate any onset of RF breakdown up to 121V.

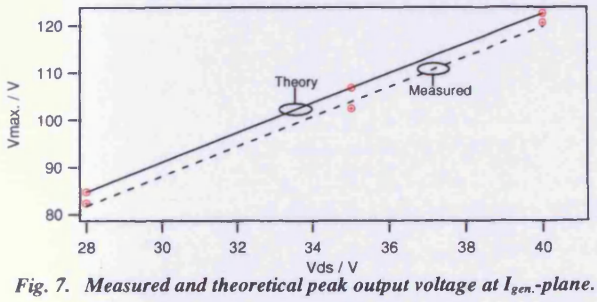

Fig. 7. Measured and theoretical peak output voltage at $I_{gen.}$-plane.

Furthermore, the very high efficiencies obtained in this study are achieved at a high extent of gain compression of the device (between 4 to 5dB compression). It is important to stress, that even under such high state of compression, this device continues to operate very efficiently and at gain levels of 14dB and above. Consequently, PAE is lower only by 0.5 to 3.5% compared to drain efficiency across all optimised efficiency conditions detailed in this research. The high gain of this GaN device lends itself very well to this high efficiency application.

VI. Conclusion & Discussion

The procedures described in this paper, to obtain very high efficiency performance from a GaN HEMT, show a systematic methodology in which maximum achievable practical efficiencies of an inverse class-F amplifier topology are obtained and analysed at 0.9GHz. At 2.1GHz the uncontrolled measurement system harmonic impedances conspire to prevent inverse class-F operation from being achieved, and instead another high efficiency mode is obtained. This performance was shown and verified through the combination of high-power waveform measurements and device package de-embedding, whilst also analysing how increased DC drain bias voltage can lead to further improved record efficiencies, and the output voltage scaling as defined in the half rectification of the output voltage waveform.

Acknowledgement

Research reported in this paper has been supported by CREE, Inc. for supply of devices, and by Milmega Ltd. for financing the research.

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4.

"An efficient, linear, broadband class-J-mode PA realised using waveform engineering"

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An Efficient, Linear, Broadband Class-J-Mode PA Realised Using RF Waveform Engineering

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Abstract — **Results from a fully implemented class-J RFPA (RF power amplifier) are presented for the first time, which demonstrate this mode's high efficiency potential across a substantial bandwidth. Using a commercially available 10W GaN (gallium nitride) HEMT device, and the high power waveform measurement and active load-pull capability at Cardiff University, class-J operation has demonstrated drain efficiencies between 60-70% across a 1.35-2.25GHz (50%) bandwidth whilst delivering 10 Watts of power at the 2dB compression point. Realisation of the design has confirmed that the optimum harmonic load impedances of the class-J amplifier are more practically realisable than conventional Class-AB modes, with better compromise between power and efficiency tradeoffs over a substantial RF bandwidth.**

Index Terms — **Bandwidth, class-J, high efficiency, power amplifiers.**

I. Introduction

Until recently, PA design for wireless communication has been focused on specified RF bandwidths of 5% or lower, due mainly to the very tight spectrum allocations. Future systems, including WiMax, 4G and beyond, will likely require larger bandwidths, not just due to wider spectral allocations, but the base bandwidth of the signals themselves which may well extend up to, and ultimately exceed, 100MHz.

To date, other RFPA applications, such as radar and ECM have not profited from advances in power and efficiency due to their much wider RF bandwidth requirements. Reported results on very high efficiency PAs, typically operating above 75% efficiency, tend to rely heavily upon precise multi-harmonic impedance terminations at the DUT (device-under-test) as well as very high levels of device gain-compression. Both of these factors lead to narrowband frequency performance limitations (less than 10%) and non-linear operation respectively. A newly presented mode of operation - class-J [1] - has shown the theoretical potential of obtaining linear RFPAs that have the same efficiency and linearity as conventional Class-AB designs but do not require a band-limiting harmonic short.

The high power measurement and characterisation capability at Cardiff University [2] has, for the first time, been utilised in the development of a broadband PA design methodology. Coupled with the theoretical backing for class-J in [1], significant investigations into the realisable performance of the class-J mode of PA are presented for the first time using a GaN HEMT power transistor. Specifically, analysis into the achievable high bandwidth-efficiency of a class-J PA from a waveform engineering-based process is presented. Waveform and systematic load-pull measurement data has been used in the development stage of the design procedure, whilst also being used to analyse the extent to which optimum broadband high-efficiency operation has been achieved in this mode.

Measurements have been performed across a bandwidth of 1.3 to 2.3GHz. Device output parasitic de-embedding has been applied to the waveforms captured at the calibrated measurement plane of the device package in order to confirm class-J behaviour from the output voltage and current waveforms at the device plane [3].

Design and realisation of PA matching networks has yielded a broadband amplifier operating at high efficiency. Finally, linearity has been confirmed through ACP (adjacent channel power) measurements.

II. Class-J Mode of Operation

A. Class-J harmonic load terminations

Class-J has been described by Cripps [1], who acknowledges some earlier work by Raab [4]. Class-J is defined as a mode where the voltage has harmonic components which make it tend asymptotically towards a half-wave rectified sine-wave, which in practice can be usefully approximated by a suitably phased second harmonic component. The key difference between Class-J and most other high efficiency modes is the requirement for a reactive component at the fundamental. This is necessary to maintain a second harmonic voltage phasing that is beneficial to efficiency, whilst maintaining a physically realisable impedance termination at the second harmonic. In this way, a higher fundamental component can significantly outweigh the loss in power implied by the reactive load, a counter-intuitive result that has been discussed in detail elsewhere [1].

A Class-J design thus displays approximate half-wave rectified sinusoidal output current and voltage waveforms, with a phase overlap between the two (Fig. 1). This mode of operation lends itself very well to the process of waveform engineering, as described previously by some current authors [2]. Independent bias control and active multi-harmonic load-

pull are used to engineer the shape of the current and voltage waveforms respectively.

The class-J output voltage waveform - assuming two-harmonics - is outlined in Table I [1]. From this the fundamental and second-harmonic impedances (1) and (2) respectively can be found, defining the matching criteria.

In order to optimise efficiency, the GaN device requires some compromises in setting the design values for the fundamental ('load-line') resistance value, due to the effect of the DC 'knee'-voltage offset [5].

TABLE I
IDEAL CLASS-J LOAD TERMINATIONS, ASSUMING TWO HARMONICS

Harmonic	Normalised voltage component
1	$1.41 \angle 45°$
2	$0.50 \angle -90°$

$$Z_{f_0} = R_L + j \cdot R_L \qquad (1)$$

$$Z_{2f_0} = 0 - j \cdot \frac{3\pi}{8} \cdot R_L \qquad (2)$$

This required loading can be realised with the inclusion of the device output capacitance within a PA matching network design, which also has the tendency to provide a short to the higher harmonics. Figs. 1 and 2 illustrate measured class-J waveforms with these harmonic terminations, and with the third harmonic also optimised for efficiency (specified in Table II). The bias point implemented here was a deep A/B.

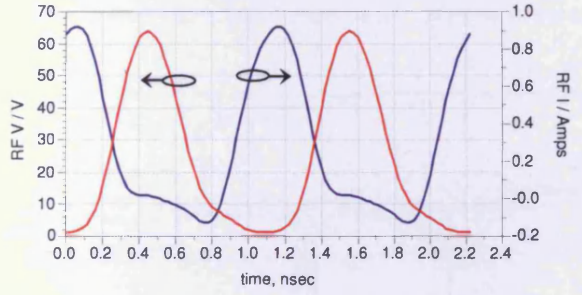

Fig.1. Measured class-J waveforms on a 10W GaN HEMT.

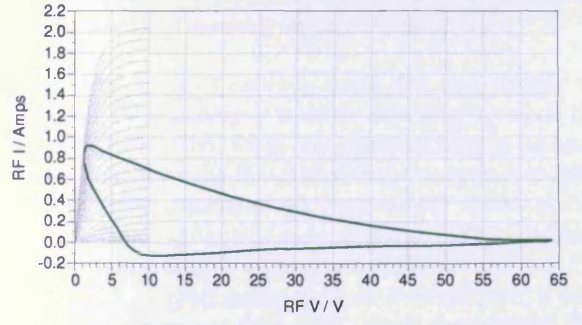

Fig. 2. Measured class-J dynamic load-line on a 10W GaN HEMT, overlaid with device DC-IVs.

TABLE II
CLASS-J $I_{GEN.}$ (CURRENT GENERATOR)-PLANE LOAD TERMINATIONS

Frequency	$I_{gen.}$-Plane Load Impedance
f_0	43.8 + j45.2 Ω
$2f_0$	1.6 – j52.0 Ω
$3f_0$	2.4 – j49.7 Ω

B. Waveform engineering very high efficiency class-J operation in a GaN HEMT

By optimising the fundamental and harmonic load impedances up to $3f_0$, applying the class-J reactive components through active load-pull, very high efficiency device operation has been measured at a fundamental frequency of 1.8GHz. The power sweep for this optimum emulated case is shown in Fig. 3. This shows the output performance of the DUT in a class-J loading configuration, operating with a bias point in class-C. A peak drain efficiency of 83% has been measured in this state with just below 10W device output power and approximately 3.5dB of gain compression. However when looking at the device output performance 6dB backed off from this point, the measured drain efficiency is still above 60%. Device output power is slightly less than may be observed in an optimised class-F/class-F^{-1} PA mode within the same boundary conditions [6].

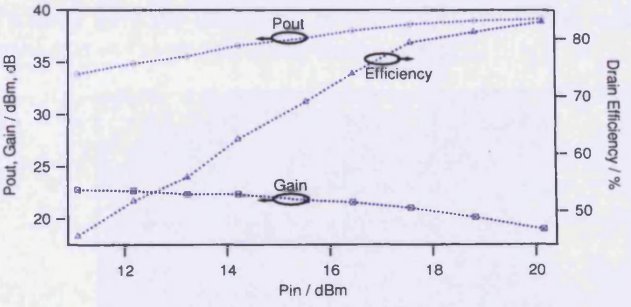

Fig. 3. Power sweep showing very high efficiency class-J operation at 1.8GHz.

Following this initial performance characterisation of the class-J mode, a 10W broadband PA design was initiated, with a goal of above 60% efficiency over a 50% bandwidth.

II. INVESTIGATING A BROADBAND CLASS-J PA DESIGN

In order to begin the design stage of the class-J PA the GaN transistor to be used in the design was put under test and harmonically load-pulled using the three-harmonic active load-pull set-up at Cardiff University [2]. This was carried out at several frequencies between 1.3 and 2.3GHz. The device was in the same state of gain compression (approximately P2dB) in each case. Working with device measurement data at the calibrated package-plane (i.e. without output parasitic de-embedding applied) the resulting load-pull sweep data was

used to map out the drain efficiency as a function of fundamental load impedance on the Smith chart.

Fig. 4 indicates the 70% drain efficiency contour obtained from each fundamental load sweep, indicating the movement of the load at the device package-plane as a function of frequency. The second and third harmonic impedances were set at the same respective load impedances for each fundamental load-pull sweep; $I_{gen.}$-plane $2f_0 = 0.95 \angle -90°$, $3f_0 = 0.95 \angle -170°$ (as indicated in Fig. 4).

A corresponding output power contour plot was extracted following the load-pull sweep which provided an 'area' of load impedances for which to aim a matching circuit design to provide a compromised class-J PA output power and drain efficiency.

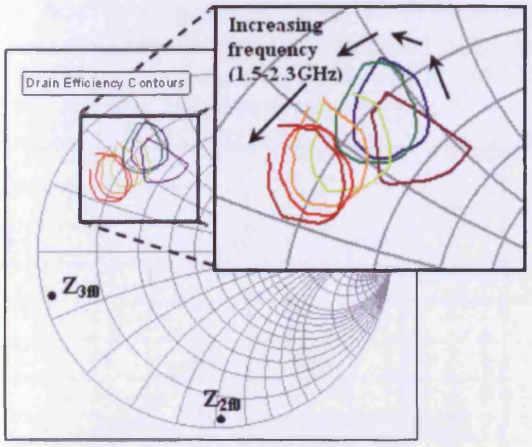

Fig. 4. Measured load-pull data for GaN HEMT indicating load impedance contour for 70% P2dB drain efficiency between 1.5-2.3GHz.

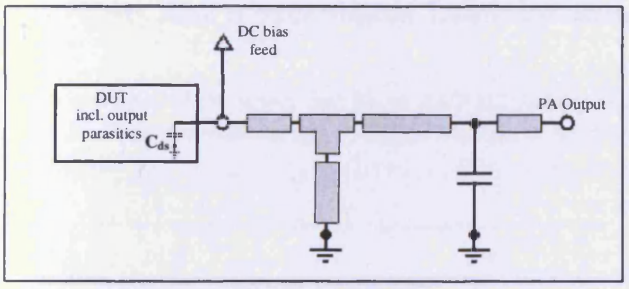

Fig. 5. Realised load matching network schematic [1].

The original target frequency band for this design was 1.5-2.5GHz. In designing a suitable matching network over this extended bandwidth, some compromises have to be made. The initial strategy on the first design iteration (presented here) was to give higher priority to the fundamental impedance and allow the second harmonic more latitude. This particular device has a low output capacitance (approximately 1.5pF) which at 2GHz is itself quite close to the optimum reactive termination at the second harmonic. Thus the network itself mainly synthesises the required fundamental load over the extended bandwidth, but through a shunt inductive stub increases the effective second harmonic capacitive reactance for lower frequencies. The output matching network is shown schematically in Fig. 5. For purposes of comparison between the load-pull data and the realised PA performance, the same 50-Ohm input impedance environment was applied for the PA input.

IV. Realised Class-J PA Performance Results

A. Efficiency and output power vs. frequency

The realised class-J amplifier is shown in Fig. 6. Power sweeps over 12dB were carried out on the PA across a frequency range of 1.2 to 2.6GHz whilst also calculating the drain efficiency of the device within the PA across this bandwidth. Results of this sweep are shown in Fig. 7. The efficiency performance at the P2dB compression state is displayed; this is customarily used as an 'end-point' for useable high-end efficiency performance in high PAR (peak-to-average ratio) signal applications.

As seen in Fig. 7, the measured P2dB drain efficiency for the realised class-J amplifier is between 60-70% between 1.35GHz and 2.25GHz; a 50% bandwidth about a centre frequency of 1.8GHz. Within this bandwidth output power from the amplifier is between 9 and 11.5Watts.

A comparison between the realised PA results and simulated efficiency from the non-linear device model, set in the same impedance environment, is also shown in Fig. 7.

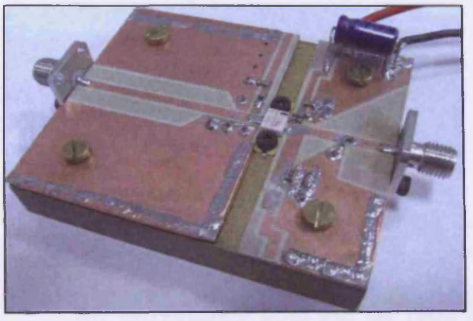

Fig. 6. Realised class-J 10W amplifier – output matched only.

B. PA Linearity and ACPR characteristics

Very high efficiency PAs can be prone to very non-linear characteristics which present users with a difficult, if not impossible, task of pre-distorting the PAs to meet communication system standards. ACPR, without any form of pre-distortion, was measured across a range of drive powers for the realised class-J PA, focusing on the centre frequency of 1.8GHz. Using a WCDMA signal of 5MHz channel bandwidth and 8.51dB PAR, a spectrum of the output signal from the PA operating, with a drive sufficient to cause 2dB peak compression, is shown in Fig. 8. Average efficiency and ACPR is displayed in Fig. 9 with increasing drive power to the PA. ACPR of –32dBc, whilst operating at 39% average

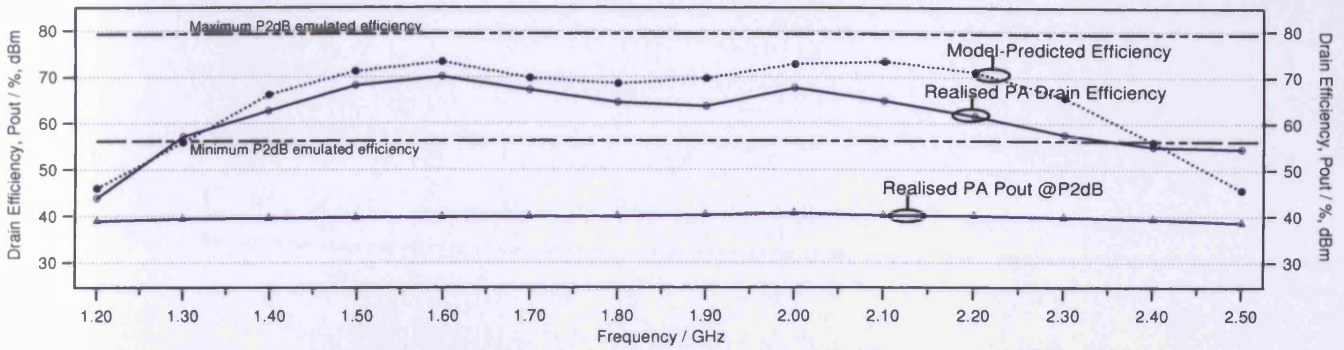

Fig.7. P2dB drain efficiency, P_{out} performance, and device model-predicted efficiency for the realised class-J PA across a bandwidth of 1.2-2.5GHz.

efficiency, has been measured at a centre-frequency of 1.8GHz. At the extremities of the measured PA bandwidth (1.4 and 2.2GHz), the averaged ACPR is –30dBc and –35dBc respectively, operating at 2dB peak compression.

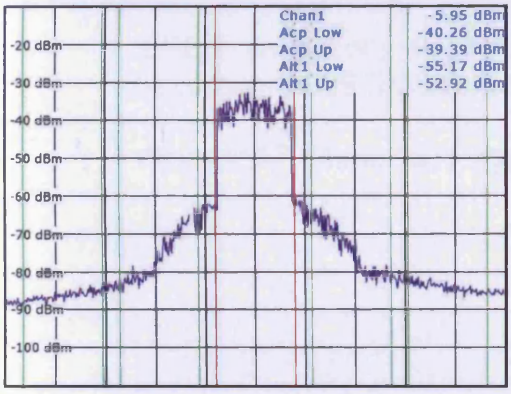

Fig. 8. Output spectrum from class-J PA, measuring ACP for a 5MHz WCDMA signal at centre frequency 1.8GHz, 39% average efficiency.

The symmetry of the upper and lower ACP sidebands, as in Fig. 8, implies minimal memory effects and good potential pre-distortability.

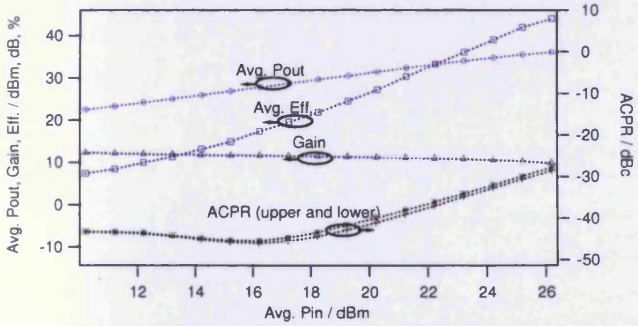

Fig.9. Average class-J PA performance with a power-swept 5MHz WCDMA signal at centre frequency of 1.8GHz.

V. Conclusion & Discussion

This paper demonstrates the fully realised performance potential of the class-J mode of PA in terms of efficiency, bandwidth, and linearity. Using waveform engineering techniques, including active harmonic load-pull, on a packaged 10W GaN HEMT power transistor, an efficient, broadband PA design has been obtained and realised. The bandwidth achieved with this PA operating at a drain efficiency of between 60-70% was 1.35 to 2.25GHz (50% at 1.8GHz centre frequency). At the same time, fundamental output power was up to 11W whilst at P2dB compression. At an ACPR for a 5MHz WCDMA signal of –30dBc, average output power was 35.5dBm and efficiency was 42%.

Acknowledgement

Research reported in this paper has been supported by Milmega Ltd., for financing the research and CREE Inc. for supply of devices.

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"A methodology for realizing high efficiency class-J in a linear and broadband PA"

P. Wright, J. Lees, P. J. Tasker, J. Benedikt, S. C. Cripps

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A Methodology for Realizing High Efficiency Class-J in a Linear and Broadband PA.

Peter Wright, J. Lees, J. Benedikt, P. J. Tasker, *Senior Member, IEEE*, and Steve C. Cripps, *Senior Member, IEEE*

Abstract—**The design and implementation of a class-J mode RFPA (RF power amplifier) is described. The experimental results indicate the class-J mode's potential in achieving high efficiency across extensive bandwidth, whilst maintaining predistortable levels of linearity. A commercially available 10W GaN (gallium nitride) HEMT device was used in this investigation, together with a combination of high power waveform measurements, active harmonic load-pull and theoretical analysis of the class-J mode. Targeting a working bandwidth of 1.5-2.5GHz an initial PA design was based on basic class-J theory and CAD simulation. This realized a 50% bandwidth with measured drain efficiency of 60-70%. A second PA design iteration has realized near-rated output power of 39dBm and improved efficiency beyond the original 2.5GHz target, hence extending efficient PA operation across a bandwidth of 1.4-2.6GHz, centered at 2GHz. This second iteration made extensive use of active harmonic load-pull and waveform measurements, and incorporated a novel design methodology for achieving predistortable linearity. The class-J amplifier has been found to be more realizable than conventional Class-AB modes, with a better compromise between power and efficiency tradeoffs over a substantial RF bandwidth.**

Index Terms—**Broadband, class-J, high efficiency, power amplifiers.**

I. Introduction

A design for wireless communication has, until recently, Pbeen focused on specified RF bandwidths of 5% or lower, due mainly to the very tight spectrum allocations. Future systems, including WiMax, 4G and beyond, will likely require larger bandwidths, not just due to wider spectral allocations, but the base bandwidth of the signals themselves which may well extend up to, and ultimately exceed, 100MHz. To date, other RFPA applications, such as radar and ECM have not profited from advances in power and efficiency due to their much wider RF bandwidth requirements. Reported results on very high efficiency PAs, typically operating above 75% efficiency, tend to rely heavily upon precise multi-harmonic impedance terminations at the DUT (device-under-test) as well as very high levels of device gain-compression. Both of these factors lead to narrowband frequency performance limitations (less than 10%) and non-linear operation respectively. A newly presented mode of operation - class-J [1] - has shown the theoretical potential of obtaining linear RFPAs that have the same efficiency and linearity as conventional Class-AB designs but do not require a band-limiting harmonic short.

This paper follows on from research presented in [2] and describes some of the key results obtained in that work in which design and realization of PA matching networks has yielded a broadband amplifier operating at high efficiency. In addition, an application of new theory [3], from which a furthering of the novel broadband class-J design methodology has been made, is presented and an enhanced PA design realized increasing the relative bandwidth-efficiency. This second and new design iteration makes comprehensive use of active load-pull, or 'waveform engineering' techniques, and uses a novel design methodology to achieve predistortable linearity. To our knowledge, such a design has never before been attempted on an *a priori* basis.

The high power measurement and characterization capability at our facility [4] has been utilized in the development of this broadband PA design methodology, enabling significant investigations into the realizable bandwidth-efficiency performance of the class-J mode of PA using a GaN HEMT power transistor.

Waveform and systematic load-pull measurement data has been used in the development stage of the design procedure, whilst also being used to analyze the extent to which optimum broadband high-efficiency operation has been achieved in this mode. Measurements have been focused around a target bandwidth of 1.5-2.5GHz.

Device output parasitic de-embedding has been applied to the waveforms captured at the calibrated measurement plane of the device package in confirming class-J behavior from the output voltage and current waveforms at the device plane [5].

II. The Class-J Mode of Operation

A. *Class-J Harmonic Load Terminations*

Cripps [1], who acknowledges some earlier work by Raab [6] has described class-J, defined as a mode in which the voltage has harmonic components which make it tend asymptotically towards a half-wave rectified sine-wave. This in practice can be usefully approximated by a suitably phased second harmonic component. The key difference between class-J and most other high efficiency modes is the requirement for a reactive component at the fundamental load.

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This is necessary to maintain a second harmonic voltage phasing that is beneficial to efficiency, whilst maintaining a physically realizable impedance termination at the second harmonic. In this way, a higher fundamental component can significantly outweigh the loss in power implied by the reactive load, a counter-intuitive result that has been discussed in detail elsewhere [1].

A class-J design thus displays approximate half-wave rectified sinusoidal output current and voltage waveforms, with a phase overlap between the two (Fig. 1). This mode of operation lends itself very well to the process of waveform engineering, as described previously by some of the current authors [4], [7]. Independent bias and drive control, and active multi-harmonic load-pull are used to engineer the shape of the current and voltage waveforms respectively.

The class-J output voltage waveform - assuming two-harmonics - is specified in Table I [1]. From this the fundamental and second-harmonic impedances, as defined in equations (1) and (2), can be found, thus defining the matching criteria. In order to optimize efficiency, the GaN device requires some compromises in setting the design values for the fundamental ('load-line') resistance, due to the effect of the DC 'knee'-voltage offset [8].

TABLE I
IDEAL CLASS-J VOLTAGE WAVEFORM, ASSUMING TWO HARMONICS

Harmonic	Normalized voltage component
1	$1.41 \angle 45°$
2	$0.50 \angle -90°$

$$Z_{f_0} = R_L + j \cdot R_L \qquad (1)$$

$$Z_{2f_0} = 0 - j \cdot \frac{3\pi}{8} \cdot R_L \qquad (2)$$

Ideal class-J theory assumes that there is no third-harmonic component present in the voltage waveform, and hence Z_{3f0} is assumed short. This required loading can usually be readily approximated through the effect of the device output capacitance within a PA matching network design, which thus has the tendency to provide a short to all of the higher harmonics. Fig. 1 illustrates measured waveforms with these harmonic terminations, however in this measurement the third harmonic load was allowed to be adjusted slightly in order to demonstrate optimum efficiency (as specified in Table II). The bias point implemented here was deep class-AB ($I_{dq} \approx 5\%$ of I_{dss}).

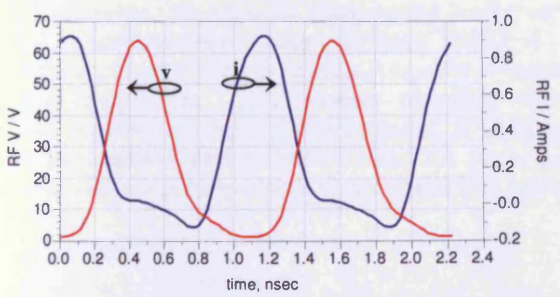

Fig.1. Measured class-J waveforms on a 10W GaN HEMT [2].

TABLE II
CLASS-J I_{GEN} (CURRENT GENERATOR)-PLANE LOAD TERMINATIONS

Frequency	I_{gen}-Plane Load Impedance
f_0	43.8 + j45.2 Ω
$2f_0$	1.6 – j52.0 Ω
$3f_0$	2.4 – j49.7 Ω

B. Waveform Engineering Very High Efficiency Class-J Operation in a GaN HEMT

By applying the prescribed class-J impedance components up to $3f_0$, through active load-pull, very high efficiency device operation has been measured at a fundamental frequency of 1.8GHz. The power sweep for this optimum emulated case is shown in Fig. 2. This shows the output performance of the DUT in a class-J loading configuration, operating with a bias point in class-C. A peak drain efficiency of 83% has been measured in this state with just below 10W device output power and approximately 3.5dB of gain compression. Note that even at the 6dB power back-off point, the measured drain efficiency is still above 60%. Device output power is however slightly less than was observed for the same device type in an optimized class-F/class-F^{-1} PA mode, within the same boundary conditions [7].

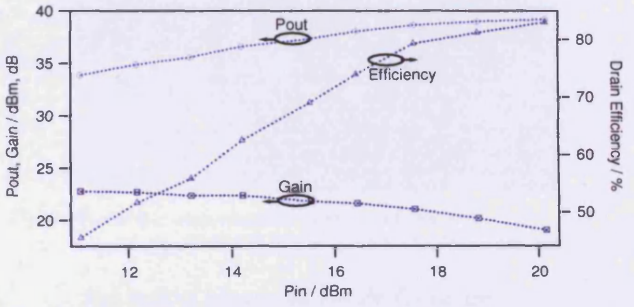

Fig. 2. Power sweep showing very high efficiency class-J operation at 1.8GHz [2].

Following this initial performance characterization of the class-J mode, a linear 10W broadband PA design was initiated, with a goal of above 60% efficiency over the 50% bandwidth of 1.5-2.5GHz.

III. A BROADBAND LINEAR CLASS-J PA DESIGN

A. Broadband Measurements and PA Realization

Active harmonic load-pull was initiated on the GaN transistor to be used in the design, using the three-harmonic active load-pull set-up [4]. This was carried out at several frequencies between 1.5 and 2.3GHz in order to begin the design stage of the broadband class-J PA. The device was set in the same state of gain compression (approximately P2dB) in each class-J measurement scenario. Working with device measurement data at the calibrated package-plane (i.e. without output parasitic de-embedding applied) the resulting load-pull sweep data was used to map out the drain efficiency as a function of fundamental load impedance on the Smith chart, with the second and third harmonic impedances fixed according to the ideal class-J terminations stated in Section II-*A*.

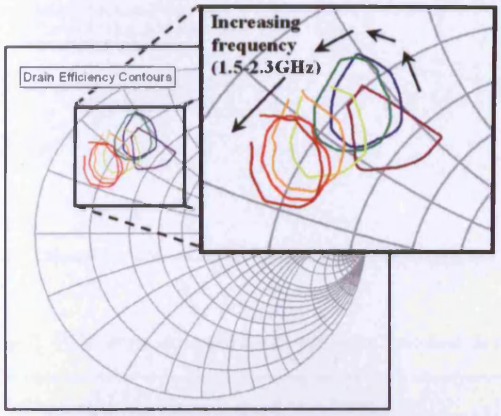

Fig. 3. Measured load-pull data for GaN HEMT indicating load impedance contour for 70% P2dB drain efficiency between 1.5-2.3GHz [2].

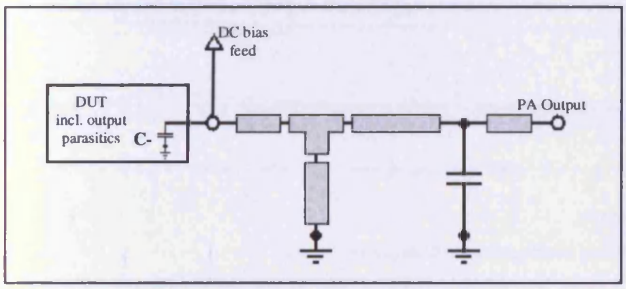

Fig. 4. Realized load matching network schematic [1].

Fig. 3 shows the 70% drain efficiency contour obtained from each fundamental load sweep, indicating the movement of the optimum fundamental load for efficiency at the device package-plane as a function of frequency. A corresponding output power contour plot was extracted following the load-pull sweep which provided a 'target region' of load impedances for which to aim a matching circuit design to provide a compromised class-J PA output power and drain efficiency.

The original target frequency band was 1.5-2.5GHz and in designing a suitable matching network over this extended bandwidth, some compromises have to be made. The initial strategy on the first design iteration (presented in this section) was to give higher priority to the fundamental impedance and allow the second harmonic more latitude. This particular device has a low output capacitance (approximately 1.5pF) which at 2GHz is itself quite close to the optimum reactive termination at the second harmonic. Thus the network itself mainly synthesises the required fundamental load over the extended bandwidth, but through a shunt inductive stub increases the effective second harmonic capacitive reactance for lower frequencies. The output matching network schematic is shown in Fig. 4. For purposes of comparison between the load-pull data and the realized PA performance, the same 50-Ohm input impedance environment was used.

B. Realized Class-J Performance Results - Efficiency and Output Power vs. Frequency

The first realized design iteration of the class-J amplifier is shown in Fig. 5. Power sweeps over a 12dB range were carried out on the PA across a frequency range of 1.2-2.5GHz. Results of this sweep are shown in Figs. 6 and 7. The efficiency performance at the P2dB compression state is displayed; this is customarily used as an 'end-point' for useable high-end efficiency performance in high PAR (peak-to-average ratio) linear signal applications.

As seen in Fig. 6, the measured P2dB drain efficiency for the realized class-J amplifier is at a level of 60-70% between 1.35GHz and 2.25GHz; a 50% bandwidth about a centre frequency of 1.8GHz. Within this bandwidth corresponding output power from the amplifier is between 9 and 11.5Watts.

A comparison between the realized PA results and simulated efficiency from the non-linear device model, set in the same impedance environment, is also shown in Fig. 6.

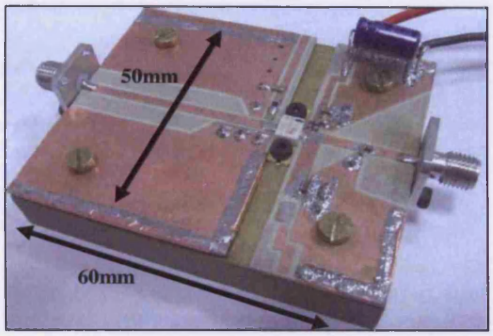

Fig. 5. Realized class-J amplifier - output matched only.

C. Analysis of Measured PA Performance

The results from this realized class-J design show a wide bandwidth of high efficiency operation; however the optimum performance is not obtained all of the way to the top end of the initially desired 1.5-2.5GHz bandwidth, i.e. above 2.2GHz, efficiency and output power begin to roll off. Using the active harmonic load-pull test set-up to present the same impedance environment as the PA (up to the second harmonic), a verification of the expected performance could be ascertained, as in Fig. 6, allowing for further investigation into the reasons for the reduced performance, and hence indicate actions to take in order to improve the high-end performance.

The load-pull results - in which the fundamental and second harmonic load impedances were presented to the device - highlights the same trend in device drain efficiency, in particular the drop in efficiency above 2.2GHz.

By introducing refinements in the basic class-J theory [3] into the design approach, a new enhanced design was made, aimed not only at improving the high-end efficiency and output power, but also addressing linearity, and potentially, predistortability.

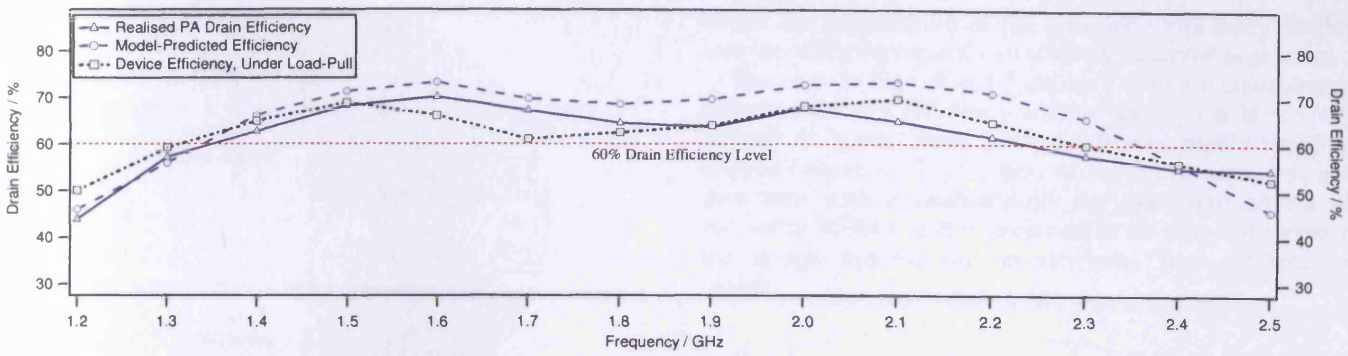

Fig. 6. P2dB drain efficiency for device under load-pull, device model-simulation and for the realized class-J PA across a bandwidth of 1.2-2.5GHz.

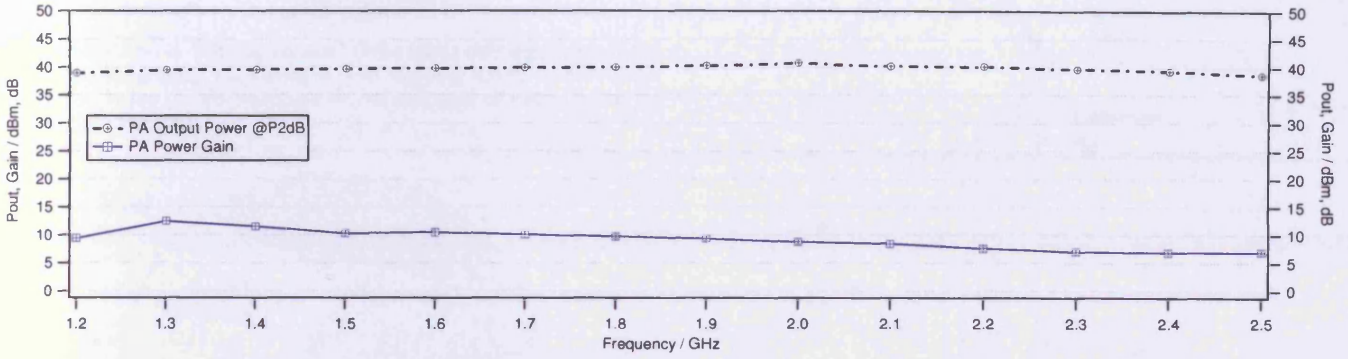

Fig. 7. Realized class-J PA output power and gain at P2dB across bandwidth of 1.2-2.5GHz.

IV. Class-J Linearity and Clipping Analysis

A. *Wider Bandwidth Potential of the Class-J Mode*

As shown in [3], the 'class-J mode' encompasses a continuum of high efficiency performance modes, each with a reactively terminated second harmonic load. The fundamental load has to have a corresponding reactive component in order to maintain a 'positive-definite', or non-zero-crossing voltage waveform. This continuum applies for second harmonic capacitive reactance terminations up to the short-circuit condition for class-B, and extends beyond this point towards what is denoted as the class-J* mode [3], i.e. the conjugates of the class-J loads in (1) and (2).

It is therefore possible to utilize this 'design-space' to implement an amplifier which has comparable efficiency, power and linearity performance as is regularly obtained using conventional class-AB design methodology, but retains almost constant performance over a substantially extended bandwidth. To our knowledge, such a design has never before been attempted on an *a priori* basis.

B. *Use of 'Clipping Contours' for Quasi-Linear Design*

The device output voltage, V_o, in a class-J PA can be written in the form [3];

$$V_o(\theta) = V_{dc} - V_{1r}\cos\theta + V_{1q}\sin\theta + \sum_n V_{nq}\sin(n\theta) \qquad (3)$$

$(\theta = \omega t)$

where in this case $n = 2$, and r and q denote the real and quadrature voltage components respectively.

If the minimum value of V_o approaches the device 'knee' (v_{min}) at any point in the RF cycle, the device current will start to 'clip', resulting in highly non-linear behavior. Such clipping will clearly cause gain compression, or AM-AM distortion, and if there is a significant phase angle between the fundamental components of current and voltage it is, in addition, a primary cause of AM-PM distortion. These strongly non-linear effects not only cause spectral distortion but can also lead to increasing problems when attempting to linearize the device using input signal predistortion.

It is therefore of much relevance to examine the parametric dependency of the 'zero-crossing' behavior of the voltage expression in (3). Even with the convenient approximation, $v_{min} = 0$, this is a mathematical problem of some complexity which we have analyzed in more detail elsewhere [3]. But for the present purpose it is possible to transform the clipping expression into a more simple graphical representation. If we assume that the current waveform remains a classical reduced-conduction-angle class-AB form, the voltage parameters V_{1r}, V_{1q} and V_{2q} in (3) can be considered to be directly proportional to the corresponding impedances at the fundamental and second harmonic. With knowledge of the impedance environment, and the assumed current waveform, (3) can be evaluated to determine whether it has a positive or negative value. Figs. 8a and 8b show how this calculation can be plotted on an impedance plane; in this case we vary the fundamental impedance (hence the V_{1r} and V_{1q} value) across the entire Smith Chart plane, for specific fixed values of Z_{2f0} (hence V_{2q}). The shaded portions indicate the clipping regions where the voltage expression crosses zero at some point in the cycle.

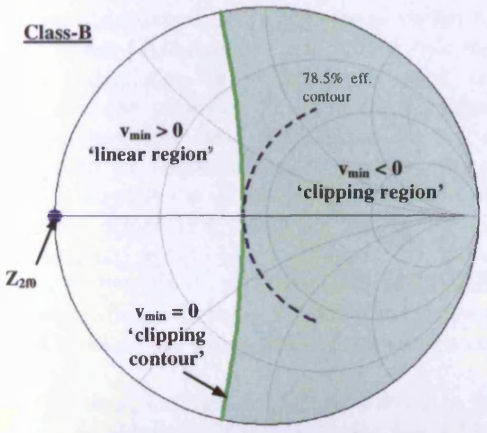

Fig. 8a. Class-B 'clipping contour' (solid trace) indicating fundamental loads for 'zero-grazing' v_{min} condition, with 'clipping region' shaded. 78.5% efficiency contour (dotted trace) also shown, indicating an optimum load for linearity and efficiency.

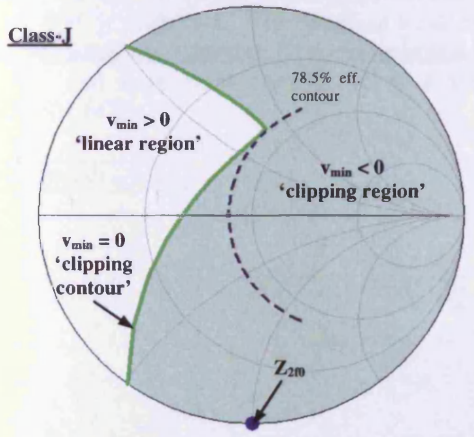

Fig. 8b. Class-J 'clipping contour' (solid trace) indicating fundamental loads for 'zero-grazing' v_{min} condition, shaded 'clipping region' and optimum load for class-J linearity and efficiency.

The shaded regions, as shown in Figs. 8a and 8b, thus provide a design guide as to load conditions that should be avoided in the circuit design process. The line which delineates the clipping region is called the 'clipping contour'. This contour in effect shows the impedance conditions for which the voltage 'grazes' zero. However, the choice of fundamental impedance will also determine the final power and efficiency. In principle, if the real part of the fundamental impedance is maintained at a constant value, equal to the device 'load-line' resistance, maximum power and efficiency will be maintained (corresponding to a fixed value of V_{1r} in (3)). This constant maximum efficiency contour is also plotted (dotted traces) in Figs. 8a and 8b. In practice, of course, the only allowable maximum efficiency condition will be the one that sits on the 'clipping contour', which can be seen to be a singular point in each case. Fig. 9 shows how the clipping contour changes as the value of second harmonic reactance is varied over the class-J range. It is of interest to note that in practice, although the clipping process will change the assumed current waveform, and as such the power and efficiency can no longer be simply related to the value of V_{1r} in (3), the continuation of the maximum efficiency condition into the 'clipping region' can often be observed in practice.

The plots in Figs. 8 and 9 define a design methodology for obtaining the best efficiency without forcing the device output voltage to 'graze' zero and thus display highly non-linear, clipped behavior. To the best of our knowledge, this is the first time such a methodology has been defined for high efficiency RFPAs, and is proposed as an essential element in the design process for broader-band, high-efficiency PA design.

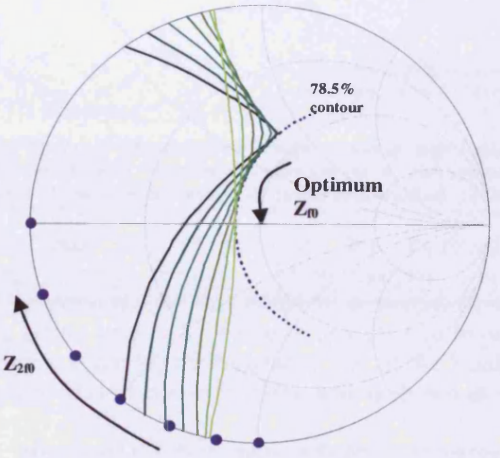

Fig. 9. $v_{min} = 0$ 'clipping contours' indicating optimum fundamental load for efficiency, as second harmonic load impedance is varied between the class-B and class-J conditions.

C. Practical Verification of Class-J Mode in High Power Devices - Effect of Second Harmonic (LP measurements)

Since for a broadband PA design - and especially PAs covering octave bandwidths - the high-end fundamental impedance tends towards the second harmonic impedance at the low-end of the band, it was necessary to observe the effect that a non-ideal (i.e. not purely reactive) second harmonic load impedance has on class-J efficiency [9]. This was carried out with a fixed fundamental load of (30+j30)Ω ($I_{gen.}$-plane), fixed third harmonic impedance of 50Ω (package-plane) and for a device bias condition of I_{dsq}=100mA (deep AB, approximately 5% I_{dss}).

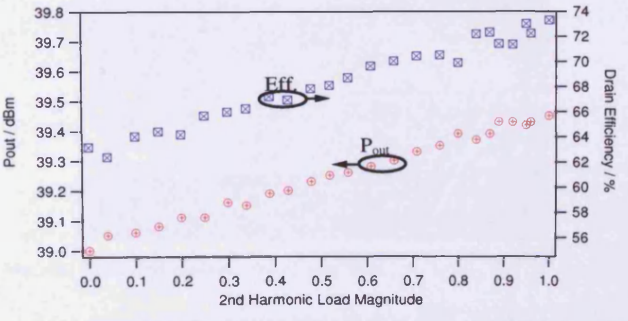

Fig. 10. Measured effect of the real component of second harmonic load on class-J output power and efficiency.

The results in Fig. 10 show a 10% decrease in efficiency, and almost 0.5dB reduction in output power as the magnitude

of the second harmonic load impedance is varied from 1 to 0 at the $I_{gen.}$-plane. Although at first glance this result shows substantial degradation in performance, there is also the indication that the transition between the fundamental load and second harmonic load impedance across an octave bandwidth can be implemented in such a way as to not dramatically degrade the efficiency performance of a class-J PA operating across this frequency range, for example; a second harmonic reflection coefficient of magnitude 0.5 would suggest just 5% drop in efficiency and 0.25dB drop in output power, whilst still being a suitable fundamental load for this device if combined with a reactive impedance component.

D. Practical Verification of Class-J Mode in High Power Devices - Improved Class-J Design Space LP Results

By following investigations in [3] and simulation findings in Section IV-*B* the second harmonic load impedance was varied between +165 and –105 degrees at the $I_{gen.}$-plane (done so through the use of output parasitic de-embedding), with magnitude 0.95 in each case. The optimum fundamental load for peak efficiency was targeted. The results of this are shown in Fig. 11, and have been carried out at a fundamental frequency of 1.8GHz.

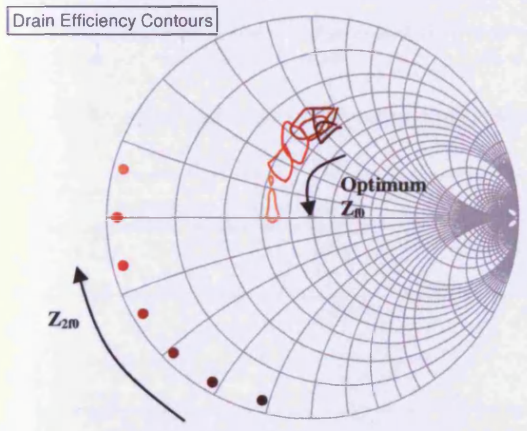

Fig. 11. Mapping the optimum (top 2%) efficiency contour as a function of changing second harmonic load impedance - $I_{gen.}$-plane impedances shown.

The measured results in Fig. 11 show reasonable agreement with the theoretical analysis of class-J and the proposed 'design space' for continuous high efficiency performance, as the second harmonic and fundamental load impedances are allowed to vary away from the class-B case. Since the same theory can be applied to the 'complimentary' class-J* mode, corresponding to inductive second harmonic terminations, the potential for a broadband high efficiency PA is clear.

V. An Enhanced Design Following Extended Theory

A. Re-designing the Class-J Output Matching Network

Using the analysis found/developed in the previous section, an iteration of the initial matching network, using the same architecture as previous (Fig. 4), was made in line with the intention of 'moving' the fundamental loads that were encroaching on the 'clipping', or non-linear region of the Smith Chart, and more precise placement of the second harmonic load, in particular regards to the phase. This second design iteration is shown by the s-parameters of Fig. 12, giving a comparison with the first output matching design.

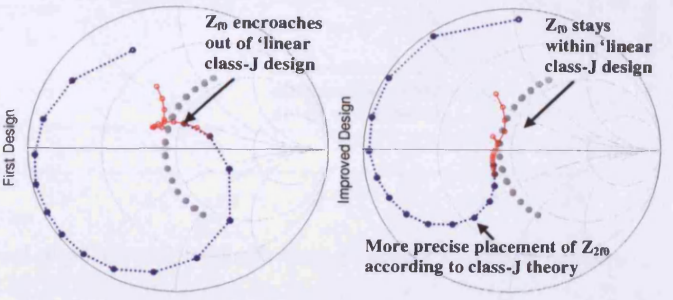

Fig. 12. Second iteration of class-J output matching (right) compared with first initial design (left), showing fundamental (solid) and second harmonic (dotted) load impedances between fundamental bandwidth of 1.2-2.6GHz.

In the same way as previous, this improved design, following extended theoretical-based analysis, was used to predict the performance that could be expected from the PA by using active load-pull. These results showed improvement in efficiency at the higher frequency end of the bandwidth of operation as desired, above 2.2GHz, and as shown in Fig. 14.

B. Measured PA Performance following Improved Output Matching Network Design

In characterizing the second realized PA, power sweeps were again conducted at 100MHz frequency spacing and the efficiency at P2dB (2dB gain compression point) was recorded, along with the output power and amplifier gain. These sets of results are displayed also in Fig. 14 and Fig. 15, along with the first design iteration results for comparison.

Measured P2dB output power, as in Fig. 15, indicates the flat characteristic associated with this broadband design, at a value of 39.5±0.5dBm (approximately 9-10W). The improvement in drain efficiency of the second iteration PA is evident in Fig. 14 between 2.3 and 2.6GHz, with up to 8% improvement obtained at 2.5GHz.

Fig. 13 shows the improved class-J amplifier.

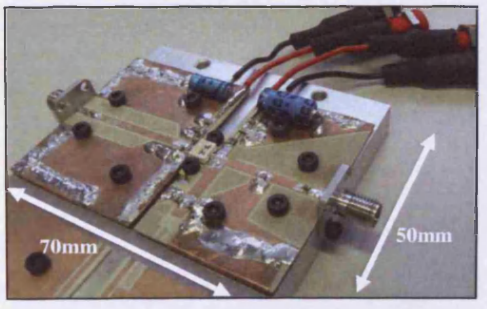

Fig. 13. Improved realized class-J amplifier.

VI. Input Matching and Affect on PA Performance

For comparison purposes the PA was measured with the same input impedance as the device was measured during the load-pull design stage; with a broadband 50Ohm impedance and not for best gain.

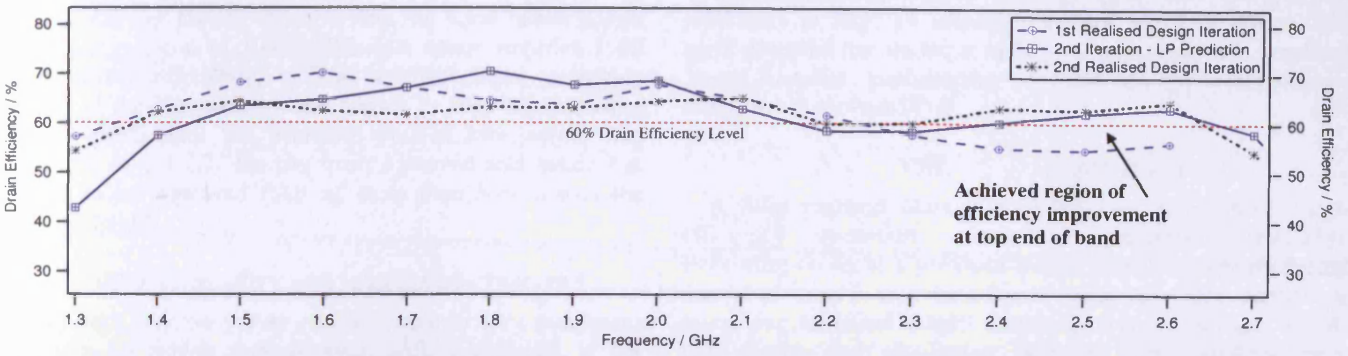

Fig. 14. Prediction and measurement of PA efficiency performance with enhanced output matching, compared with first class-J PA design performance.

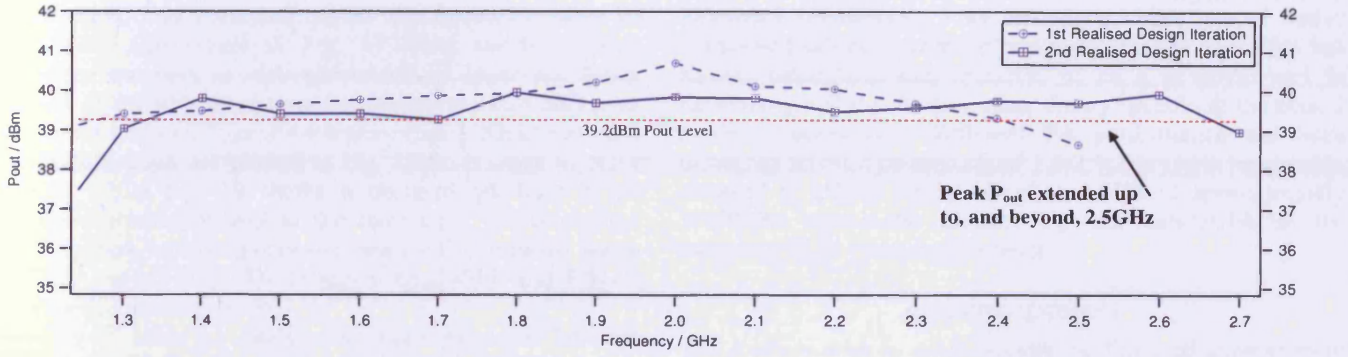

Fig. 15. Broadband measurement of PA output power performance with enhanced output matching, compared with first class-J PA design iteration.

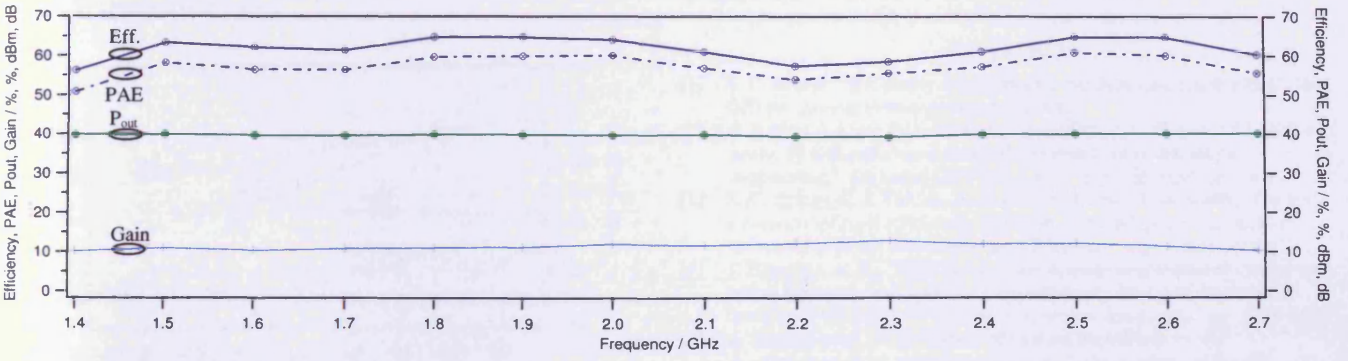

Fig. 16. Broadband measurement of PA performance with enhanced output matching, and input matching.

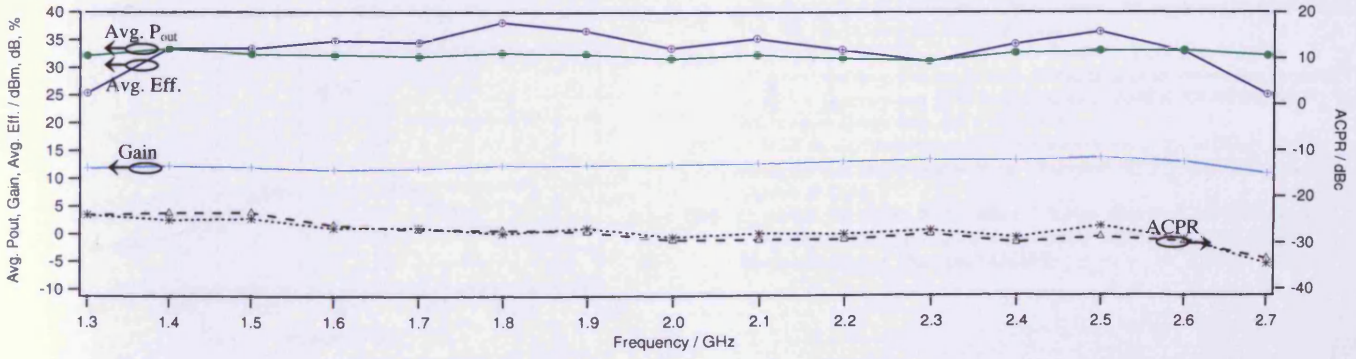

Fig. 17. Broadband PA linearity characterized under stimulus of 5MHz BW, 8.51dB PAR, WCDMA signal.

Following the performance characterization in the previous sections attention turned to improving the input match across the frequency band of 1.4-2.6GHz and hence improve PAE (power-added efficiency). The applied input matching resulted in the PA performance shown in Fig. 16, including PAE. Here, gain of between 10.2-12.2dB across the bandwidth of 1.4-2.7GHz has been observed and hence has resulted in an improved PAE of more than 50% across the same bandwidth.

VII. PA LINEARITY AND ACPR CHARACTERISTICS

Very high efficiency PAs can be prone to very non-linear characteristics which present users with a difficult, if not impossible, task of predistorting the PAs to meet communication system standards. ACPR, without any form of predistortion, was measured across the frequency range of 1.3-2.7GHz and results in Fig. 17 show average power, efficiency and gain as well as worst-case upper and lower channel ACPR with drive power sufficient to cause 2dB peak compression. At a CF (centre-frequency) of 2.0GHz, the same PA characteristics are plotted in Fig. 18 for a range of drive powers, whilst Fig. 19 shows a captured spectrum at an average efficiency of 40% at the same CF. The modulated signal applied, in order to characterize the PA linearity, was a WCDMA signal of 3.84MHz signal bandwidth and 8.51dB PAR (peak-to-average ratio).

ACPR of close to –30dBc has been measured between 1.7-2.7GHz, decreasing to approximately –25dBc below 1.7GHz; this at the same time as the PA operating at more than 30% average efficiency.

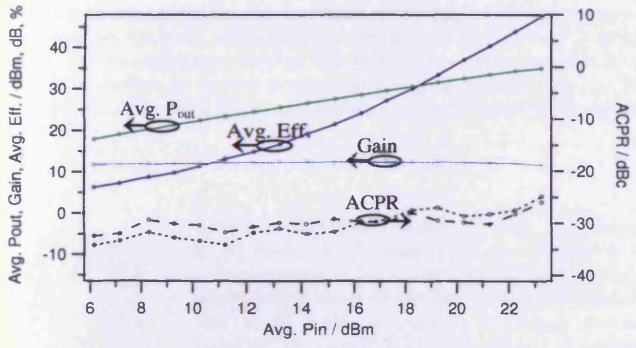

Fig.18. Class-J PA performance with a power-swept 5MHz BW, WCDMA signal at centre frequency of 2.0GHz.

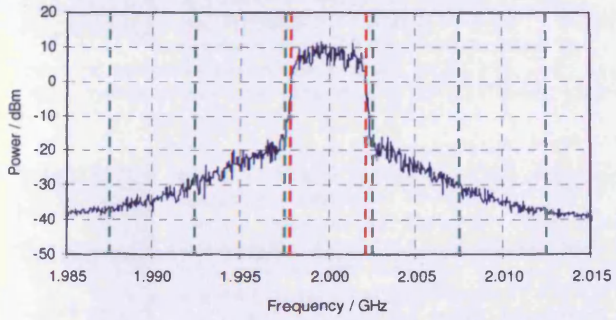

Fig.19. Output spectrum from class-J PA, measuring ACP for a 3.84MHz WCDMA signal at centre frequency 2.0GHz, and at 40% average efficiency.

The relative symmetry of the upper and lower ACP sidebands in Fig. 19 implies minimal memory effects and good potential for predistortability. We attribute this excellent 'raw' linearity performance to the design methodology described in section IV-*B*.

VIII. CONCLUSION

A fully realized class-J amplifier has demonstrated high efficiency operation across a substantial bandwidth. Following on from a previous paper, further newly presented theory of class-J as a broadband mode has been applied in improving an initial output matching network design. Load-pull results and simulation analysis have justified these changes and enabled a second design and fabrication of an output matching network which has shown improved efficiency performance with frequency. The use of active harmonic load-pull and waveform measurement capability has shown, throughout this research, to be a powerful tool in developing real PA designs using theory specific to the class-J mode of operation. Efficient PA performance has been measured across a bandwidth of 1.4-2.6GHz (60% bandwidth, centered at 2GHz) whilst showing ACPR of approximately 25-30dBc across the entirety of this bandwidth at the measured P2dB compression level.

ACKNOWLEDGMENT

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Steve C. Cripps obtained his Ph.D. degree from Cambridge University, England. He worked for Plessey Research on GaAsFET hybrid circuit development. Later he joined Watkins-Johnson's solid state division, Palo Alto, CA, and has held Engineering and Management positions at WJ, Loral, and Celeritek. During this period, he designed the industry's first 2-8 GHz and 6-18 GHz 1 watt solid state amplifiers, and in 1983 published a technique for microwave power amplifier design, which has become widely adopted in the industry. In 1990 he became an independent consultant and was active in a variety of commercial RF product developments, including the design of several cellular telephone power amplifier MMIC products. In 1996 he returned to England, where his consulting activities continue to be focused in the RF power amplifier area. He has recently published a second edition of his best-selling book, "RF Power Amplifier Design for Wireless Communications" (Artech House). He is currently vice-chair of the High Power Amplifier subcommittee of the Technical Co-ordination and Technical Program Committees of the IEEE Microwave Theory and Techniques Society, and writes the regular "Microwave Bytes" column in the IEEE Microwave Magazine. Dr Cripps has recently been appointed a Professorial Research Fellow at Cardiff University, UK. He is the 2008 recipient of the IEEE Microwave Applications Award.

6.

"Power amplifier memory-less pre-distortion for 3GPP LTE application"

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Power Amplifier Memory-less Pre-distortion for 3GPP LTE Application

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Abstract— **A new and simple Power Amplifier (PA) linearization method is proposed and demonstrated using a very high efficiency yet inherently nonlinear inverse class-F PA. This was conducted in the presence of a generic variable envelope RF signal in order to extract its AM-AM and AM-PM characteristics. Deducing the polynomial pre-distortion parameters from the AM-AM and AM-PM characteristic has resulted in the successful linearization of the PA in the presence of 3GPP Long Term Evolution (LTE) signals. The results obtained for the PA - a 12W GaN HEMT inverse Class-F structure designed to operate at 900MHz - demonstrate the proof of concept and the efficiency of the proposed linearization technique with significant advantageous reduction in base-band resources for 3GPP LTE applications.**

I. Introduction

The 4th generation of wireless communication systems is to be deployed in the near future. This 3GPP LTE based protocol allows users to access various multimedia services by receiving up to 100Mbps download speeds. The possibility of achieving such high bit rates is only possible due to the use of a spectrally efficient complex modulation technique; Orthogonal Frequency Division Multiplex (OFDM). According to the recently updated 3GPP LTE technical specifications [1], the 3GPP LTE signal's dynamic range is given by the minimum values showed in Table I. The relative Peak-to-Average Power Ratio (PAPR) is variable and depends on the channel bandwidth and the number of allocated resource blocks. Clearly, the transmitter block, in the 4th generation wireless communication infrastructure, has to handle 3GPP LTE downlink signals which are variable in terms of bandwidth and PAPR.

TABLE I
3GPP LTE Downlink Characteristics

channel bandwidth (MHz)	Total power dynamic range (dB)
1.4	7.7
3	11.7
5	13.9
10	16.9
15	18.7
20	20

In the transmitter block, RF power amplifiers are known for their strong non-linear behaviour, and have to be designed to target a minimum linearity of 45dBc in terms of adjacent channel leakage ratio ACLR [1]. In order to achieve that level of linearity, several linearization techniques can be applied. One form of linearization used is digital (base-band) pre-distortion (DPD) [2][3][5]-[9]. The DPD intentionally distorts the input signal of a power amplifier in order to compensate for its non-linear behaviour. Pre-distorting the input signal requires the extraction of the inverse transfer function of the power amplifier in terms of AM-AM and AM-PM characteristics. Therefore, the quality of the linearization depends on the accuracy of the power amplifier AM-AM and AM-PM measurements. Moreover, the AM-AM and AM-PM characteristics depends on the RF signal used in the measurement procedure; i.e. the AM-AM and AM-PM profiles depend on the dynamics of the test signal in terms of bandwidth and PAPR [5]. In a 3GPP LTE context, the variability of the RF signals presents a challenge, and trying to characterize an amplifier for all the possible scenarios is difficult and time consuming. On the other hand, implementing in the base-band infrastructure several pre-distortion parameters, to compensate for all possible scenarios, results in large baseband memory requirements. Therefore, in order to achieve a reasonable base-band cost implementation, it is important to be able to linearize a power amplifier in such a way that this linearization can be applied in the presence of various 3GPP LTE signals. The scope of this paper is the implementation of a pre-distortion procedure, in the presence of several 3GPP LTE signals that linearises the power amplifier.

The proposed method extracts the pre-distortion parameters from the AM-AM and AM-PM characteristics obtained by driving the power amplifier using a generic, variable envelope signal. The use of the generic test signal allows the extraction of the "static" nonlinearities of the power amplifier, so that a memory-less polynomial pre-distortion method can be applied. The advantage of the proposed method is its simplicity and its suitability to a manufacturing environment.

The approach presented in this paper has been validated by linearizing a highly efficient 10W inverse Class-F PA .This 900 MHz structure uses a CREE 10W GaN HEMT and is particular interesting as this type of PA is typically considered unsuitable for use in modern communications systems due to its perceived inherent nonlinearity. The measurement setup and the linearization procedure are described in section II. The results are discussed in section III.

II. Measurement Setup and Linearization Procedure

A. *Setup Description*

Figure 1 shows the measurement setup used for the power amplifier AM-AM and AM-PM characterization. The RF generator (R&S SMATE200A) feeds the driver with a 3GPP LTE or a pre-distorted signal. The LZY-2 amplifier is able to deliver a suitably high output power level (47dBm) such that it can remain linear while driving the power amplifier over its entire dynamic range. The Device Under Test (DUT) comprises the inverse Class-F GaN HEMT PA followed by a 13 dB attenuator.

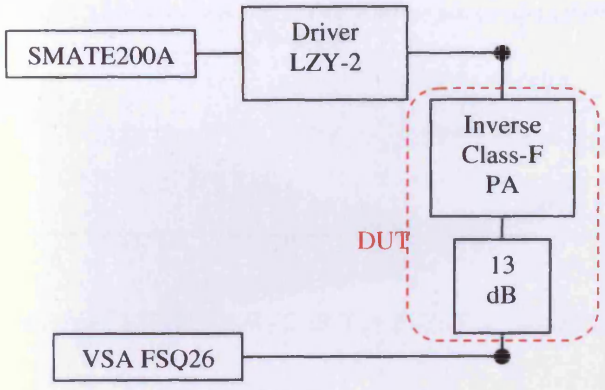

Fig. 1 Measurement setup for AM-AM and AM-PM Characterization

The inverse class-F PA was realised using a waveform-based design procedure [10]. This approach combines active high-power harmonic load-pull with high-frequency time domain measurement, and enabled the device output waveforms to be measured and 'engineered' for optimised inverse class-F mode behaviour, minimising overlap between the current and voltage waveforms and thus reducing dissipated energy. This technique enabled operation with peak Power Added Efficiency (PAE) of 80%, whilst delivering 12W from a 10W rated device. Figure 2 depicts measured current and voltage waveforms at the drain current generator of the DUT for several output power levels, and clearly show the expected square current waveform along with a half-rectified voltage waveform indicative of this mode of operation.

The PA operates with a 28V drain rail voltage and has a peak output power of 12W. Since the inverse class-F mode must operate at a high level of gain compression in order to achieve its high efficiency, the potential for nonlinear operation is very high. This has tended to limit practical application of inverse class-F in modern, linear communications systems. At the DUT terminations input and output complex envelopes are measured and the AM-AM and AM-PM characteristics are extracted using a vector signal analyser (VSA) (R&S FSQ26).

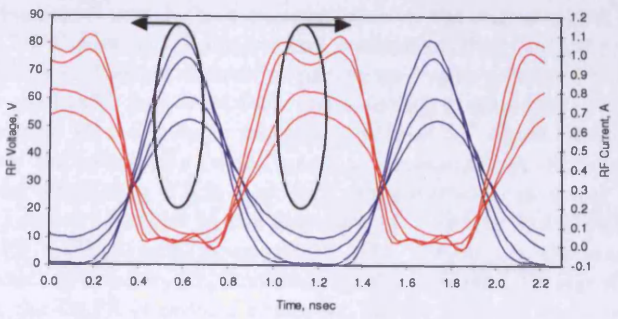

Fig. 2 Current and Voltage waveforms at the Drain current generator of the inverse Class-F power amplifier for several output power levels

B. *Linearization Procedure*

The generic signal used to extract the polynomial pre-distortion parameters is an RF signal with a repetitive triangle magnitude. The peak value of the triangle magnitude varies as shown in Figure 3. The period repetition of the generic RF signal magnitude is chosen to avoid the generation of some memory and thermal effects [2]. So that "true" static nonlinearities of the DUT can be measured accurately. The relative slow envelope variation of the generic signal (500kHz), allows the use of a reasonable acquisition speed and make delay compensation relatively simple.

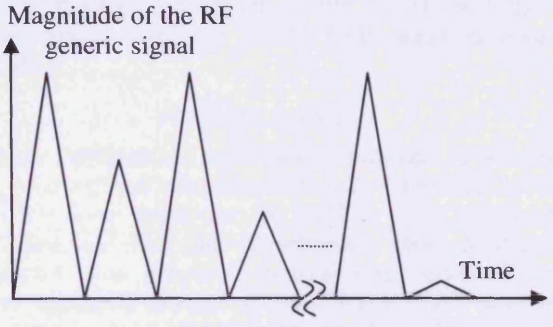

Fig. 3 Magnitude of the RF generic signal

Performing the same measurements in presence of wide band 3GPP LTE signals requires high frequency sampling, careful delay estimation and non-negligible data processing in order to estimate the static nonlinearities [5]. Figures 4 and 5 show AM-AM and AM-PM characteristics of the DUT using the generic RF signal and some 3GPP LTE signals. Results show that the obtained static nonlinearities, while the generic signal is applied, can be considered as a good approximation to those obtained in the presence of LTE modulated signals. Therefore, extracting polynomial pre-distortion parameters from the "generic" AM-AM and AM-PM should yield to good linearization performance in the presence of various 3GPP LTE signals. In fact, due to memory effects [5] and in the case of coarse delay estimations [4], AM-AM and AM-PM curves exhibit hysteresis behaviour. Therefore, extracting the polynomial pre-distortion parameters from the measurements performed in presence of the generic signal is a much easier task than doing this in presence of the wideband LTE signals.

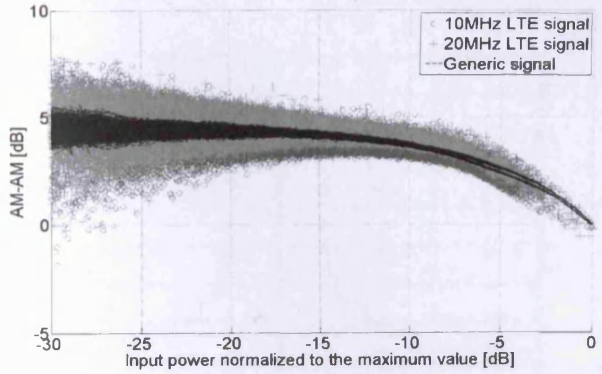

Fig. 4 AM-AM of the PA in presence of the generic signal and some 3GPP LTE signals

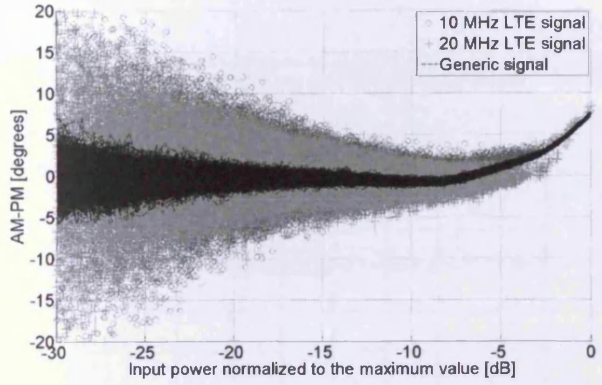

Fig. 5 AM-PM of the PA in presence of the generic signal and some 3GPP LTE signals

The accuracy and the efficiency of the pre-distortion rely strongly on the modelling of the true static nonlinearities of the DUT. But the use of a good approximation of these nonlinearities allows a linearization good enough to meet the 3GPP LTE linearity requirements (45dBc of ACLR).

III. Measurement Results

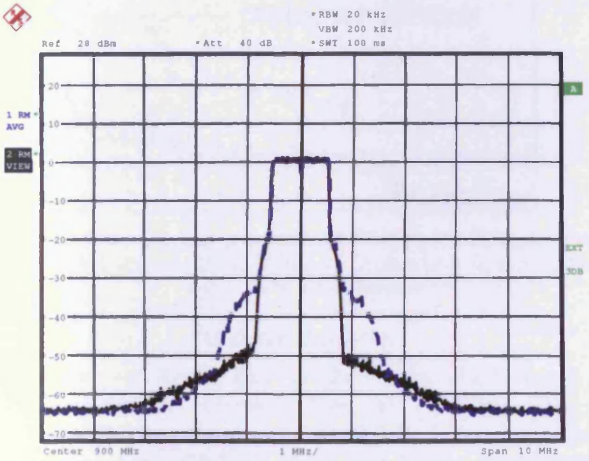

Fig.6 PA Linearization in presence of 1.4 MHz 3GPP LTE signal using a generic signal for AM-AM and AM-PM measurement.

Figures 6 and 7 show the spectrum of the output signal of the DUT with (solid curves) and without (dashed curves) pre-distortion. The pre-distortion parameters were extracted from the AM-AM and AM-PM characteristics obtained in the presence of the generic triangle envelope RF signal. Results show the efficiency of the proposed linearization procedure since more than 15dB and 5dB improvements in terms of ACLR are obtained in the presence of 1.4MHz and 20MHz 3GPP LTE signals, respectively. The reason for the small amount of linearity improvement for the 20MHz LTE signal is that the PAPR is around 15dB, so, further back-off is needed to drive the PA within its input dynamic range, and obviously the single ended PA tested in this study is less nonlinear at such back-off input power. Figure 8 shows the linearity improvement (10 dB in term of ACLR) of the DUT when a 10MHz LTE signal is applied and pre-distorted with the proposed method (solid curve). In order to verify the accuracy of the linearization with the generic signal, the 10 MHz LTE input signal is also pre-distorted using the AM-AM and AM-PM characteristic measured in presence of the 10MHz LTE signal (dashed curve). Similar performances are obtained when classic and generic linearizations are applied. This observation demonstrates that the generic signal is suitable for the extraction of memory-less polynomial pre-distortion parameters. In Figures 6, 7 and 8, the residual nonlinearities observed in the output signals after pre-distortion are attributed to memory effects, but all the results show that the linearized signals meet the 3GPP LTE standard linearity requirement.

IV. Conclusions

A generic linearization procedure is proposed in this paper. The proposed method is based on the use of a generic variable envelope RF signal applied to the DUT in order to extract its AM-AM and AM-PM characteristics for static nonlinearity compensation. The proposed method was validated on an inherently nonlinear inverse Class-F RF PA and successful linearization results are obtained enabling the very high efficiency RF power amplifier to meet the 3GPP LTE standard linearity requirements. This linearization strategy is simple, cost effective and suitable for a production environment for the following reasons:

- Simple extraction of the pre-distortion parameters due to the use of a relatively slow variable envelope RF signal.
- Less sensitivity to a coarse delay estimation of the AM-AM and AM-PM measurements.
- Pre-distortion parameters are valid in the presence of various LTE signals which relax the requirements on base band resources.

The main disadvantage of the proposed method is the fact that memory effects are not taken into account. This results in residual nonlinearities in the output signal after linearization, but good linearity performance was obtained for the PA measured for this paper. Work is currently under way addressing the issue of how memory effects can be taken into account using a modified form of the method described here.

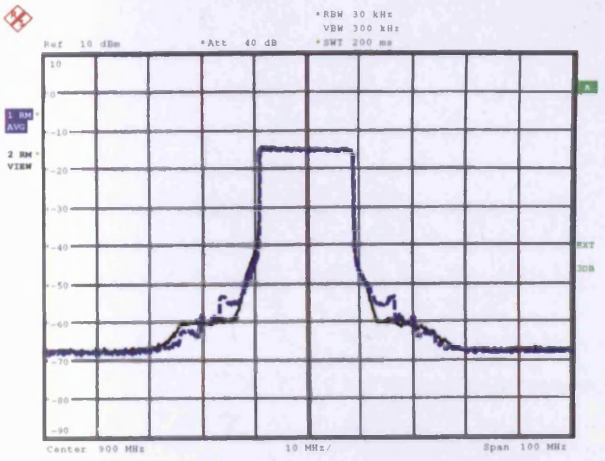

Fig. 7 PA Linearization in presence of 20 MHz 3GPP LTE signal using a generic signal for AM-AM and AM-PM measurement.

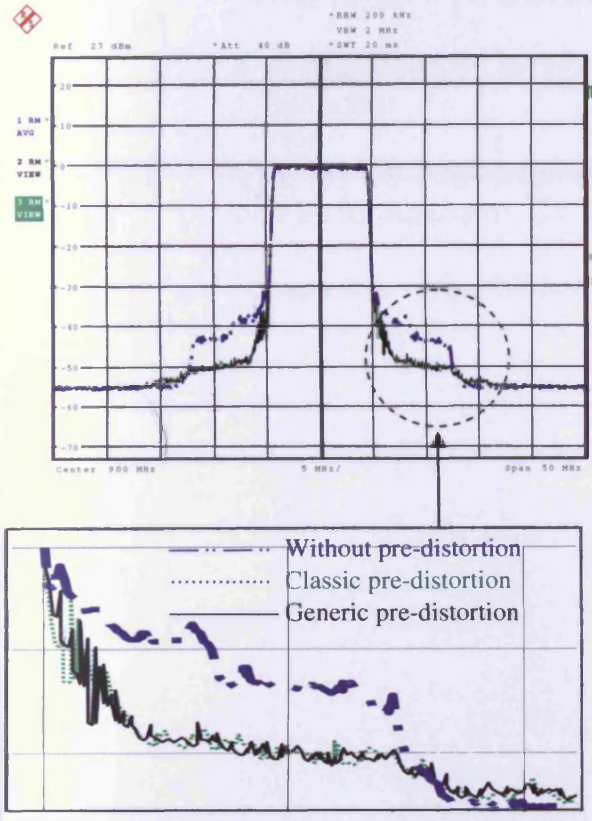

Fig. 8 PA Linearization in presence of 10 MHz 3GPP LTE signal using a generic (solid line), and 10MHz 3GPP LTE (dashed line) signal for AM-AM and AM-PM measurement.

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7.

"Novel wide band high-efficiency active harmonic injection power amplifier concept"

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Novel Wide Band High-Efficiency Active Harmonic Injection Power Amplifier Concept

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Abstract — **This paper introduces a novel approach for the realization of wide band (>octave) high-efficiency (>95%) high Power Amplifiers (PAs). The proposed concept utilizes active harmonic injection to achieve the appropriate waveform shaping of the voltage/current waveforms necessary to deliver simultaneously both high power and high efficiency operation. The new PA structure thus consists of two parallel PAs where the main PA generates fundamental power and an auxiliary PA injects a harmonic signal at the output of the main PA to perform waveform shaping. An active harmonic injection PA circuit designed around the 10 W GaN transistor is demonstrated, along with the basic mathematical analysis and computer simulation of this new mode of operation. The measured performance of the PA demonstrator realized at 0.9 GHz provided a drain efficiency of 74.3% at P1dB, validating the concept and its potential.**

Index Terms — **Broadband amplifiers, high efficiency, injection amplifiers, microwave amplifiers, power amplifiers.**

I. Introduction

In many communication and radar systems there is an increasing need to improve the functionality of the Power Amplifier (PA) to meet new system specifications; definitely in terms of output power, bandwidth, efficiency and often also linearity. For example, wireless communication systems consume significant electric power with the component consuming the largest amount of power being the Power Amplifier (PA), thus the importance of improving their efficiency.

Fundamentally the only way to improve the efficiency of a Power Amplifier is to use harmonic injection to provide for wave shaping of the RF output voltage/current waveforms. This harmonic injection is typically achieved by presenting appropriate passive reactive output load terminations at the harmonics. Power Amplifiers operating in the traditional class B (78.5%) and F (100%) modes are all examples of this approach. Generally these modes, since they require high Q-factor short and/or open circuit terminations, provide solutions that are inherently narrow band.

More recently and alternative mode of operation, class J (78.5%), was introduced that requires only reactive second harmonic terminations [1]. Additionally by exploiting the newly highlighted design continuum combining both the Class B and J modes this bandwidth limitation can be partially overcome. Recently a PA demonstrating high efficiency (>60%) over a 60% bandwidth has been demonstrated [2]. However, the maximum theoretical efficiency of this approach is only 78.5% and it cannot address systems requiring over an octave bandwidth.

This paper introduces a novel power amplifier approach, which utilizes active rather than passive second harmonic injection, to address these theoretical limitations on efficiency and bandwidth associated with passive second harmonic injection. The paper starts with an investigation of optimum waveforms that would deliver best performance in terms of efficiency and power. Next, the active load pull system developed by Cardiff University [3] was used to experimentally investigate whether the 10 W GaN transistor can support these optimum waveforms. Finally, a prototype amplifier test structure based on this new topology is designed, simulated, built and measured to demonstrate its feasibility.

II. Theoretical Analysis

A. Passive Second Harmonic Injection

In Class B and J amplifiers the transistor is initially biased so that, ideally, the resulting current waveform is shaped to provide a half rectified sinusoid. The key feature of the half rectified sinusoid is that over the same maximum current swing it provides for same fundamental signal as the sinusoidal waveform but importantly it has a reduced $(2/\pi)$ DC component, hence providing for an increase of $(\pi/2)$ efficiency. In Class B a short circuit at the second harmonic is used to shape the voltage waveform to a simple sinusoid. While in class J an appropriate fundamental and second harmonic reactive termination is used to shape the voltage waveform into a band limited half rectified sinusoid. In both these cases it is assumed that all higher harmonics are passively terminated into low impedance, in which case they both have a maximum theoretical efficiency of 78.5%.

B. Active Second Harmonic Injection

On close inspection it is observed that the performance potential of the Class J current and voltage waveforms is limited by the constraint of requiring passive harmonic injection. The two half rectified waveforms are offset by 135 rather than the optimum 180 case; the value required for a real only fundamental load (maximum output power) and to minimize current and voltage waveforms overlap (maximum efficiency).

The voltage and current waveforms in the optimum case are given by the following equations:

$$v(\theta) = V_{dc}\left[1 - \sqrt{2}\cos(\theta) + 0.5\cos(2\theta)\right] \qquad (1)$$

$$i(\theta) = I_{max}\left[\frac{1}{\pi} + \frac{\cos(\theta)}{2} + \frac{2}{3\pi}\cos(2\theta) + \cdots\right] \quad (2)$$

Indicated that the required optimum fundamental load is given by;

$$R_f = 2\sqrt{2}V_{dc}/I_{max} \quad (3)$$

Analysis of these waveforms indicates the following output power and efficiency performance.

$$P_{dc} = 2V_{DC}\,I_{max}/\pi = 2V_1/\pi R_f = 2\sqrt{2}V_{DC}^2/\pi R_f \quad (4)$$

$$P_{out} = V_1^2/2R_f = V_{dc}^2/R_f \quad (5)$$

$$\eta_{Drain} = P_{out}/P_{dc} = \pi/2\sqrt{2} = 111\,\% \quad (6)$$

Obviously efficiency greater than 100% is not theoretically possible. Further analysis of the current and voltage waveforms indicates that the required load impedance at the second harmonic is negative and is given by;

$$R_{2f} = -\frac{3\pi}{4}V_{dc}/I_{max} \quad (7)$$

While this is not possible with passive second harmonic injection it is achievable if active second harmonic injection is utilized. However, in this case the efficiency calculation must be modified, as follows, to include the addition of this energy input.

$$\eta_{IPA\,Drain} = P_{out}/(P_{dc} + (P_{dc0}/\eta_0)) \quad (8)$$

where P_{dc0} and η_0 are the DC power and efficiency of the generated harmonic power. The modified drain efficiency calculation shows that the efficiency of the second harmonic PA is important for achieving high overall efficiency. Table (1) shows the predicted theoretical performance when the efficiency of the second harmonic PA is 100% and 50% respectively.

For $V_{dc} = 1$ V and $I_{max} = 2$ A;

TABLE 2
PERFORMANCE PARAMETERS

	$P_{dc}(W)$	$P_{out}(W)$	$PUF(dB)$	$V_{max}(V)$	$\eta_{Drain}(\%)$
ClassB	$2/\pi$	$1/2$	0	2	78.5
IPA^{2nd} 100%	$\frac{2}{\pi}+\frac{2}{6\pi}$	$1/\sqrt{2}$	1.5	2.9	95.2
IPA^{2nd} 50%	$\frac{2}{\pi}+\frac{4}{6\pi}$	$1/\sqrt{2}$	1.5	2.9	83.3

The results show that even when the second harmonic power is fully accounted for and with realistic efficiency values for the second harmonic power generator that the active injection second harmonic Power Amplifier (IPA) has the potential to provide for efficiencies over 80%. The bandwidth advantage expected is inherently associated with such mode of operation since the fundamental matching can be broadband covering multiple octaves and harmonic impedances can be actively adjusted using broadband PAs such as multi octave class-A PA design. Moreover, the expected power of IPA will be around 50% enhanced relative to class-B equivalent.

III. TRANSISTOR VALIDATION

To validate these theoretical results experimental transistor investigations were undertaken using the previously developed waveform measurement and engineering system at Cardiff University. Since these measurements system utilized active harmonic load-pull they can provide the negative impedances necessary to experimentally demonstrate the IPA mode of operation on the selected 10W packaged GaN device. For the appropriate comparison with theory the V/I waveforms at the current generator plane of the packaged device are required, hence a package parasitic de-embedding process [4] was used.

A. *Measurement and Results*

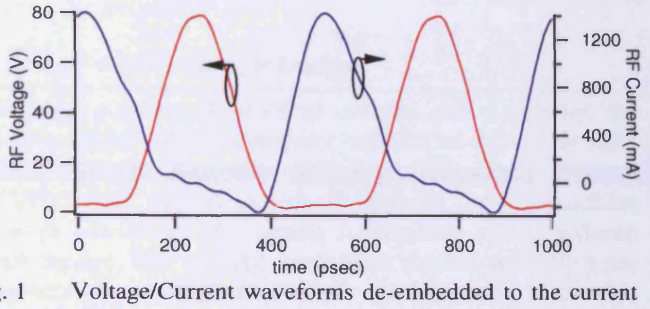

Fig. 1 Voltage/Current waveforms de-embedded to the current generator plane

In order to achieve the required half rectified class-B current waveform the 10 W GaN device was biased around pinch-off at a 28V drain voltage. The active load pull measurement started from inverted class-F optimum fundamental loading condition [5]. The active second harmonic loop was then used to inject energy at the second harmonic to appropriately shape the voltage waveform; targeting a band-limited half rectified waveform offset by 180 from the current waveform. The measured V/I waveforms achieved at the current generator plane are shown in Fig.1. It clearly demonstrates that transistor can support this mode of operation. The required optimum load reflection coefficient of the second harmonic measured is 4 with a phase of 178° relative to the fundamental load reflection coefficient.

The dynamic RF load line for this IPA mode is shown in Fig. 2 and is compared to that achieved for class-B operation; passive harmonic injection into the same fundamental load at the same drive level. In the Class-B case the transistor is clearly overdriven in contrast to the IPA mode. In the IPA the active injected second harmonic voltage component allowing the fundamental voltage component to be increased without forcing the current into a clipping regime and consequently as theoretically predicted both the RF output power and efficiency increases.

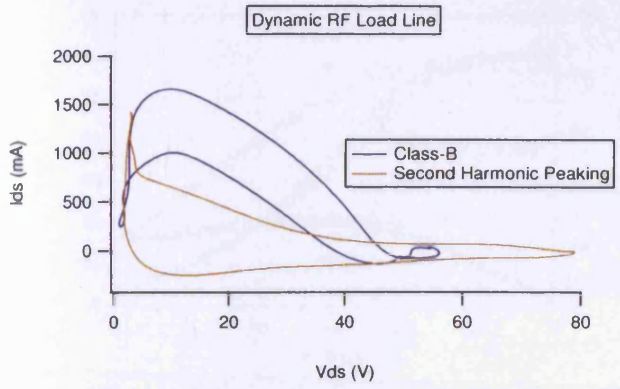

Fig. 2 RF load line of class-B and IPA de-embedded to the current generator plane

B. *Discussion*

The measured efficiency, taking into account the RF energy injected at the second harmonic is 92%. This is very close to that predicted theoretically which is 95.2% (correspond to that predicted for a 100% efficient second harmonic generator). The reduction of efficiency can be associated with the knee effect which will limit the minimum voltage value. Considering knee effect in drain efficiency calculation predicts an efficiency of 90.4%:

$$\eta_{IPA\ Drain} = P_{RF} / (P_{dc}(1 + V_k/V_{dc}) + (P_{dco}/\eta_0)) \quad (9)$$

$$= 90.4\%$$

where $V_k = 1.74$ V is the measured minimum voltage value. The measured efficiency is slightly higher than the theoretical value and possibly this is the advantageous effect of the higher harmonic voltage components produced by the system impedance.

Also as theoretically predicted the measured output power in this IPA mode has increased by 2 dB. This is in part due to the injected second harmonic power contributing around 1 dB of the change. This outcome highlights an alternative interpretation of how this amplifier works. The resulting waveform shaping allow for the conversion of RF power injected at the second harmonic to a RF power at the fundamental frequency [6]. These results show that significant advantages can be gained from second harmonic injection in terms of efficiency, power and possibly bandwidth.

IV. PA Demonstrator

A. *Proposed Topology*

The proposed Injection Power Amplifier (IPA) consists of two paths where the upper one (Fig. 3) generates the main fundamental radio frequency (RF) signal and a lower path with a voltage source/auxiliary PA to control the V/I waveforms of the main PA by injecting the even harmonics of the fundamental signal, resulting in the V/I waveforms being shaped for better PA performance in terms of power, efficiency and bandwidth. The baseband information (BB) are up converted by Local Oscillator (LO) through this constant LO power and the fundamental signal is up converted to second harmonic by a doubler. This solution of generating the second harmonic is just a suggestion and could be realised by other circuit topologies.

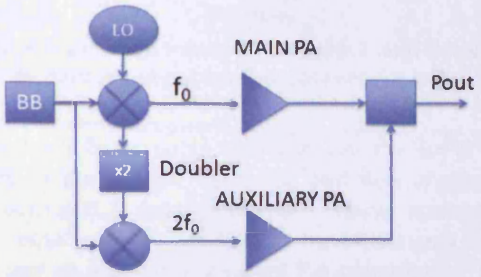

Fig. 3 Proposed topology

B. *PA Demonstrator Design*

For the purpose of proof of concept and simplicity, the actual realized PA demonstrator consists of two 10 W GaN HEMT (High Electron Mobility Transistor) devices (CGH40010F) biased at class-B and an output matching network consisting of a simple multiplexer and impedance transformers. The devices have been chosen since they are commercially available; nonlinear model exist and provide relatively high output power levels. The board used is a high frequency laminate board (TMM3) from Rogers Corporation. Input drive is achieved using two ESGs (Electronic Signal Generators); hence one is used to generate the second harmonic signal instead of a doubler and thus feeds the auxiliary PA directly.

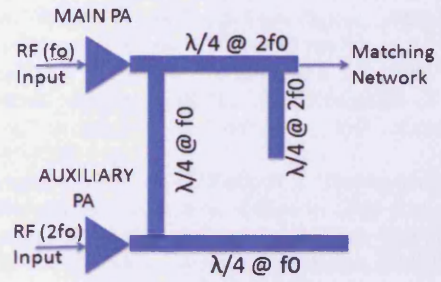

Fig. 4 Multiplexer

The design starts with a multiplexer (Fig.4) where the main PA fundamental signal sees only constant load while the auxiliary PA, active second harmonic injection, sees only the main PA. Therefore, the RF fundamental signal finds its way to the load and the auxiliary PA performs the required waveform shaping.

The output matching network was designed for optimum performance according to load pull measurement while the auxiliary PA's matching network was designed based on ADS simulation for maximum efficiency. Next, an optimization process in ADS has been used and the simulated results showing a drain efficiency of around 75 % at P1dB.

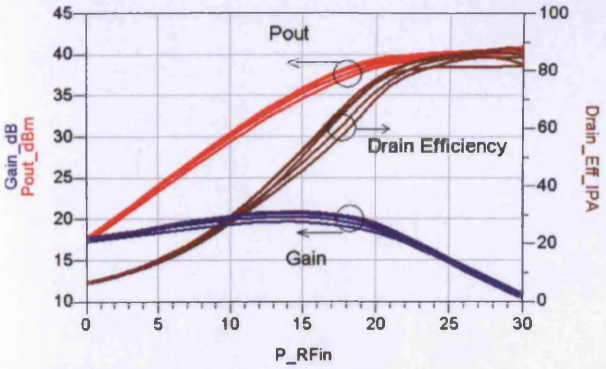

Fig. 5 IPA Simulation results for an increasing phase offset between the two input signals

It is believed that with further investigations/optimization that this value can be further increased using an optimised drive strategy as can be seen in Fig.5. However, it was felt that this design performance was sufficient to demonstrate the potential of the IPA mode of operation, hence demonstrate the feasibility of using this concept in PA design for high efficiency wide band applications. Moreover, this topology has interesting drain efficiency behaviour. It does not decrease but continues to increase as the PA is driven hard into saturation, a result that can be utilized in some applications. The predicted efficiency is 88% at 11W.

C. *Realized PA Demonstrator*

The demonstrator PA (Fig.6) has successfully fabricated and characterized. It achieved the expected efficiency at P1dB with IPA drain efficiency of 74.3 % at 900 MHz for a yet not optimised drive strategy. The highest drain efficiency was 85.7% at the saturated output power of 10W. (Fig.7)

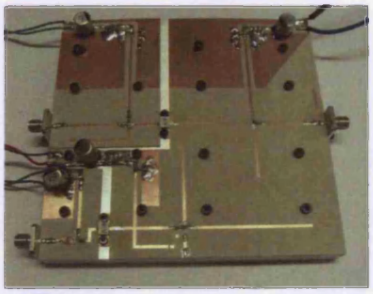

Fig. 6 Realized IPA

V. Conclusion

A novel approach for wide band high efficiency high power amplifier has been introduced. The approach is based on the concept of using active second harmonic injection to wave shape the transistor output V/I waveforms. Theoretical analysis indicated that this concept is capable of delivering very high, >95%, efficiencies.

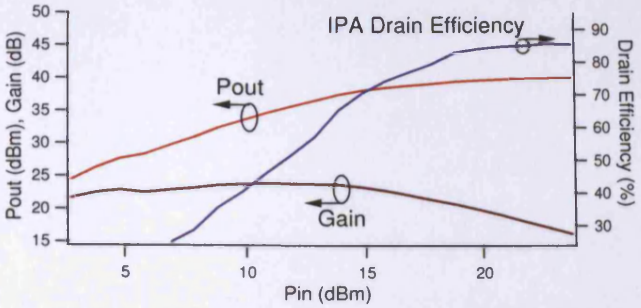

Fig. 7 IPA measurement results for a constant (and hence not yet optimized) magnitude and phase offset between the two drive signals.

This analysis fully takes into account the input energy component at the second harmonic and was confirmed by initial experimental measurements. These measurements involved both active load-pull measurements on the transistor and on a proof of concept PA structure.

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