Doherty Amplifier Structures for Modern Microwave Communication Systems

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Doctor of Philosophy

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SUMMARY

The Power Amplifier (PA) is a critical component in any mobile communications system with performance that is very sensitive to RF envelope dynamics. Achieving the required linearity demanded by evolving communications systems invariably involves increasing PA complexity at the cost of reducing PA efficiency; the consequences of which are severe and include for example reduced operational time for portable communications devices and perhaps less obviously the significant running, capital and thermal management costs associated with mobile communication system base-stations. The Doherty PA is one of a number of elegant architectures that have been developed to address this problem, and although conceived and patented in the 1930's, has only recently become established as a means of enhancing efficiency in microwave PA applications.

The Doherty is renowned for its elegant simplicity; however, the realisation of functional Doherty PAs using modern microwave devices is problematical and hindered by many hidden complexities, which are in general brought about by the complex, 'load-pulling' action of two active devices that conspire to cause a variety of performance related problems. Although harmonic behaviour is important, understanding device interaction at a fundamental level has been found to be the critical factor in achieving good overall Doherty performance.

With this in mind, this thesis concentrates initially on developing an extensive understanding of fundamental device interaction through the use of a novel Doherty measurement approach which involves replacing the classical Doherty's symmetrical input power division arrangement with independent, phase-coherent excitations. The resulting insight has meant that it has been possible to introduce more focused measurement techniques including harmonic analysis and waveform engineering in order to further explore individual device behaviour. The extensive use of harmonic load-pull measurement systems and the direct synthesis of the impedance environments that exist within the Doherty have allowed a number of device technologies to be considered within the application environment resulting in the realisation of GaAs and GaN Doherty prototypes.

As a direct result of this analysis, a number of optimisation approaches have been identified that involve the dynamic adjustment of relative input magnitude, relative input phase and relative device bias, which has in turn exposed the various design trade-offs that exist between linearity and efficiency within the Doherty.

Other work includes the development of modulated measurement systems and specialised excitations that allow the meaningful comparison between measured single-tone and modulated performance, as well as allowing more comprehensive investigations into Doherty linearity under varying IF impedance conditions.

LIST OF PUBLICATIONS

1. **J. Lees**, A. Sheikh, J. Benedikt and P. J. Tasker, "The Design of a GaN Doherty Amplifier Using Waveform Measurements and Active Harmonic Load-Pull", **INMMiC-2006**, Aveiro, Portugal, **2006**

   Abstract - The Doherty Power Amplifier (PA) architecture is rapidly gaining popularity in the mobile communications system application domain. Its principle of operation relies upon the intentional interaction between two transistors, and in order to obtain optimum performance the large signal characteristics of both devices need to be considered. This poses a significant challenge as firstly, the current non-linear models available within CAD-based design environments generally lack the required accuracy, and secondly the established trial-and-error based design approaches are less effective and tend to be impractical for complex, multiple device PA structures. This paper describes how active harmonic load-pull systems and the direct measurement of voltage and current time-domain waveforms can be directly utilised in the design and optimisation of a GaN Doherty PA. As part of this process a large signal measurement system is employed to synthesise the precise dynamic impedance environment that would need to exist around a single, '*main*' 1mm GaN device within a prototype Doherty structure.

2. **J. Lees**, J. Benedikt, K. P. Hilton, J. Powell, R. S. Balmer, M. J. Uren, Martin, and P. J. Tasker, " An Experimental Gallium Nitride Microwave Doherty Amplifier," **IEE Electronics Letters**, September **2005**.

   Abstract — A 1.8 GHz, 1.8 Watt Gallium Nitride (GaN) Doherty Power Amplifier (PA) is presented demonstrating that GaN devices can be highly effective when used within the efficiency enhancing Doherty PA architecture. A power density of circa 1 W/mm is demonstrated with linearity that remains comparable to that observed in other GaAs Doherty architectures.

3. **J. Lees**, J. Benedikt, K. P. Hilton, J. Powell, R. S. Balmer, M. J. Uren, T. Martin, and P. J. Tasker, "Characterisation of an Experimental Gallium Nitride Microwave Doherty Amplifier," **EuMC**, Paris, **2005**.

   Abstract — The efficiency of microwave power amplifiers is highly dependent upon both amplifier architecture and the active device technology employed. This paper presents for the first time the combination of Gallium Nitride (GaN) device technology with the now well established efficiency enhancing Doherty Power Amplifier (PA) architecture. The amplifier is characterised at 1.8 GHz using both single-tone and modulated excitation through the use of a purpose built multi-port, multi-stimulus measurement system. Initial measurements are very positive and show how GaN devices can be highly effective within the Doherty amplifier, even with the limitations of the simple experimental structure used. Measurements show that efficiency is successfully extended over 6dB of dynamic range, and a power density of 0.9W/mm is demonstrated, while linearity remains comparable to that observed for a GaAs Doherty.

4. **J. Lees**, A. Haczewski, J. Benedikt, and P. J. Tasker, "An Automated Multiple-Stimulus Measurement System for Characterising Multiple-Device Amplifiers," **EuMC, 2004**.

   Abstract — A novel, fully automated, fully calibrated multiple-stimulus measurement system has been developed for the extensive characterisation of complex amplifier structures under single-tone and modulated signal excitation. Achieving precise relative phase and magnitude control of the independent RF, base-band and bias signals allows analysis and measurement of otherwise hidden device interaction. Use of the measurement system in characterising multiple-device amplifier behaviour has led directly to a novel optimisation approach, allowing the efficiency and linearity to be

maximised. In order to control the base-band impedance environment, a fully calibrated IF-load-pull capability has been incorporated, allowing investigations into amplifier sensitivity to memory effects, specifically those associated with base-band impedance termination.The features of this system are demonstrated through its application in characterising a dual input Doherty structure. By varying a number of independent parameters including relative RF input phase, relative RF input power and bias, behaviour has been uncovered that has led to improved insight and understanding of the Doherty structure. It has been shown for example that device specific bias dependent S21-phase behaviour can significantly degrade expected performance of an adaptive-bias Doherty amplifier.

5. **J. Lees**, J. Benedikt, M. Goss, and P. J. Tasker, "Measurement Based Optimisation of an Adaptive-bias Doherty Structure," **IEEE MTT-S** International Microwave Symposium, **2003**.

Abstract — The Doherty PA configuration has become well established as a means of enhancing PA efficiency. The improvement however is usually accompanied by deterioration in overall linearity. This paper addresses two important features of the Doherty PA configuration, which offer a means of improving the linearity / efficiency trade-off obtained using a classical adaptive-bias implementation. One issue is the need to generate a suitable bias control voltage for the *auxiliary* PA device. Such control enables the use of two devices with equal periphery for *main* and *auxiliary* functions. The second issue is the use of phase compensation to ensure the combined signals sum in the correct manner prescribed by classical analysis. Both of these refinements are demonstrated using an experimental circuit operating at 1.8 GHz. Extensive experimental data is presented on the beneficial effects of phase control which show that a better compromise between optimum efficiency and linearity can be obtained using different phase offsets at different drive levels. This raises the interesting possibility of adjusting relative phase, bias and relative input magnitude dynamically in order to obtain improved linearity from the Doherty configuration, especially for signals having high peak to average ratios.

6. **J. Lees**, J. Benedikt, B. Bunz, C. Gaquiere, D. Ducatteau, A. Marquez-Segura, T. M. Martin-Guerrero, and A. Barel, "Comparison of Load-Pull Measurement Results of a 4W pHEMT Involving Five European Laboratories," **EuMC** Paris, **2005**.

Abstract — Load and source pull measurement data has for some time now been a critical and integral part of the power amplifier design process, offering accurate performance data of the actual device that is to be used. This data can be used directly to generate graphical representations of key parameters such as output power, efficiency and gain as functions of source and load impedance, for model verification or perhaps more interestingly as the basis of a model itself. There are a number of excellent research groups across Europe looking into these interesting areas, however until recently, collaboration and dissemination of information has been limited. TARGET, as a network of excellence has provided a close working relationship between these groups where for the first time these key capabilities have been compared and contrasted.

7. Z. Aboush, C. Jones, G. Knight, A. Sheik, H. Lee, **J. Lees**, J. Benedikt and P. J. Tasker, "High Power Active Harmonic Load-Pull System for Characterization of High Power 100Watt Transistors", **IEEE MTT-S** International Microwave Symposium, **2005.**

Abstract — This paper presents, for the first time, a waveform/time-domain measurement system with active harmonic load pull that is capable of characterising 100W LDMOS devices. In order to achieve the required high-power capability the measurement system employs a new bias-tee design [1] coupled with broadband impedance transformers [2]. The unique characteristics of the high-power bias-tee increases the performance of the measurement system up to 12GHz, 100W CW for the RF channel, and 100V, 10A for the DC channel. The broadband impedance transformers are embedded within the time-domain measurement system and dramatically reduce the power levels required from the active load-pull system for device characterization. This system is demonstrated through the successful characterisation of a 100W LDMOS device, where only 120W of active load-pull power is required to emulate the low impedance optimum load. This represents a remarkable reduction in required power from the impractically high 688W needed in a conventional system with no impedance transformation.

8. Z. Aboush, C. Jones, G. Knight, A. Sheikh, H. Lee, **J. Lees**, J. Benedikt, and P. J. Tasker, "High Power Active Harmonic Load-Pull System for Characterization of High Power 100Watt Transistors", **EuMC**, Paris, **2005**.

Abstract — High-power devices (>30W) require low load impedances (<5W) for optimum power performance. In presenting the necessary fundamental and harmonicimpedances, traditional passive load-pull systems are restricted by inherent system losses. Active load-pull can compensate for this problem, but unfortunately does not scale well with high power applications. This paper presents a novel solution allowing harmonic load-pull characterization of high-power devices. Broadband impedance transformers allow the necessary load-pull power to be dramatically reduced whilst maintaining the accuracy and integrity of measured waveforms. This approach has been successfully demonstrated through the measurement of a 30W LDMOS device, where the required active load-pull power required to present the optimum load has been reduced from 270W to 50W.

Chapter 1 Introduction

1.1 Research perspective

According to recent estimates[1] the mobile telephony industry contributed £22.0 billion to UK Gross Domestic Product (GDP) in 2003. This represents 2.2% of the UK's total economic output and to further place the significance of the industry into perspective, is equivalent to the combined contribution of the UK's oil and gas extraction industries. Furthermore, in terms of employment the mobile telephony sector directly supported over 170,000 jobs in 2003 which represents 0.6% of total UK employment in the same period. These statistics clearly illustrate both the importance of the industry as well as the public's insatiable appetite for both voice and data based mobile communications. As well as talking, users equipped with portable computers and a growing array of mobile devices incorporating wireless communication technologies increasingly need to connect to corporate networks, exchange messages, access the internet and transfer multi-media data files. The evolving nature of these complex applications continues to impose significant system-wide challenges on modern communication systems. The general desire for improved spectral efficiency coupled with a continual, and increasing demand in data throughput has resulted in the deployment of a variety of complex multi-carrier modulation schemes employing a combination of both phase and amplitude modulation with RF envelopes possessing significant peak-average power ratios.

1.2 The advent of mobile communications

James Clerk Maxwell was responsible for the first colour photograph, defined the nature of gases and with a few mathematical equations exposed the fundamental relationship between electricity and magnetism. Between 1864 and 1873, he worked on extending Michael Faraday's theories of electricity and magnetic lines of force and demonstrated how an oscillating electric charge produces an electromagnetic field.
Between 1885 and 1889 Heinrich Hertz clarified and expanded Maxwell's electromagnetic theory of light, proving that energy can be transmitted as electromagnetic waves, which travel at the speed of light and which possess many other properties of light. It wasn't until some years later in 1895 that Guglielmo Marconi first transmitted radio signals any significant distance. Unable to interest the Italian government in his invention, Marconi took his crude transmitter and receiver to

1 Report commissioned by O_2 In May 2004 http://www.gsmworld.com/documents/cebr.pdf

England, where the British navy quickly realized the maritime potential of radio: within two years, the Marconi Wireless Telegraph Company had been founded, and the era of radio communications was born.

1.3 The Power Amplifier

This Thesis is concerned with a single yet critical part of any mobile telecommunication system - the Power Amplifier (PA). In its simplest form, the PA is a device that, in response to an input stimulus converts DC energy into a required amount of RF energy suitable for transmission. The PA architecture used to achieve this amplification depends upon a number of application specific factors, the most significant of which being the required efficiency, the required linearity and ultimately the cost.

A PA for a satellite application for example will need to be highly efficient due to the obvious on-board power limitations. This is in contrast to a mobile handset PA where although linearity and efficiency are increasingly significant design drivers, cost remains an extremely important consideration due to the highly competitive nature of the mobile telephony market.

The very first PAs were generally spark-gap [1], arc [2] or alternator [3] type transmitters working in the LF to MF bands and were capable of generating many kW of RF power. It wasn't until 1907 however and the appearance of the thermo-ionic vacuum tube or '*valve*' that the means to both generate and critically, control RF power electronically became available. Valve transmitters were dominant for many years up to the 1970's, and were typified by their high voltage supply requirements resulting in conveniently high optimum load impedances.

Discrete solid-state RF power devices started to appear in the 1960's with the introduction of the silicon bi-polar transistor. In contrast to their valve counterparts, these devices operated at low supply voltages, higher currents and consequentially lower load impedances. It wasn't until the late 1970s however and specifically, the appearance of the GaAs MESFET that transistors started to be used in large numbers in microwave applications. The following years witnessed a steady progression in the development of solid state microwave device technology and associated applications. New devices included HEMT's, pHEMTs, HFETs, HBTs and alike, whilst the materials from which these devices were fabricated became increasingly exotic and included GaAs, SiC, InP, InGaP and GaN.

1.4 The evolution of modulation schemes and associated problems

Before the early 1940's and the earlier publication of Edwin Armstrong's definitive paper [4] introducing the concepts of Frequency Modulation (FM), Amplitude Modulation (AM) was the only practical and reliable way to convey information using radio transmission. During this time, the very large scale power amplification of modulated RF carriers with significant peak to average power ratios resulted in extremely high running costs due to poor linear PA efficiency. The cost incentives of improving efficiency applied particularly to commercial radio stations that were in the business of generating typically many hundreds of kW of RF power; and it is no surprise that there was significant motivation in developing efficient, large scale PAs that were capable of accurately amplifying the amplitude modulated RF signals of the day. This era resulted in a number of rather elegant PA designs that directly addressed the problem of linear efficient power amplification, one of which was the Doherty PA, the analysis of which forms the basis of this research.

Problems associated with AM transmission resulted in significant commercial and defence related motivation and resultant development into other, more accurate, increased bandwidth modulation techniques with improved noise immunity. The appearance for instance of accurate frequency and phase discrimination techniques allowed the use of constant amplitude envelope modulation schemes that could convey information using deviations in phase or frequency. This development and the adoption of CW modulation schemes such as FM, PSK and GMSK had significant implications for the PA as constant envelope modulation techniques immediately removed the problematical amplitude variation that led directly to poor PA efficiency. This in turn meant that the emphasis of PA design shifted from the accurate amplification and reproduction of magnitude variation towards the accurate amplification and reproduction of frequency and phase variation. The PA efficiency problem was therefore considerably eased with the extensive use of sometimes very high efficiency, reduced conduction angle PA architectures using classes of biasing including C, D, E and F.

Due to the massive worldwide growth of mobile communications systems over recent years, and the unyielding need for ever more spectral efficiency in increasingly crowded radio spectrums, complex modulation schemes have evolved that employ both phase and amplitude modulation in order to convey the increasing amounts of voice and data information. Modern modulation schemes include Quadrature Phase

Shift Keying (QPSK) and Quadrature Amplitude Modulation (QAM), and are all typically generated through vector or I-Q sub-carrier modulation. The latter of these schemes result in modulated carriers with simultaneous amplitude and phase variation typified by peak to average power ratios ranging typically between 3 and 6 dB [5].

In a typical, modern, mobile telecommunication system, many such signals will need to be amplified and transmitted simultaneously. For example, in the multi-carrier environment of a mobile base-station, the combination and hence summation and cancellation of amplitude and phase modulated carriers inevitably means that the resulting, composite carrier will possess a much higher degree of amplitude variation, and will be characterised by peak to average power ratios of anything between 8 and 13 dB [5].

Other emerging, high spectral efficiency modulation schemes such as Orthogonal Frequency Division Multiplexing (OFDM) [6] rely on the simultaneous use of large numbers of carriers to effectively distribute the modulated information over a wide bandwidth. This is a powerful technique that is effective in solving a number of specific problems including simplification of hardware[2] and multi-path mitigation. The resulting modulation envelopes of such schemes cause an even greater problem for the microwave PA due to significant amplitude variations in the transmitted carrier.

These developments in modulation schemes, along with the fact that many modern, battery reliant mobile devices such as mobile telephone handsets, PDA's and laptop computers need to transmit voice and data information have meant that, as was the case in the 1930s, efficiency as well as linearity is once again a primary PA design concern.

1.5 Linearity and the PA

PA linearity is essentially a measure of the accuracy of the amplification process or more specifically the fidelity with which the PA can amplify both the phase and amplitude of an input stimulus. PA *non*-linearity is conversely any process or mechanism that introduces distortion into these quantities and can generally be considered as belonging to one of three distinct groups; phase or AM-PM conversion, amplitude or AM-AM distortion, and memory effects.

Although memory effects are not themselves considered as classical PA non-linearities, they are certainly non-linear processes that can significantly complicate the 'anticipated' or 'memory-less' non-linear system behaviour by introducing time-

[2] This is in relation to a conventional FDM approach, where arrays of sinusoidal waveform generators and coherent demodulators are replaced with an FFT approach which is nowadays easily realisable.

dependency into the 'normal' AM-AM and AM-PM characteristics of the PA. These effects are highly complex and are attributable to a number of factors including electrical properties such as time-varying envelope impedances, thermal properties such as the electro-thermal couplings between a device its package and the heat-sink; and finally device physics related properties such as charge storage or 'trapping' effects.

PA non-linearity has traditionally been characterised by measuring the Carrier to Interference (C/I) ratio and specifically the relative magnitude of the third-order inter-modulation products in comparison to the carrier magnitude. Typically, a linear PA will be expected to have a C/I ratio of no more than 30 dB at Peak Envelope Power (PEP).

In modern communications systems however, linearity tends to be measured in terms of Error Vector Magnitude (EVM) and Adjacent Channel Power Ratio (ACPR) which describe the accuracy of the detection process and how non-linearity impacts adjacent channels respectively. This shift in approach is not only due to improvements in measurement techniques, but can also be considered indicative of the fact that over the last 5 to 10 years, PA design has increasingly been driven by rigid linearity requirements and the ability of a PA to accurately amplify the phase and magnitude of a modulated carrier, as well as minimising spectral re-growth in adjacent channels. Figure 1 and Figure 2 illustrate the rigidity of the spectral requirements through a 3G-UMTS spectral mask, and an example of a linearised Doherty PA measurement respectively.

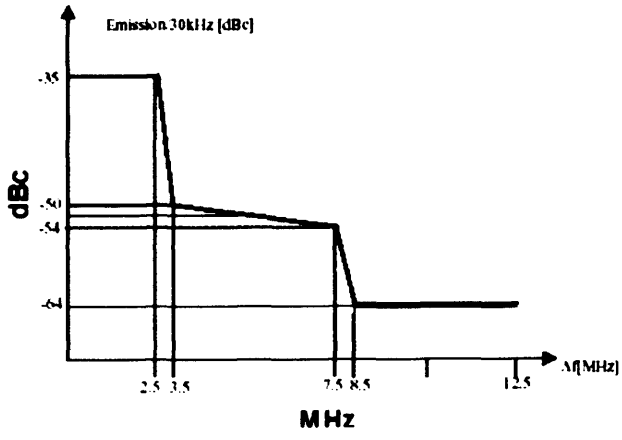


Figure 1 3G–UMTS Mobile Station spectrum mask [7]

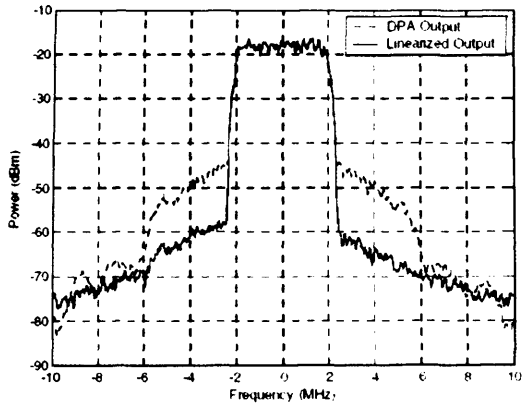


Figure 2 –spectrum of a Doherty PA before and following linearisation [8]

Attaining required PA linearity has classically been achieved through use of class-A or class-AB bias, and 'backing-off' the PA such that the applied modulated excitation stimulates only the most linear parts of the device trans-conductance characteristic: in other words, the linear dynamic range of the PA must encompasses the dynamic range of the modulation. When this is the case, maximum linear power and hence maximum linear efficiency will only occur infrequently with the peaks of maximum modulation.

This simple approach can involve backing-off the PA by anything between 10 and 20 dB and involves operating devices well within their peak capability for the vast majority of time. Although highly effective in improving linearity, this tends to be impractical for many commercial PA applications due to efficiency and PUF penalties, and other more complex approaches are generally employed including feed-forward, feed-back and digital pre-distortion linearisation techniques.

1.6 Efficiency and the PA

It is evident that with so much recent PA development effort being directed towards meeting increasingly stringent linearity requirements, efficient-linear PAs have had to take something of a 'back seat' in terms of research effort. In the last few years however, both academia and industry have realised that the traditional trade-offs used in achieving required PA linearity at the expense of efficiency is an increasingly unacceptable solution. In the telecommunications industry, this is the case for PA's embedded within both handsets and base-station applications for different reasons: primarily reduced battery-life and hence talk-time, and increased running and capital costs respectively.

As has been mentioned, the rather major consequence of adopting the traditional PA 'back-off' approach is that PA efficiency degrades rapidly with increasing PAR of the modulation envelope. This renders linear PA's designed using this approach hopelessly inefficient when used to amplify modulation envelopes with significant amplitude variation.

Consider for example the amplification of a multi-carrier signal with a 10 dB peak-to-average power ratio using ideal class-A and class-B PAs. These ideal amplifiers have corresponding PEP efficiencies of 50% and 78.5% and yet when faced with amplifying this particular modulation, will have average efficiencies of only 5% and 28% respectively [5].

As shown in Figure 5, PAR is a very useful and intuitive measure in describing modulation envelope dynamics, but is sometimes a little too general when

considering various complex, 'continuous' modulation schemes alongside unorthodox PA efficiency characteristics, such is the case with the Doherty and other efficiency enhancing PA architectures. A more comprehensive approach involves the statistical analysis of modulation dynamics and generation of Probability Density Function (PDF) or Cumulative Density Function (CDF) profiles that describe the statistical likelihood that a modulation envelope will possess a given amplitude, and the likelihood a modulation envelope amplitude is to exceed a single, specific amplitude, respectively. These measures are extremely useful as they can be integrated directly with PA efficiency characteristics in order to obtain a very accurate estimation of efficiency for any non-constant amplitude modulation.

This is an important feature as it allows for example a PA's efficiency characteristic to be engineered and optimised to suit the dynamics of a particular modulation. This is certainly the case with the Classical Doherty PA architecture which has two distinct efficiency peaks, the relative position of which can be manipulated through design [9].

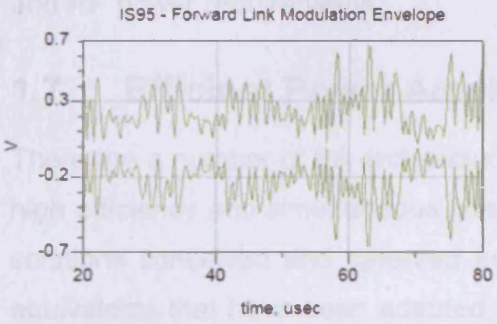


Figure 3 – multi-carrier envelope (upper and lower shown)[3]

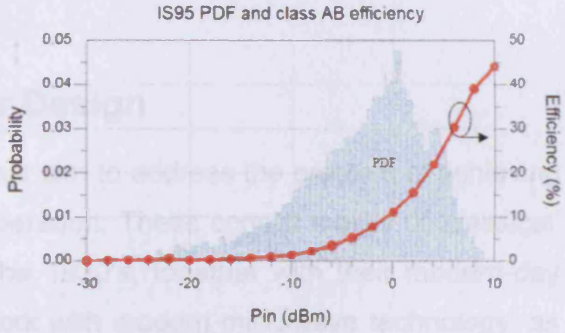


Figure 4 – multi-carrier CDMA PDF with example class-AB efficiency characteristic

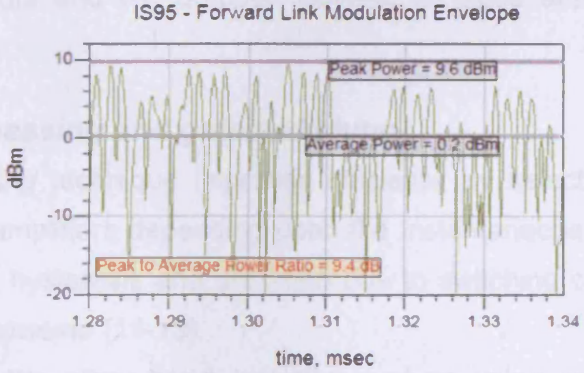


Figure 5 – instantaneous envelope power as a function of time with identified average and peak power, and PAR

Figure 4 shows the PDF of the IS95-CDMA[3] modulation envelope shown in Figure 3 and Figure 5, overlaid with the simulated efficiency characteristic of a realistic class-AB PA. From these two measures, it is clear that in this particular example, the modulation spends most of its time around 0 dBm, where the corresponding PA efficiency is approximately 10%.

To further place the importance of PA efficiency into perspective, it is constructive to consider the impact of poor efficiency from a commercial perspective. For example, consider the running and capital cost saving potential for a large network with many base-stations. It is shown in [10] for example that across a complete network of approximately 10,000 base-stations (based on a major EU country and the DCS1800 system), an annual power saving of approximately £10M can be achieved through the use of improved efficiency linearised multi-carrier PAs alone. Less obvious advantages of more efficient PA's include the possibility of locating cooler, smaller PA's in mast-head locations, close to antennas, thus reducing cable costs, cable loss and RF power requirements.

1.7 Efficient Power Amplifier Design

There are a number of PA architectures that aim to address the problem of achieving high efficiency and simultaneous linear operation. These consist mostly of 'classical' solutions conceived and patented from the 1930's, together with their modern-day equivalents that have been adapted to work with modern microwave technology, as well as modern digital control techniques. All of these techniques however fall into two categories: those that can be described as true, *'RF-in / RF-out'* PAs, and those that are more accurately described as transmitter architectures possessing base-band or digital inputs and RF outputs. Several of these approaches are briefly discussed below.

1.7.1 Stage by-passing and gate switching

The *stage by-passing* technique improves efficiency by selecting or 'switching-in' different periphery amplifiers depending upon the instantaneous signal level applied to the PA. Avoiding hysteresis and distortion due to switching can be problematical with this approach however [11-13].

Gate switching on the other hand typically involves using multiple devices with different periphery connected in parallel. These devices are biased such that only a

3 The IS-95 modulation shown is based on a simulation using 9 channels, including pilot, synch, paging, and 6 traffic channels that used Walsh codes 34-39.

single device is active for the low power requirements, with the other devices becoming active as and when needed. This approach benefits from reduced losses due to the absence of RF switching, however as the devices are directly coupled, does suffer from dynamic variations in load and source impedance over dynamic range.

1.7.2 The Khan technique

The Khan Envelope Elimination and Restoration (EER) technique describes an RF transmitter rather than a true PA architecture. The approach employs a highly efficient, non-linear RF PA together with another highly efficient low frequency envelope amplifier. In its classical form, a limiting amplifier is used to 'strip-off' the modulation and pass only the constant amplitude, phase-modulated carrier to the non-linear PA. The original envelope is then regenerated through the action of the envelope amplifier, which derives its input from the original modulation.
Using this technique, efficiencies have been demonstrate that are three to five times that of a conventional linear PA [14].

1.7.3 Class-S modulation

This approach relies upon the principles of Pulse Width Modulation (PWM) and typically employs a high power device together with a diode and low-pass filter network in order to generate the required modulated envelope [11]. This type of PA is ideally 100% efficient, has a potentially large bandwidth, and is attractive for its ability to be directly controlled through digital techniques and DSP.

1.7.4 Envelope tracking

This is a similar technique to that of Khan and EER. The difference lies in the fact that the Khan technique uses a highly efficient yet non-linear RF PA, where Envelope Tracking (ET) employs a modulator, usually in the form of a DC to DC converter, to modify the supply voltage delivered to a linear PA in response to the instantaneous amplitude of the applied RF envelope. In principle, accurate tracking of the modulation envelope by the supply voltage allows high efficiency to be achieved for all output amplitudes. ET systems employing modulators with switching frequencies up to 20 MHz have been implemented using a variety of different device technologies [15-18].

1.8 Active load-pull within PA structures

Unlike all of the techniques described above, there are a number of unique PA architectures that exploit the useful device interaction that occurs when one active device is allowed to influence the load presented to another. The Chireix and the Doherty are two such PA architectures, and are briefly discussed below.

1.8.1 The Chireix technique

In typical outphasing applications, which now tends to be termed LInear amplification using Non-linear Components (LiNC), the output modulation envelope is synthesised from the combination of two, constant amplitude, phase modulated carrier signals possessing very precise and specific relative phase. Typically, a hybrid combiner is used to sum these signals such that the outputs of the active devices are isolated from the highly reactive loads that would exist if the device output's were directly connected. [19]. The efficiency of such hybrid-coupled outphasing PAs varies with output power, and as both devices are always operating at maximum drive, will be inversely proportional to the Peak-to-Average power Ratio (PAR) of the modulation [11]. Although it is possible to recover some of the wasted power from the 'dump' port of the hybrid combiner used, this process is complex and tends to be problematical [20].

In the Chireix outphasing technique, the outputs of the active devices are directly coupled via a simple transformer and intentionally allowed to influence and actively load-pull each other. The inclusion of compensating shunt reactive components at the output of each device has the effect of resonating out the highly reactive loads that each device experiences as a result of the active load-pull, at a specific point in the dynamic range, thus maximising the efficiency at that point. Through careful selection of component values, a high efficiency plateau can be engineered that exists over typically 6dB of dynamic range.

The Chireix technique, without question, can be highly effective in enhancing PA efficiency. It is however a transmitter structure consisting of both a RF synthesis and RF combination elements. One disadvantage of this structure lies in the fact that it is difficult to synthesise two precisely phased, constant amplitude phase modulated carrier signals. Having said this, developments in modern digital techniques and accessibility to powerful DSP continues to ease this problem.

1.8.2 The Doherty technique

The Doherty is another structure that employs intentional device interaction and the concept of active load-pull in order to enhance efficiency. Unlike the Chireix however,

the Doherty can be described as a true RF-in, RF-out PA architecture, and in its classical form can be realised incredibly simply using two active devices along with a simple impedance transforming network.

This extraordinary simplicity coupled with the fact that the Doherty is potentially a linear structure offering high efficiency over typically 6dB of dynamic range has meant that the Doherty has been the subject of much recent research and commercial interest, and as a consequence is now the architecture of choice in many base-station PA assemblies.

1.9 Research Motivation

Although the Doherty is now a well-researched and well funded area of microwave PA design, there are still many aspects of the Doherty PA architecture that remain over-simplified and unexplored. This was especially true at the outset of this research, when for example there were no commercial realisations of microwave Doherty PA's, and very few publications that demonstrated clear and convincing measured Doherty behaviour. It became clear for instance that it was relatively easy to assemble a classical Doherty PA and achieve some degree of enhanced efficiency. It was felt however that such realisations although offering some benefit, could offer much improved performance through optimisation.

The overriding motivation behind this research was to investigate the Doherty structure in more detail, identify sensitivities, and to formulate an optimal design approach that if possible, was technology independent.

It was felt that due to the existing capabilities in terms of harmonic load-pull and waveform measurement systems at Cardiff University, the research group was ideally placed to develop this approach and conduct detailed research into the Doherty PA structure.

1.10 Research Objectives

The commercial motivation behind this research was strong, and the *main* objectives of the industrial supporting partner was to learn as much as possible regarding the Doherty PA solution, ideally using LDMOS technology, and to understand how the Doherty PA might be implemented and ultimately optimised. Such information was simply absent in commercial PA design, with working solutions being based upon practical engineering and the traditional iterative design process. It was clear that industry was lacking a deeper insight into Doherty PA and needed to understand ways in which designs could be optimised for base-station applications. Some of the

significant specific research objectives that were established by the industrial partner and Cardiff University are identified in the list below, and shown in Figure 6.

- Suitability of device technologies within the Doherty PA
- Optimising the Doherty for linearity, efficiency and bandwidth
- A description of distortions generated within the Doherty PA
- Device scaling for the *main* and *auxiliary* amplifiers
- Optimal matching topologies
- The use of active bias
- Recommended linearisation methods

Whilst developing an understanding of the Doherty PA application and formulating a strategy on how best to realise the objectives, it became clear that there was more to this 'simple' PA structure than was first apparent. A theme of work emerged that naturally broke-down into two distinct paths: firstly, addressing the numerous Doherty issues relating to fundamental Doherty behaviour, and secondly addressing those issues relating to harmonic behaviour of the Doherty.

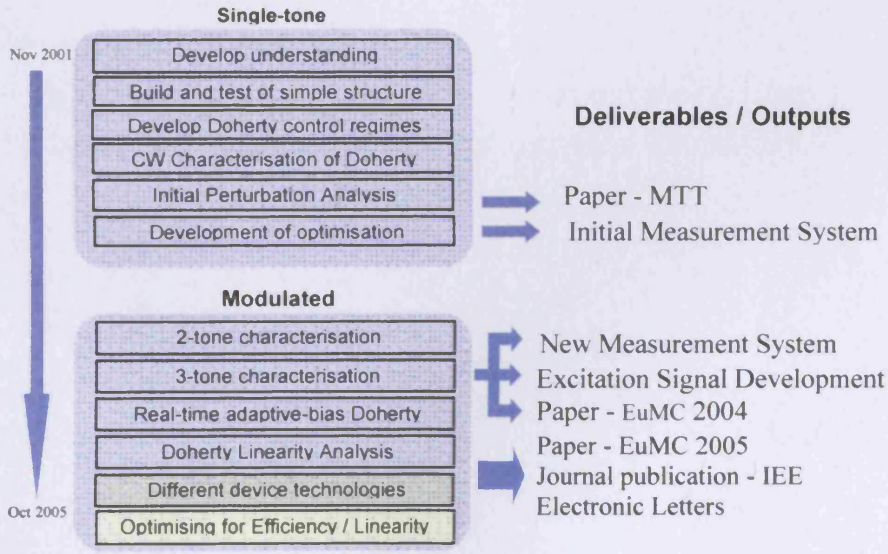


Figure 6 - research strategy

An early decision was taken to focus on the exploration of fundamental Doherty behaviour through the development and use of test structures that provided a high degree of harmonic suppression. This would allow research effort to concentrate on the observation of fundamental Doherty behaviour in the absence of significant

harmonics. It was considered that once a good understanding had been established, harmonic analysis could be addressed at a later stage of the research, which would involve adapting existing harmonic load-pull and waveform measurement systems to support such an activity

1.11 Thesis Organisation

This thesis is laid out and structured in five significant sections: following an introduction, Chapter two considers some essential Doherty background and focuses on the classical, and a number of other Doherty PA topologies in detail, with the aim of highlighting the limitations of simplistic designs. Chapter three goes on to introduce some of the measurement issues relating to Doherty characterisation in general, whilst chapters four and five address single-tone and modulated Doherty measurement and characterisation respectively. Finally, chapter six deals with the design, fabrication and measurement of a number of experimental Doherty structures using a number of different device technologies and characterisation techniques. The thesis concludes with a discussion of future work, and directions for future research.

Chapter 2 The Doherty Amplifier – Theory and Operation

The purpose of this chapter is to briefly review the fundamental Doherty theory that is relevant to the *main* body of this research, with the intention not to describe Doherty PA concepts in every detail (there are many excellent publications that already do this [21-24]), but rather to focus on some of the more interesting aspects of Doherty operation that are generally not covered in detail in literature.

2.1 Doherty Fundamentals

The Doherty PA is an elegant multiple-device structure that in its classical form works by typically employing an *auxiliary* device to maintain a constant-voltage, high-efficiency state at the output of a second, *main* device. The true elegance of the Doherty lies in the fact that the *auxiliary* power that is injected into the output matching structure, as well as bringing about very specific and efficient *main* device behaviour has an important additional role: it combines with the *main* device power in the load in such a way that the overall structure remains linear. This is a truly remarkable feat and promises to offer a panacea to modern PA design: high PA efficiency over wide dynamic range with no degradation in linearity or output power performance.

2.1.1 The concept of active load-pull

Controlled device interaction and specifically the concept of active load-pull are at the very centre of Doherty operation. Understanding this process is fundamental in understanding Doherty behaviour itself, and the usual place to begin is by considering the simplified circuit shown in Figure 7 [21].

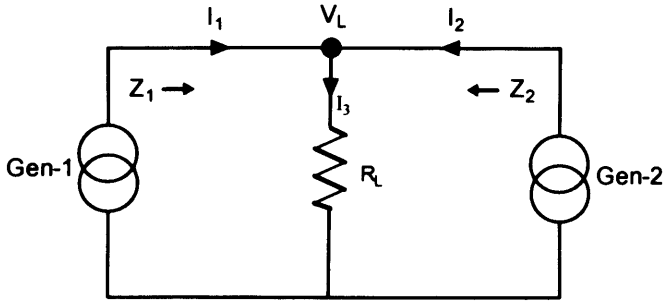


Figure 7 – simplified equivalent circuit

Here, two microwave transistors are modelled using two ideal current sources, *Gen-1* and *Gen-2* connected to a common load (R_L). It is clear that if current generator *Gen-2* is inactive and of high impedance, current generator *Gen-1* will be presented with a load of

R_L and will develop a voltage $V_L = I_1 \cdot R_L$. If however, Gen-2 begins to supply a current I_2, then the resultant voltage developed across the load can be calculated using the simple circuit theory summarised in (1) and (2).

$$V_L = I_3 \cdot R_L \qquad (1)$$

$$V_L = R_L(I_1 + I_2) \qquad (2)$$

In terms of DC, any additional current flowing in the load will cause an increased voltage to be developed across the load, which is the same effect that would be observed if R_L were to physically increase. The diagram of Figure 7 can therefore be redrawn to describe the new, '*effective*' load $R_L^{'}$ that is presented to Gen-1. This is shown in Figure 8 and defined in (3).

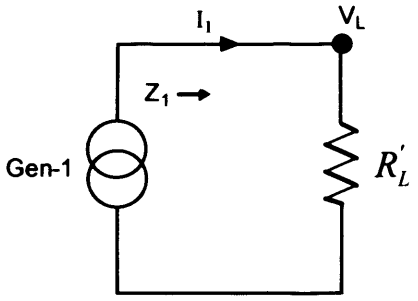


Figure 8 – simplified Doherty equivalent circuit from perspective of Gen-1

$$R_L^{'} = \frac{V_L}{I_1} \qquad (3)$$

Substituting (2) into (3), the *effective* load of $R_L^{'}$ can be defined in terms of the actual load R_L along with currents I_1 and I_2, as described by (4), where it is clear that any increase in I_2 will result in an increase in $R_L^{'}$.

$$R_L' = \frac{R_L(I_1 + I_2)}{I_1} \qquad (4)$$

As the structure is symmetrical, the effective load R_L^* presented to *Gen-2* can be defined using the same approach as shown in Figure 9 and defined in (5), where conversely it can be seen that assuming I_1 is present, any increase in I_2 will cause a decrease in R_L^*.

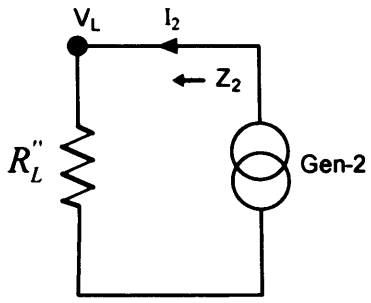


Figure 9 – simplified DC equivalent circuit from perspective of Gen-2

$$R_L^* = \frac{R_L(I_1 + I_2)}{I_2} \qquad (5)$$

This approach can be easily extended to AC by representing currents, voltages and impedances in complex form. With reference to Figure 7, this is summarised in (6) and (7).

$$Z_1 = R_L\left[1 + \frac{I_2}{I_1}\right] \qquad (6)$$

$$Z_2 = R_L\left[1 + \frac{I_1}{I_2}\right] \qquad (7)$$

In summary, it can be seen how the effective load presented to one device can be modified by the injected current from another. In the above example for instance, it is clear that an increasing current I_2 will lead to an increasing load impedance Z_1, and a decreasing load impedance Z_2.

In the case of the Doherty PA, the current generators Gen-1 and Gen-2 are replaced by *main* and *auxiliary* active devices. The situation needs to be slightly different however and both *main* and *auxiliary* devices must experience a decreasing load with increasing input drive. This is achieved through the presence of a critical $\lambda/4$ impedance transformer (*T1* in

Figure 10) linking the outputs of *main* and *auxiliary* devices, which has not been included in the above analysis for reasons of simplicity. It is however an essential element in any Doherty structure and is responsible for inverting an increasing impedance at the load to the necessary decreasing impedance for presentation to the *main* device.

2.1.2 The classical Doherty – an Introduction

The classical Doherty architecture consists of *main* and *auxiliary* devices connected to a shared load via an impedance inverting λ/4 transformer (*T1*), as illustrated in Figure 10. In order to allow the *main* and *auxiliary* voltages to sum in-phase at the load, a delay line (*T2*) is usually incorporated into the *auxiliary* path to compensate for the phase delay introduced by the inverting transformer (*T1*). The following explanation of the principals of Doherty operation assumes that the input signal is split symmetrically between the *main* and *auxiliary* devices.

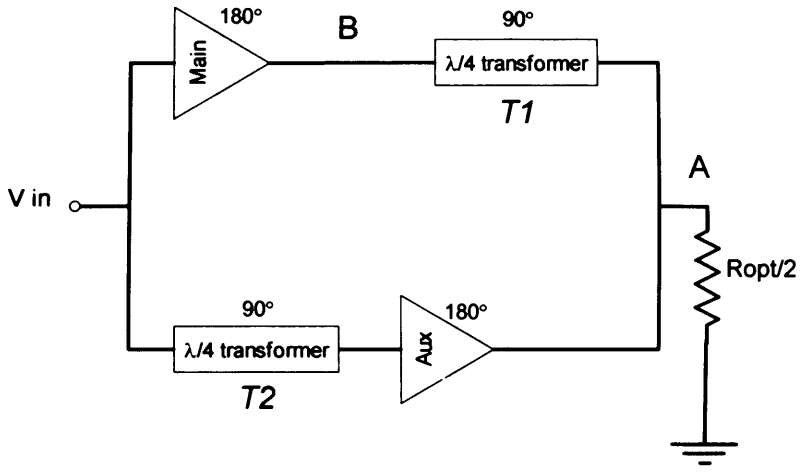


Figure 10 – simplified Doherty structure

Conduction behaviour is different for *main* and *auxiliary* devices, and can be described as a function of input drive voltage magnitude. In order to achieve the required device behaviour, control must be established such that the *main* device remains active over the entire defined dynamic range, whilst the *auxiliary* device becomes active for only part of the dynamic range between a pre-defined transition point (P_T), and the point of maximum linear output power (P_{max}). In the classical Doherty, P_T is defined to exist at 6dB 'backed-off' from P_{max}. Under maximum drive conditions and regardless of the control mechanism used, the *main* and *auxiliary* devices must deliver the same maximum output power into a load of R_{opt}, where R_{opt} is defined as the *main* device optimum load for the bias condition used. The 'delayed' conduction of the *auxiliary* device relative to the *main* device is achieved through the use of fixed, offset biasing in combination with devices with different

gain. For example, the *main* device can be biased in class-B whilst the larger *auxiliary* device would be biased in some degree of class-C. Generally, the depth of class-C bias is chosen such that the *auxiliary* amplifier starts to conduct when the input signal reaches a magnitude corresponding to the transition point. The gain of the *auxiliary* device will generally need to be increased to more than double that of the *main* device to compensate for lower fundamental current associated with reduced conduction angle *auxiliary* device biasing, and to ensure that both devices are delivering the same fundamental current at the point of maximum linear output power.

The devices' outputs are ultimately combined through a λ/4 transformer possessing a characteristic impedance (Z_T) equal to R_{opt}. A load impedance of $R_{opt}/2$ must then exist at the output of the *auxiliary* device, which is transformed by the inverting λ/4 transformer to an impedance of $2R_{opt}$ at the output of the *main* device.

2.1.3 Understanding Doherty behaviour

Firstly consider the behaviour of the *main* amplifier where the input drive is increased up to, but does not exceed the input power corresponding to the transition point. Over this *low-power* region of dynamic range, the *auxiliary* device can be assumed to be inactive[4] and the structure can be represented by the equivalent circuit shown in Figure 11.

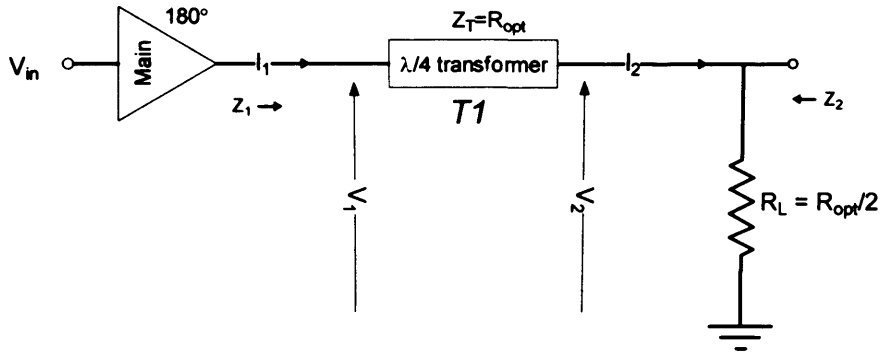


Figure 11 – main device in isolation

In response to the applied input voltage V_{in}, the *main* device generates an output current I_1 that flows through transformer T1. This is transformed to a voltage V_2 which is developed across the load, and in turn results in a current I_2 flowing in the load.

With reference to Figure 11, basic transmission line theory [25] tells us that the terminal voltages and currents will be modified by the λ/4 transformer, according to equations (8) to (13).

[4] This is not the case for all device technologies

$$Z_T = \sqrt{Z_1 Z_2} \tag{8}$$

$$V_1 I_1 = V_2 I_2 \qquad Z_1 = Z_T^2 / Z_2 \qquad Z_2 = Z_T^2 / Z_1 \tag{9}$$

$$I_2 = \frac{V_1}{Z_T} \tag{10}$$

$$I_1 = \frac{V_2}{Z_T} \tag{11}$$

$$V_2 = I_1 Z_T \tag{12}$$

$$V_1 = I_2 Z_T \tag{13}$$

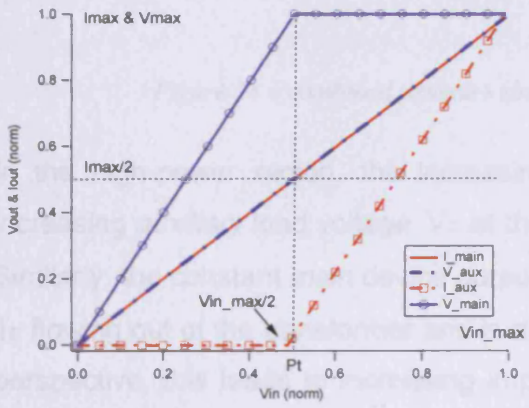


Figure 12 – main and auxiliary device fundamental voltage and current

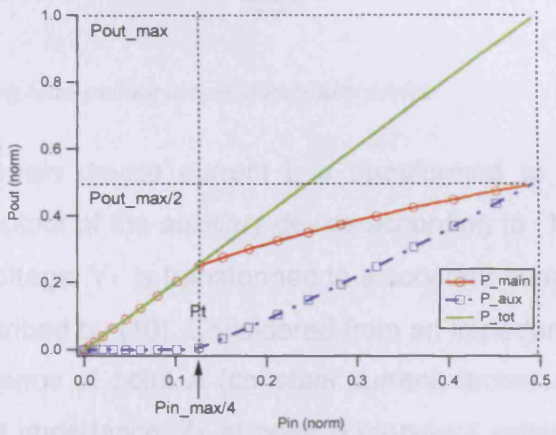


Figure 13 – main and auxiliary device fundamental power

By setting $Z_T = R_{opt}$, the net effect of these transformations throughout the low power region will be that the load impedance of $R_{opt}/2$ will be transformed and presented to the *main* device as an impedance of $2R_{opt}$, according to (9), which results in the *main* device achieving its maximum fundamental voltage magnitude whilst only delivering half its maximum fundamental current magnitude, as shown in Figure 12. This corresponds to the first peak of maximum linear efficiency at the *transition point* (P_T).

As the input drive increases beyond the *transition point*, the *auxiliary* amplifier begins to generate a phase-coherent current I_{aux}, which combines with the *main* current flowing into the load R_L. This area of dynamic range is termed the *high-power* region and the structure can be represented slightly differently, as shown in Figure 14. As discussed earlier, the combined current flowing into the load causes an increased voltage V_2 to be

developed across the load. The impedance Z_2 observed at point A, from the perspective of the *main* device will therefore increase, as identified earlier by (6). This will be transformed to a decreasing impedance at the output of the main device.

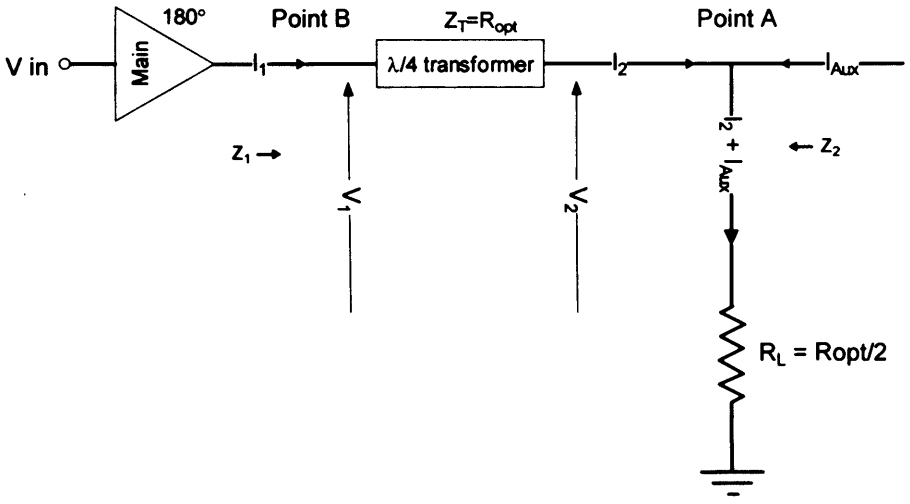


Figure 14 – combined structure showing load-pulling action of auxiliary device

In the high-power region, the increasing *main* device current I_1 is transformed to an increasing *auxiliary* load voltage V_2 at the output of the *auxiliary* device according to (12). Similarly, the constant *main* device output voltage V_1 is transformed to a constant current I_2 flowing out of the transformer and is described by (10). Considered from an impedance perspective, this leads to increasing impedance at point A (constant current, increasing voltage) which is transformed to decreasing impedance Z_1 at point B (constant voltage, increasing current).

Simple Ohm's law and (13) tells us that assuming I_2 is constant, a correct choice transformer characteristic impedance Z_T will lead to the required maximum, constant voltage at point B, and maximum *main* device efficiency over the entire 6dB dynamic range of the high-power region.

For any classical Doherty structure, this balancing act involves setting the characteristic impedance of the combining transformer to equal R_{opt}, and the load to R_{opt} /2.

2.1.4 The advantages of maintaining a constant output voltage

During theoretical analysis of the ideal Doherty, it is usually assumed that the *main* device efficiency will be constant and high throughout the high-power region of operation, i.e., where the *main* device is being actively load-pulled and maintaining a constant output voltage magnitude.

This is not always true however, even in the case of the ideal Doherty and it is important to realise that the efficiency profile of two, equal magnitude maximum peaks that has now become synonymous with the ideal Doherty behaviour occurs only under certain ideal bias conditions; specifically when the *main* device maintains a constant efficiency throughout the high-power region. This in turn only occurs when the *main* device is biased in ideal class-B, where the conduction angle is 180°.

To illustrate this point and to understand the important trade-off between bias, conduction angle and maximum achievable *main* device efficiency within the Doherty environment, it is constructive to analyse how a single device behaves whilst being maintained in a constant fundamental output voltage state.

2.1.4.1 An ideal analysis using IGOR

This analysis is conducted here using the Wavemetrics IGOR software environment [26] and a relatively ideal, simple device model extracted from pulsed DC measurements of a GaAs MESFET device, as discussed in 6.1.1. Figure 15 presents the maximum achievable efficiency as a function of drive and gate bias for a constant fundamental output voltage magnitude, as would be the condition for the *main* device in a Doherty environment. Four different biasing arrangements are highlighted, specifically class-C, class-B, class-AB and finally class-A. The simulation results show that the bias condition offering the most constant efficiency over the upper 6dB of dynamic range is class-B, as predicted, whereas class-AB and class-A bias conditions show increasingly degrading efficiency with back-off due to high quiescent drain current. The class-C case can be seen to offer increasing efficiency with back-off.

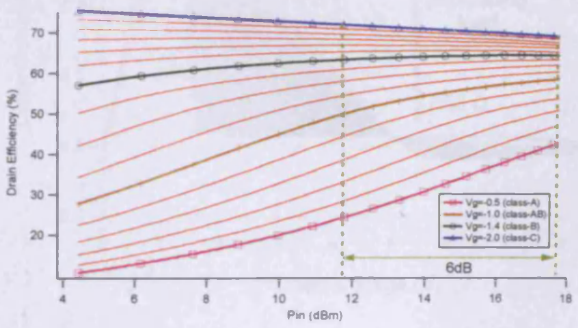


Figure 15 – main device efficiency as a function of P_{in} and gate bias whilst maintaining a constant, maximum output voltage

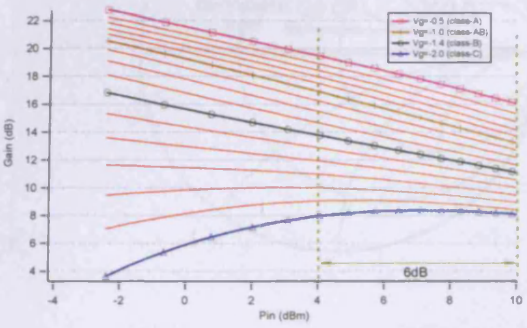


Figure 16 – main device gain as a function of P_{in} and gate bias whilst maintaining a constant, maximum output voltage

Figure 16 shows the corresponding gain in dB and illustrates the compressive nature of the Doherty's *main* device under constant output voltage conditions, which is due to the

fact that the output current is increasing whereas the output voltage is static. It is important to remember that if the *auxiliary* device was considered separately, a similar expansion would be observed, resulting in overall constant gain and linear performance. It is interesting to observe that the class-B case offers the best agreement, although all classes of bias between class-B and class-A offer a reasonable comparison. This is a useful analysis as it identifies the role of the *auxiliary* device, i.e. what it needs to do in order to maintain overall linear performance or flat gain. In other words, in order to achieve overall linear performance, the *auxiliary* device needs to produce an expansive gain characteristic that is the inverse of the chosen *main* device gain characteristic.

2.1.4.2 A more realsitic analysis using Agilent's ADS

By using a simple ADS simulation employing a vendor-supplied Fujitsu FLK-102XV device model, it was possible to analyse this in a little more detail and with additional realism. In this way, the above ideal analysis could be developed to give a better indication of what could actually be expected to happen when the above was practiced on a real device in a real measurement scenario. As before, the output voltage swing of a single, *main*, shallow class-B biased device was maintained at a constant, maximum value and over a very wide dynamic range of input power. This was achieved within ADS using the optimiser to identify the load required to fulfil this condition. The set of load-lines that resulted are shown in Figure 17.

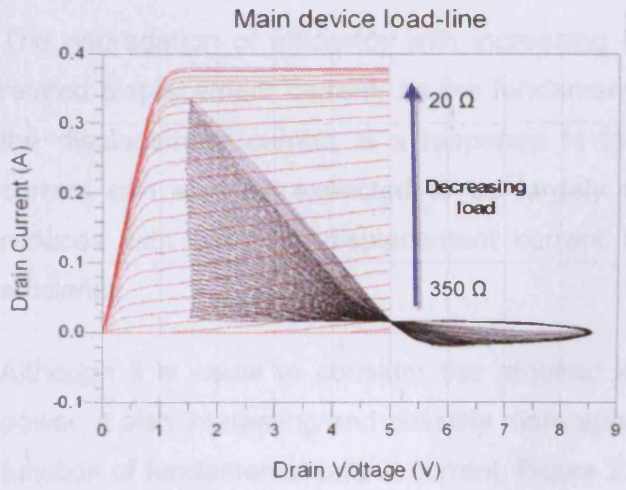


Figure 17 – ADS simulated main device dynamic load-lines for loads ranging between 20 Ω and 350 Ω

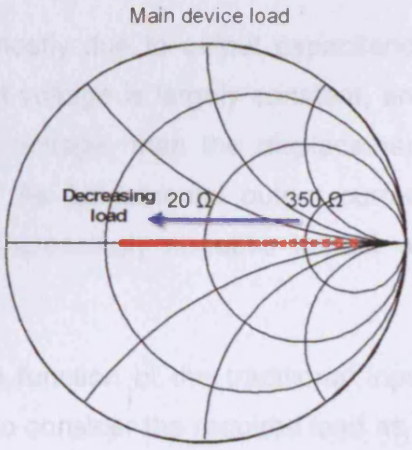


Figure 18 – Smith chart trajectory of dynamic load normalised to 50 Ω.

For reasons of simplicity and because the output capacitance of this device is quite small, the optimiser was constrained to changing only the real part of the load, the trajectory of which is presented in terms of impedance normalised to 50Ω in Figure 18. Figure 19

shows the constant fundamental drain voltage magnitude that is achieved, and also how, although high efficiency is maintained over most of the dynamic range, it does begin to degrade quite rapidly at lower drive levels. Figure 20 shows the fundamental gain as a function of fundamental drain current, and demonstrates the compressive characteristic of the shallow class-B *main* device in the constant output voltage state, which is a requirement of Doherty. This clearly does not exist throughout the entire dynamic range however with the gain collapsing at lower drive levels, where the load-line is forced to operate low-down in the I-V plane.

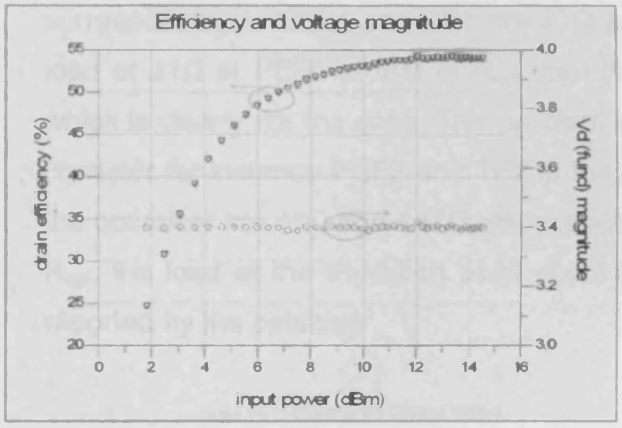


Figure 19 – ADS simulated efficiency and fundamental drain voltage magnitude vs input power for main device in class-B under constant O/P voltage condition

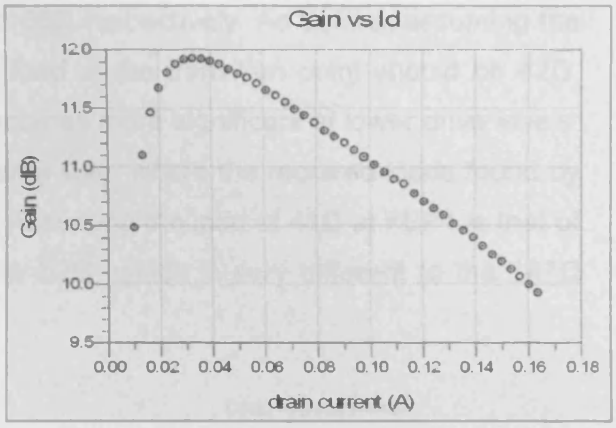


Figure 20 – ADS simulated Gain vs Id plot for device in class-B under constant O/P voltage condition

The degradation of efficiency with increasing load is mostly due to output capacitance related displacement current; as the fundamental output voltage is largely constant, and the displacement current is a response to the output voltage, then the displacement current can also be expected to be largely constant. As fundamental output current reduces with back-off, displacement current has an increasingly negative impact on efficiency.

Although it is usual to consider the required load as a function of the traditional input power, it also interesting and possibly more appropriate to consider the required load as a function of fundamental output current. Figure 22 shows for instance two pairs of markers that both describe an output dynamic range of 6dB. The upper points of the two pairs (PEP1a and PEP2a) represent two cases of maximum power, whilst the lower value markers correspond to the output current at two corresponding cases of transition point (TP1a and TP2a). For the first pair of points, the required loads found by the optimiser that correspond to PEP1a and TP1a are 21Ω and 43Ω respectively. If it is assumed that the load of 21Ω at PEP1 is that of R_{opt}, then the load at the corresponding transition point

should in theory be 2 R_{opt} or 42Ω. In fact it is found to be 43Ω, which is very close. The other two points, which are still 6dB apart, describe a dynamic range that exists much lower in the IV-plane. If these are considered in the same way, the required loads found by the optimiser, that correspond to PEP2a and TP2a are 86Ω and 171Ω respectively. Again assuming that the load of 86Ω at PEP1 is that of R_{opt}, then the load at the corresponding transition point should in theory be 2 R_{opt} or 172Ω. Again, the optimised value is very close at 171Ω.

If this is now considered in terms of input power, the required loads found by the optimiser corresponding to PEP1 and TP1 are 21Ω and 56Ω respectively. As before, assuming the load of 21Ω at PEP1 is that of R_{opt} then the load at the transition point should be 42Ω, which is clearly not the case. This problem becomes more significant at lower drive levels: consider for instance PEP2 and TP2 in the same way, where the required loads found by the optimiser are 41Ω and 147Ω respectively. Assuming the load of 41Ω at PEP1 is that of R_{opt}, the load at the transition point should be 82Ω, which is very different to the 147Ω reported by the optimiser.

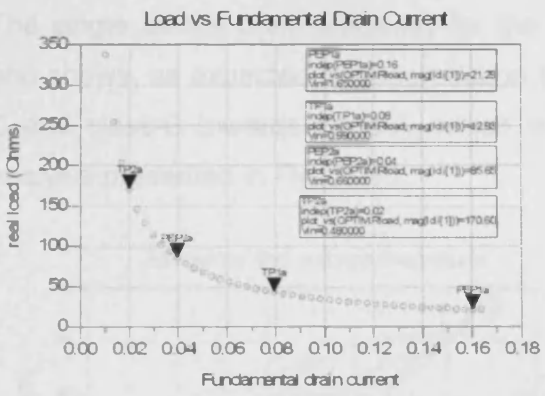


Figure 21 – ADS simulated Gain vs Id for device in class-under constant O/P voltage condition

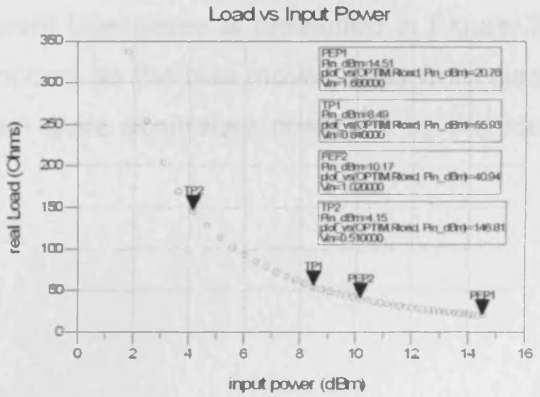


Figure 22 – ADS simulated Gain vs P_{in} for device in class-under constant O/P voltage condition

This effect is due to non-constant device gain over dynamic range and only becomes an issue when considering the required Doherty loads in terms of applied input power. This effect has large implications for Doherty structures that rely upon precise relative power relationships that are determined at the structure's input, such as is case is the classical Doherty where a passive power splitting arrangement is used.

The final part of this simulated analysis explores what happens when the above simulation is conducted for a number of different gate bias conditions. Figure 23 shows the dynamic load-lines that result from bias arrangements ranging from class-C, through class-B to class-AB. The optimised maximum fundamental output voltage swing is maintained

constant in each case, and the resulting variation of gain is presented in Figure 24, where it is clear that the compressive nature changes significantly for the class-C case. It is also clear that the results agree very well with those resulting from the ideal analysis in Figure 16.

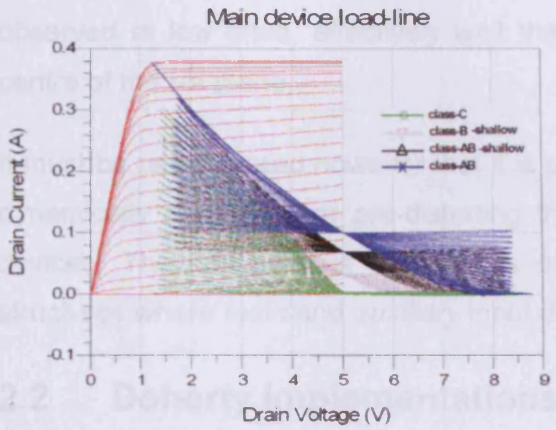


Figure 23 – ADS simulated main device dynamic load-lines for different cases of gate bias

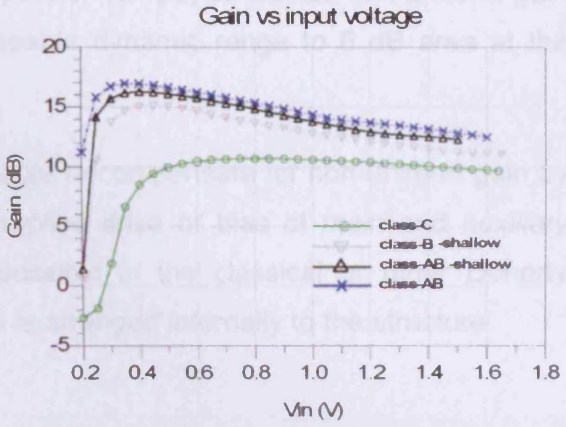


Figure 24 – gain as a function of input voltage for different cases of gate bias

The single device drain efficiency for the different bias cases is presented in Figure 25, and shows, as expected the degradation that occurs as the bias moves away from class-C and class-B towards class-A, which is again quite accurately predicted by the ideal analysis presented in Figure 15.

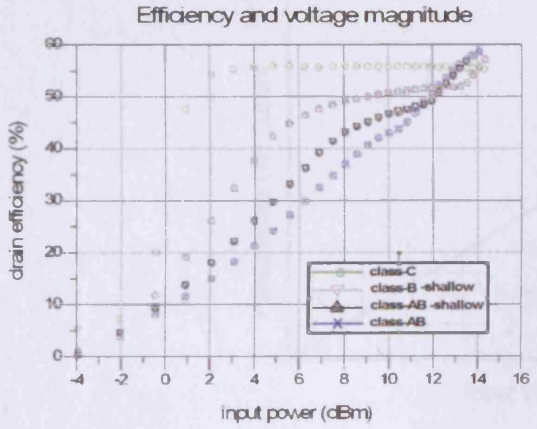


Figure 25 – efficiency as a function of input power, for different cases of gate bias

This analysis becomes important when considering the operational range of the Doherty as when dynamic range is increased, the *main* device load-line is forced to occupy an increasingly large area of the I-V plane. By plotting gain as a function of fundamental drain current as in Figure 20, it becomes clear that the dynamic range of the classical Doherty is

effectively limited by the area of the I-V plane where the trans-conductance is relatively constant. This can become particularly important when considering device technologies where gain over the I-V plane is non-uniform, which becomes apparent in the design of the GaN Doherty discussed in Chapter 6, where the combined effects of 'current-slump' and 'knee-walkout' associated with RF-DC dispersion [27-29] as well as non-uniform gain observed at low drive, effectively limit the useable dynamic range to 6 dB area at the centre of the I-V plane.

It must be remembered however that it is possible to compensate for non-uniform gain by dynamically modifying, or pre-distorting the applied drive or bias of *main* and *auxiliary* devices. The key point is that this is not possible in the classical or other Doherty structures where *main* and *auxiliary* input drive is arranged internally to the structure.

2.2 Doherty Implementations

A number of Doherty realisations are discussed in this thesis, all of which can be considered as being variations of the classical Doherty approach, differing technically only in terms of the methods used to control the conduction behaviour of the *auxiliary* device. All of the implementations however strive to achieve the ideal *main* and *auxiliary* fundamental current growth profiles shown in Figure 26 below, which assumes that there is a linear trans-conductive relationship between input voltage and output current.

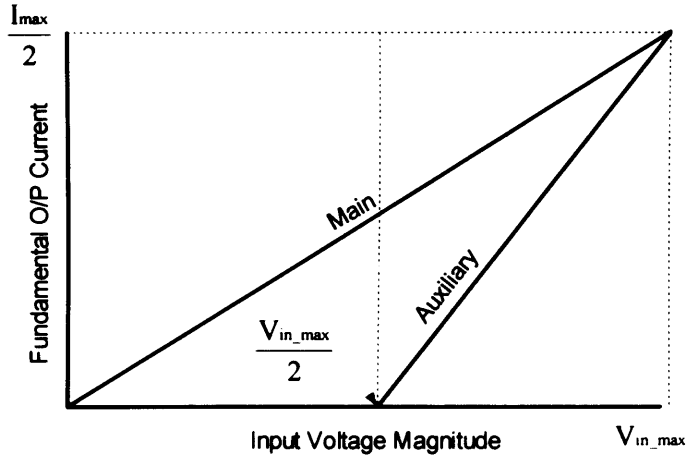


Figure 26 – main and auxiliary device ideal fundamental current behaviour as a function of input voltage magnitude

2.2.1 The classical Doherty

The classical Doherty is used here as a reference case upon which all other variations are based, so it is worth spending some time defining exactly what constitutes the approach.

This is of course open to some interpretation, but for the purpose of this work, the classical Doherty is defined as possessing the following specific properties:

a) A symmetrical power split at the input and a 90° phase delay is introduced into the *auxiliary* signal path to compensate for the combining λ/4 transformer at the output.

b) The point of *auxiliary* device conduction is controlled through the use of fixed, offset bias. This is assumed to be class-B for the *main* device and the specific depth of class-C that causes the *auxiliary* device to begin conducting at the transition point.

c) Both *main* and *auxiliary* devices deliver the same maximum fundamental current at the point of maximum power.

d) The transition point is located 6dB backed-off from the point of maximum power hence the active dynamic range is defined as being 6dB.

e) The load impedance at the output of the *auxiliary* device is arranged to be equal to R_{opt} /2 in the low power region of operation.

f) The characteristic impedance of the *main* combining output transformer is equal to R_{opt}, where R_{opt} is the optimum design impedance for the *main* device in the bias conditions used.

g) The required fundamental output current delivered by each device is achieved by suitable scaling, i.e. using a larger *auxiliary* device.

The advantages of the classical Doherty approach over other implementations is that it is simple, easily realisable, self-contained and requires no external control or signal pre-conditioning. A disadvantage of the approach is that use of reduced conduction angle biasing of the *auxiliary* device results in the generation of both even and odd order harmonics that can prove difficult to remove. Another disadvantage is associated with the turn-on behaviour of the *auxiliary* device: whereas abrupt turn-on is advantageous in the Doherty, a soft turn-on characteristic can cause problems resulting in degraded efficiency in the low-power region of operation and around the transition point.

2.2.2 The input-attenuation Doherty

Another way of controlling the conduction behaviour of the *auxiliary* device is to modify the magnitude of the applied *auxiliary* device excitation in response to the instantaneous magnitude of the applied *main* device excitation, as illustrated in Figure 27. This approach can be simplistically visualised by the placement of a variable attenuator in the *auxiliary*

input path, as discussed in [21, 22], but in practice may be more readily accomplished using an IQ modulator[30], which has the additional advantage of being able to adjust relative input phase[5].

There are a number of advantages associated with this approach. Firstly, both *main* and *auxiliary* devices can be optimally biased in class-B such that odd-order harmonics are suppressed, dramatically simplifying harmonic behaviour. As conduction is being controlled externally, there is no longer a rigid requirement relating specific device gain, thus allowing similar devices to be used. Another important advantage is that any unwanted bias-dependent behaviour is avoided, such as bias-dependent gain-phase, which for instance has been observed in GaAs and GaN devices used [31-33].

The input-attenuation approach does have its disadvantages however including the need for additional complexity, both in terms of input signal pre-conditioning, as well as detection of the input magnitude. Also; efficiency tends to be slightly degraded in the low power region and around the transition point, due to the unavoidable presence of *auxiliary* device quiescent current. Another problem is the *auxiliary* device will tend to have low gain when its output power is low, which occurs around the transition point. In order to reduce the impact of this problem, it is possible to compensate by modifying the applied *auxiliary* input magnitude profile such that proportionately more drive is applied, as suggested by the 'optimal' trace shown in Figure 27.

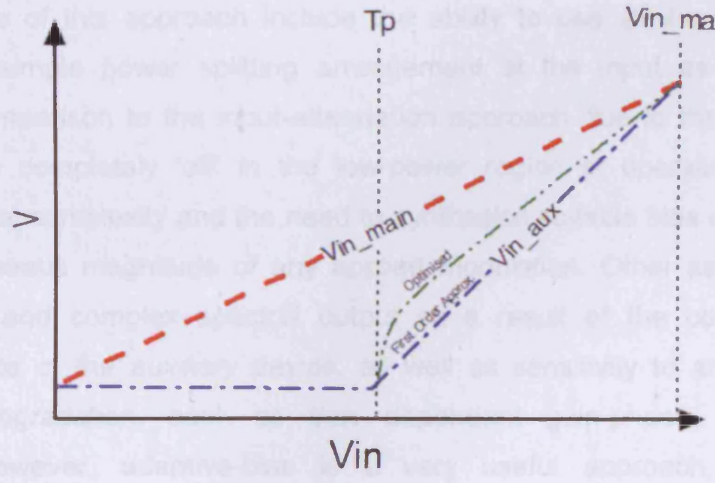


Figure 27 – input voltage profile for input-attenuation Doherty implementation

2.2.3 The adaptive-bias Doherty

Yet another way of meeting the fundamental current contribution requirement illustrated in Figure 26 is to control *auxiliary* conduction by modifying the *auxiliary* base or gate bias

[5] This is mentioned here as it is important for Doherty optimisation, which is discussed in later chapters.

voltage. This method exploits the fact that trans-conductance (gm), which is a highly non-linear function of conduction angle and can be approximated as being relatively linear over a limited range of conduction angles between 0 and π radians. This is illustrated in Figure 28 which shows typical device behaviour in terms of fundamental current, DC drain current and drain efficiency as a function of conduction angle, and also in Figure 29 which presents the harmonic current spectra as a function of applied gate voltage. These results have been obtained using the simple GaAs MESFET model and the IGOR software environment. Peak values of output current and output voltage have been maintained at their maximum values throughout both sweeps.

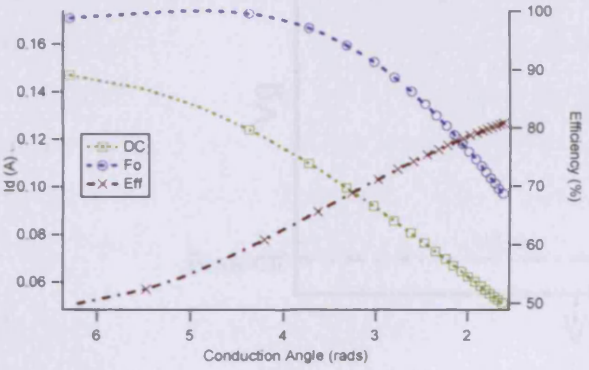


Figure 28 – fundamental current, DC current and efficiency

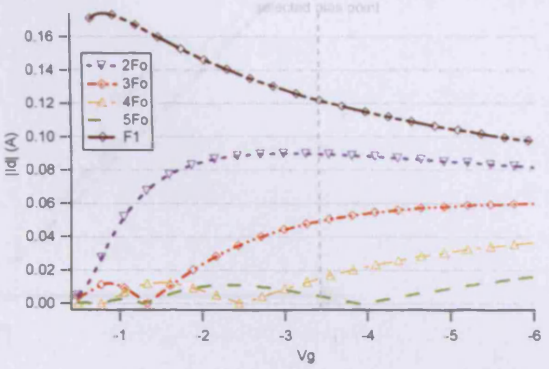


Figure 29 – harmonic current spectra as a function of gate voltage

The advantages of this approach include the ability to use similar sized devices, the retention of a simple power splitting arrangement at the input as well as improved efficiency in comparison to the input-attenuation approach due to the ability to bias the *auxiliary* device completely 'off' in the low-power region of operation. Disadvantages include additional complexity and the need to synthesise suitable bias signals in response to the instantaneous magnitude of any applied modulation. Other associated problems include a rich and complex spectral output as a result of the continually changing conduction angle of the *auxiliary* device, as well as sensitivity to any bias dependent performance degradation, such as bias dependent gain-phase. Even with these complexities however, adaptive-bias is a very useful approach, especially when attempting to extract the best possible efficiency from prototype Doherty structures.

The general adaptive-bias approach is illustrated in Figure 30 and involves firstly adopting a specific *auxiliary* gate-bias voltage that is sufficiently negative (in the case of a depletion mode device) to prevent the *auxiliary* device from conducting during the entire low power region of operation. This voltage is termed '*bias_off*' and is a critical value in the adaptive-bias approach as it needs to be set such that the *auxiliary* device is almost conducting as

the transition point is approached. From this point on, the adaptive-bias system takes over, applying the necessary gate bias to cause the required *auxiliary* device conduction.

As with the input-attenuation approach, it is possible to compensate for the soft turn-on characteristic of the *auxiliary* device by modifying the applied *auxiliary* gate-bias profile from the first-order approximation. This is illustrated by the example 'optimised' trace in Figure 30.

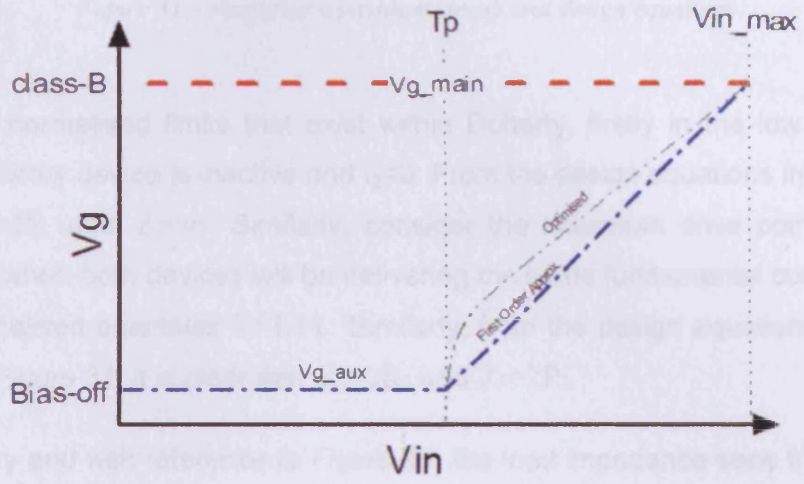


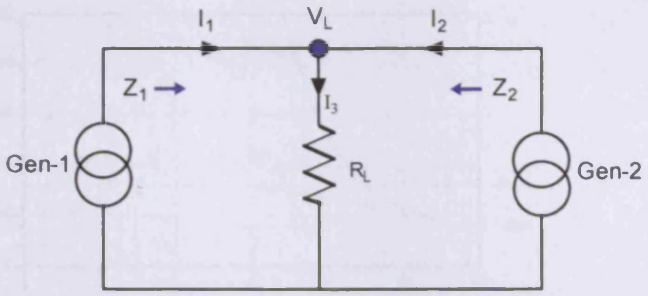
Figure 30 – gate voltage profile for input adaptive-bias Doherty implementation

2.2.4 The extended or asymmetrical Doherty

For reasons of simplicity, all Doherty realisations discussed in this work employ a dynamic range of 6dB. This is of limited use however when considering Doherty realisations for modern modulation schemes where the PAR can extend 10 dB or more. Although the methods and implications of extend the dynamic range of the Doherty are considered outside the main focus of this work, they are discussed briefly in Appendix 5.

2.3 Understanding Doherty load-line behaviour

This section has been included to address the confusion that often exists regarding load-line behaviour in terms of the dynamic impedance that is presented to each device. For example, there is a common misconception that the *main* device experiences a decreasing load impedance whilst the *auxiliary* device experiences the inverse, i.e. an increasing load impedance. To analyse this, reconsider the simple AC active load-pull circuit and design equations presented earlier in this chapter.



$$Z_2 = R_L\left[1+\frac{I_1}{I_2}\right]$$

$$Z_1 = R_L\left[1+\frac{I_2}{I_1}\right]$$

Figure 31 – simplified equivalent circuit and design equations

Consider the normalised limits that exist within Doherty, firstly in the low power region where the *auxiliary* device is inactive and I_2=0. From the design equations in *Figure* 31 it is clear that $Z_1=R_L$ and $Z_2=\infty$. Similarly, consider the maximum drive point in the high-power region when both devices will be delivering the same fundamental current, where in terms of normalised quantities $I_2=I_1=1$. Similarly, from the design equations on the right-hand-side of *Figure* 31, it is clear that $Z_1=2R_L$ and $Z_2=2R_L$.

So in summary and with reference to *Figure* 31, the load impedance seen from Gen-1 can be expected to increase from R_L to $2R_L$, and the load impedance seen from Gen-2 to decrease from infinity to $2R_L$. In the Doherty structure however, the presence of the impedance transformer and the load of $R_{opt}/2$ means that the load impedance seen from the *main* device is inverted, and will decrease from $2R_{opt}$ to R_{opt}, whilst the load impedance seen by the *auxiliary* device will also decrease from infinity to R_{opt}. To further clarify this point, the following plots show the simulated impedance presented to both *main* and *auxiliary* devices for three different Doherty realisations, specifically classical, input-attenuation and adaptive-bias.

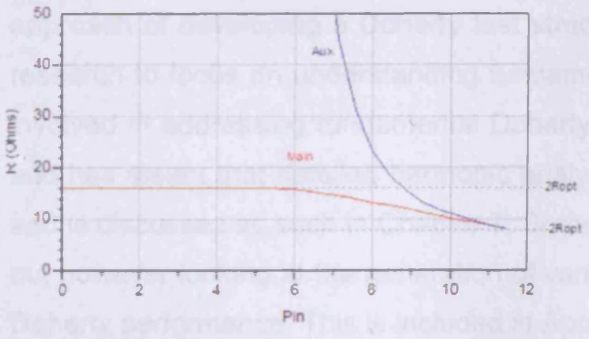


Figure 32 – load impedances in adaptive-bias Doherty (R_{opt}=8 Ω)

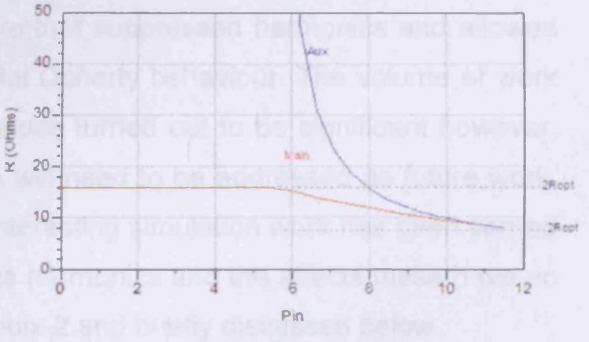


Figure 33 – load impedances in input-attenuation Doherty (R_{opt}=8 Ω)

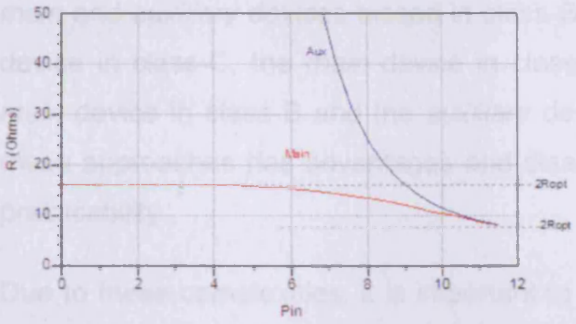


Figure 34 – load impedance in classical Doherty (R_{opt}=8 Ω)

Eqn Zmain=Vdmain[1]/Id_main.i[1]
Eqn Zaux=Vdaux[1]/Id_aux.i[1]

Figure 35 –simulation equations used to extract main and auxiliary load impedance

These realisations are discussed elsewhere in this chapter, but here it is interesting to note that although the expected impedance behaviour is clearly identifiable in all three plots, there are some subtle differences in both *main* and *auxiliary* impedance behaviour. It is clear for instance that the change in *main* device load needed to maintain a constant voltage swing for both adaptive-bias and input-attenuation is nearly a linear function of input power, which is not the case for the classical approach.

It is also clear from each plot exactly where the *auxiliary* device becomes active and starts to cause the *main* device load to change. As expected, the adaptive-bias approach causes *auxiliary* conduction to begin at the transition point of 6dBm, whereas in both input-attenuation and classical approaches, the *auxiliary* load can be seen to change before the transition point is reached.

2.4 Harmonics and the Doherty

Harmonic generation and termination play important roles in Doherty design and can have a large influence on overall performance. It was this realisation that prompted the initial approach of developing a Doherty test structure that suppressed harmonics and allowed research to focus on understanding fundamental Doherty behaviour. The volume of work involved in addressing fundamental Doherty issues turned out to be significant however, and has meant that detailed harmonic analysis will need to be addressed as future work, and is discussed as such in Chapter 7. Some interesting simulation work has been carried out however looking at the generation of various harmonics and the affects these have on Doherty performance. This is included in Appendix-2 and briefly discussed below.

2.4.1 Harmonic generation – help or hindrance

As has been discussed, the Doherty can be realised in a number of different ways, where the devices themselves may be established in various bias conditions. For example, both

main and *auxiliary* devices biased in class-B, the *main* device in class-B and the *auxiliary* device in class-C, the *main* device in class-AB and the *auxiliary* device in class-B, the *main* device in class-B and the *auxiliary* device dynamically biased, and so on. Each of these approaches has advantages and disadvantages both in terms of performance and practicability.

Due to these complexities, it is important to understand the issues surrounding harmonic generation within the Doherty structure, as it is considered that detailed understanding of harmonic behaviour may prove to have a significant impact on a number of critical design issues. These include the following:

Simplification of design – Unlike suppression of even-order harmonics, suppression of odd-order harmonics is problematical. If odd-order harmonics can be to a large extent ignored, then the design process can be simplified.

Choice of architecture – Different Doherty realisations generate harmonics of different magnitudes. For example, due to a constantly changing conduction angle with increasing drive, the spectra for both classical and adaptive-bias Doherty structures tend to be quite complex, and rich in both even and odd harmonic components. In contrast, the input-attenuation Doherty involves establishing both devices in a static, optimised class-B bias condition, where odd-order harmonics are minimised.

Choice of device – Device characteristics play a large role in the nature of harmonic generation: the magnitude of the generated harmonics is a function of the device dynamic transfer characteristic, and the number of significant harmonics generated will relate to the operational bandwidth of the device. One example where device properties can present an advantage is with LDMOS device technology, where large output capacitance effectively limits bandwidth and naturally suppresses harmonic voltage generation. It is evident however from recent publications [34-38] that there are significant problems that need to be addressed before these devices can be used within Doherty.

Optimisation – It must be stated that concentrating on suppressing generated harmonics may prove not to be the optimal approach, and there may be some advantage in using other, specific harmonic terminations for the *auxiliary* and *main* devices. One example is the possibility of using a class-F approach within a Doherty design [39].

Chapter 3 Doherty Measurement Issues

3.1 Overview

In the field of discrete device characterisation, the objective is generally to use a variety of measurement techniques to extract specific device behaviour that is ultimately useful in the PA design process. The resulting measurement information is traditionally used in the design of bias, matching and stabilisation networks, but is now more commonly used within CAD environments, either directly through the import of measurement data into file-based simulation components [40], or indirectly through the generation or extraction of various types of non-linear device models that can be used in design and optimisation [41]. The latter option moves towards the ideal design scenario where all PA design and optimisation is conducted within the CAD environment, and all measurement and characterisation restricted to only that which is necessary to develop adequate linear and non-linear models. This measurement based approach will typically involve measuring DC behaviour, small-signal bias dependent s-parameters, single-tone and modulated P_{in} -P_{out} as well as source and load-pull characterisation. These measurements would usually be conducted under different bias conditions, harmonic terminations and possibly different temperatures and IF impedance conditions.

Measurement approaches change when considering PA characterisation in contrast to device characterisation however, as it is realised that the discrete device is only one of many other components that comprise the PA, which will typically contain other active devices, matching networks, biasing networks, along with many other active and passive components. The consequence of this necessary and additional complexity is that individual active device behaviour is 'obscured' from the outside world, and hidden from any measurement approach. PA Characterisation is therefore generally limited to 'black-box' type approaches where the amplifier structure is measured in terms of generalised parameters that are a consequence of the interaction of all of these additional components. These include classical parameters such as spectral power, gain, efficiency, AM-AM, AM-PM, ACPR and EVM. Another way to view this is to realise that for a production PA, measurement tends to be limited to that required for 'compliance testing', and interrogative measurement is made impossible by the filtering nature of the input, output and bias structures; for instance it is not possible to measure waveforms as the harmonic content will usually have been filtered out.

Having said this, it is usually considered acceptable to 'lose' the detailed visibility of discrete device behaviour within the PA itself. This view is based upon the assumption

that the structure would have been optimally designed using detailed device measurement data in the first place.

3.2 Characterising the Doherty PA structure

The Doherty is one of a number of PA structures that rely upon beneficial device interaction in order to enhance efficiency over wide dynamic range. One of the attractive features of the Doherty is its elegant simplicity, with the classical structure consisting of as little as two active devices connected via a simple impedance matching network. In reality however, the realisation of functional Doherty PAs using modern microwave devices holds many hidden complexities that are generally brought about by the non-linear behaviour of the devices, coupled with active load-pulling effects; and conspire to cause problems that exist at both a fundamental and harmonic frequencies.

With these issues in mind, it can be appreciated that when faced with characterising the Doherty PA, there is an immediate and significant measurement problem: whereas observing device behaviour within static, well-behaved impedance environments is relatively straight forward, achieving the same visibility within the highly complex and dynamic impedance environments that exist within the Doherty structure is extremely difficult. This problem is further aggravated by the fact that that in some Doherty realisations, both the bias and excitation delivered to *main* and *auxiliary* devices will be dynamic functions of the applied drive magnitude [31, 42, 43].

Understanding the Doherty PA at a theoretical level is usually tackled in terms of the fundamental frequency component alone [21, 44]. It must be appreciated however that in reality, Doherty structures employ non-ideal and sometimes high-bandwidth devices, and the overall performance will be determined by the complete harmonic interaction between devices and their surrounding impedance environments. This complex behaviour cannot be easily explained through simple, idealised theory, and must be uncovered through some form of enhanced measurement approach [45].

3.2.1 A 'harmonic' measurement approach

At the start of the research activity, it was considered important to identify the characterisation approach that would allow the most complete understanding of interaction within the Doherty structure. It was quickly realised that in order to achieve this, it would be necessary to develop two key objectives: firstly, to understand and be able to ***synthesise*** the dynamic, harmonic impedance environments that surround both devices within the Doherty structure, and secondly, to be able to ***measure*** how the devices within

the Doherty respond to, and behave within these complex dynamic impedance environments.

The ability to externally synthesise harmonic impedances would allow the Doherty to be considered as separate *main* and *auxiliary* sections or branches. Once a 'first-order' understanding of individual device behaviour within the Doherty had been established, approximations of the harmonic impedances generated by *main*, and then *auxiliary* branches of the Doherty could be synthesised, whilst the real-life behaviour of *auxiliary* and then *main* devices, respectively, could be observed.

3.2.1.1 Synthesising impedance environments

The impedance environments that exist within the Doherty structure are complex functions of a number of dynamic and static variables. These variables include drive level, various device specific properties as well as characteristics of the passive impedance transforming output network that physically links the two devices. In addition, any device matching and harmonic termination networks also play a significant role.

In order to begin synthesising the required impedance environments, an initial, theoretically derived idea of the conditions that would exist in an ideal classical structure around each device is required [21]. Using harmonic load-pull techniques [46, 47], an experimental process is instigated that involves establishing the ideal classical Doherty impedance environment, and using this as a starting point from where exploration of how the devices react to this environment begins. Characterisation, including perturbation analysis is then possible, and this approach will is effective in identifying the conditions for optimal Doherty behaviour. As understanding of the impedance environments matures and develops, the initially crude behavioural models representing the impedance environments surrounding the active devices become increasingly accurate.

Although this approach is in its infancy, it is already proved fruitful and has led to a number of key observations relating to GaN Doherty behaviour [48] that are discussed in detail in Chapter 6. It is anticipated that further optimisation will become possible, specifically the impedance transformation networks responsible for presenting correct fundamental impedances, as well as the dynamic control over bias and relative input drive that is necessary in achieving Doherty behaviour in input-attenuation and adaptive-bias Doherty realisations respectively.

3.2.1.2 Characterising device response

The second requirement is to understand how the devices themselves respond to the dynamic impedance environments within the Doherty. Assuming for a moment that the

approach begins with an approximate, theoretical idea of the harmonic impedances that will be presented to the devices within the structure, harmonic load-pull together with waveform measurement techniques can be employed to characterise device behaviour under a specific range of synthesised harmonic load conditions. The analysis can be conducted in a number of different ways, and specifically:

Pseudo-real-time approach - the measured, real-time response of the device is used directly in the design and optimisation process.

Offline measurement-based behavioural model approach – focused measurement data can be collected and used 'off-line' within a CAD environment, allowing accurate, detailed investigation and optimisation exercises based on actual measured data.

The *off-line measurement-based behavioural model* approach is particularly interesting as it allows complex, active devices to be represented using actual, focused measurement data, whilst other passive circuit elements such as transmission lines are represented using reliable and well established CAD-based components. In using the 'off-line' model approach, the importance of anticipating the drive, bias and impedance environments within the Doherty cannot be understated, as this will allow the measurement scope for such a model to be limited to a manageable subset of bias, drive and impedance conditions, thus allowing the measurement time to conduct the necessary measurements to remain reasonable. As an example, consider a FET measurement based model that responds to input voltage, gate bias, drain bias and output reflection coefficient. If the eventual environments for the model are unknown, then measurements for all combinations of these independent variables will be required, making this an unrealistic option. If the application is known to be the Doherty PA however, a good idea of these operational conditions can generally be developed, and the number of necessary measurements dramatically reduced. Using this ideal approach, it is clear that a large degree of characterisation and optimisation could be achieved within the simulation environment. The additional advantage of employing the measurement based 'off-line' behavioural models is that the process is device independent, so could be applied equally effectively for example to Doherty structures employing GaAs pHEMT, LDMOS or GaN device technologies.

3.2.2 A 'fundamental' measurement approach

As discussed earlier in this chapter, it was considered that characterising the deceptively simple Doherty structure would lead to observations of many inter-related complexities that relate to both fundamental and harmonic behaviour. It was also considered that

although harmonic behaviour was going to be important, understanding Doherty behaviour at a fundamental level would be the critical factor in achieving good overall Doherty performance. The adopted strategy was therefore to initially focus on fundamental Doherty behaviour in the absence of harmonics.

Achieving this involved the design of a *simple*, *flexible*, *measurable* and *open*[6] Doherty measurement prototype structure that is shown in Figure 45, surrounded by a dedicated Doherty measurement system [31]. The structures ability to suppress the generation of harmonics allowed focus to be maintained on fundamental Doherty analysis. Once a good understanding had been developed, it would be possible to interpret the results gained from more in-depth Doherty analysis using more complex measurement techniques including waveform engineering through harmonic load-pull.

3.3 The Doherty Measurement Prototype

The Doherty measurement structure needed to contain all of the necessary elements to support Doherty behaviour, for example active devices, output impedance transformation network, harmonic suppression mechanisms, stabilisation mechanisms, bias circuits, etc, and would to all intents and purposes be a complete and functional Doherty amplifier. Whereas many aspects of the design are covered in Chapter 6, this section aims to introduce the first structures that incorporated initially GaAs MESFET devices, and later GaN HFET devices.

There are a number of subtle yet critical differences that distinguish the proposed measurement structure from other, more conventional Doherty structures. These differences were critical to the success of the approach and are identified in the following sections.

3.3.1.1 Suppression of harmonics

The suppression of harmonics was achieved through a combination of optimal class-B[7] bias to suppress the generation of odd-order harmonics, and the use of a shorted quarter-wave line as an even order harmonic trap, as shown later in *Figure* 46.

3.3.1.2 Maintaining structure simplicity

Based on measurement observations of previous, early prototype Doherty structures, it was decided that the primary design goal for the measurement prototype would be to keep the design as simple, symmetrical and compact as possible such that all physical

[6] The term 'open' describes a structure that allows various parameters to be changed or perturbed, which is in contrast to a classical 'closed' Doherty design where most parameters are set internally within the structure.

[7] Optimal class-B refers to the bias point near pinch-off that results in the best suppression of odd-order and especially third-order harmonic current spectra.

effects could be minimised and accurately predicted. One example is to minimise the physical distance and delay between each device's output and the impedance transforming network. This involved mounting the active devices literally onto the combining transformer in addition to using physically small, low-parasitic device packages. This is illustrated in Figure 36, where although exaggerated, the additional delay that can be introduced in physically mounting the devices away from the transformer can be appreciated, here shown as Δ1 and Δ2.

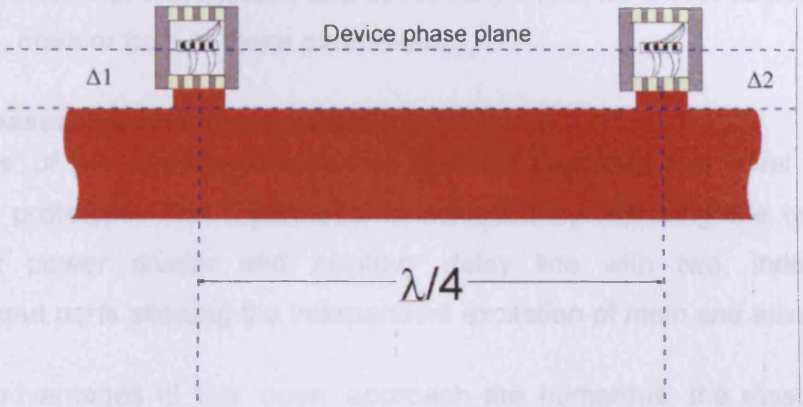


Figure 36 – example placement of main and auxiliary devices on main combining transformer

The additional delays can only interfere and detract from the normal operation of the critical λ/4 transformer, whose job it is to establish a precise impedance transformation between *main* and *auxiliary* device reference planes. Although it is possible to compensate for this error by reducing the length of the transformer, the element's behaviour will be significantly affected by any differences in impedance associated with the additional delay elements, and the ideal transforming nature of this element will be degraded (see 8.1.5) There may also be other parts of the circuit that rely upon this transforming element, such as the even-order harmonic trap. This network relies upon the *main* combining transformer being exactly λ/4 as the capacitive short needs to propagate to both *main* and *auxiliary* devices at all even harmonic frequencies.

3.3.1.3 Identical main and auxiliary devices

In any true classical Doherty design, the *main* and *auxiliary* devices must deliver the same fundamental output current at maximum drive [21]. In order to account for the lower *auxiliary* gain imposed by reduced conduction angle biasing, the *auxiliary* device needs to be typically 2.15 times the periphery of the *main* device. From a design perspective, it is possible to achieve this in a number of ways, for example through the use of devices with

different physical periphery and hence gain, or by physically coupling multiple packaged devices together. There are however a number of problems associated with both of these approaches including difficulty in sourcing appropriately sized devices, and the physical problems associated with coupling two or more, relatively large packaged devices at microwave frequencies.

In order to adhere to the primary design goal of maintaining structure simplicity, it was decided that the measurement prototype would employ identical devices. The implications of doing this, such as the need to realise increased *auxiliary* fundamental current would be the role of the measurement system, and specifically would be achieved through dynamic control of bias, drive or both of these parameters.

3.3.1.4 A measurable and 'open' structure

The 'openness' of the structure is arguably the most important and novel feature of the measurement prototype. This 'openness' is achieved by replacing the typical Doherty passive input power divider and *auxiliary* delay line with two, independent and symmetrical input ports allowing the independent excitation of *main* and *auxiliary* devices.

The specific advantages of this 'open' approach are numerous, the most significant of which are listed below.

Isolated inputs – As well as allowing the independent stimulus of *main* and *auxiliary* devices, the complete isolation between *main* and *auxiliary* inputs allows independent measurement of each device's input characteristics. For example, one interesting measurement is the dynamic input reflection coefficient of both devices, as a function of input drive. This measurement is important as any significant drive or bias dependent change in s_{11} could obviously have a profound effect on branch gain and hence overall performance. This measurement would not be possible in a closed classical structure.

Control over relative input magnitude - One of the properties that defines the classical Doherty approach is the fixed power division between *main* and *auxiliary* devices. Although the power division ratio can be varied through the use of asymmetric power splitters, this cannot be easily implemented dynamically. Doherty implementations of this type are generally limited to those that can be realised through bias-control. Dynamic control of relative input magnitude allows interesting Doherty implementations such as the input-attenuation approach to be investigated, which would not be possible using a classical structure.

Control over relative input phase - It was considered probable that the very specific relative input phase requirements stipulated by classical Doherty theory could be prohibitive. For example, any drive or bias related phase distortion inherent in the devices used within a Doherty structure would have a profound effect on Doherty performance. Independent input drive allows the perturbation of the relative input phase and investigation of this possibility.

3.3.2 Optimum impedance and expected output power

Before the design of the GaAs Doherty structure could begin, it was important to know the optimum impedance for the devices to be used. From measured DC behaviour (that is presented in Chapter 6), and assuming that $V_{peak}=(V_{dd}-V_k)$, and that $I_{peak}=(I_{max}/2)$, where I_{max} is the maximum useful DC current of the device (as identified on the left-hand y-axis of Figure 153), and assuming a somewhat conservative knee voltage of 1V and a supply voltage (V_{dd}) of 5.5V, the optimum impedance (R_{opt}) for the GaAs MESFET device was calculated using (14).

$$Ropt=\left[\frac{(Vd-Vk)*2}{\mathrm{Imax}}\right]=\left[\frac{(5.5-1)*2}{0.35}\right]=25.7\Omega\approx 25\Omega \qquad (14)$$

For the initial Doherty design, both *main* and *auxiliary* devices were assumed to be driving into a load of R_{opt} at PEP, so both could be expected to deliver the same maximum power. This results in a combined output RF power given by (16).

$$P_{max}=2\left\{\left[\frac{(V_d-V_k)}{\sqrt{2}}\right]*\left[\frac{(I_{max}/2)}{\sqrt{2}}\right]\right\}=2\left\{\left[\frac{(V_d-V_k)*(I_{max}/2)}{2}\right]\right\}=2\left\{\left[\frac{(V_d-V_k)*(I_{max})}{4}\right]\right\} \qquad (15)$$

$$P_{max}=2\left\{\left[\frac{(5.5-1)*(0.35)}{4}\right]\right\}=0.8\ Watt\ (29\ dBm) \qquad (16)$$

3.3.3 Initial measurements

The design strategy for the GaAs MESFET Doherty measurement prototype involved firstly the collection of static and pulsed DC measurements. These are shown later in this thesis and were used to develop the simple model introduced in the previous section and that allowed some initial analysis within *Wavemetrics-IGOR* and *Agilent-ADS* software and simulation environments. This approach allowed the design to commence without placing the devices at unnecessary risk.

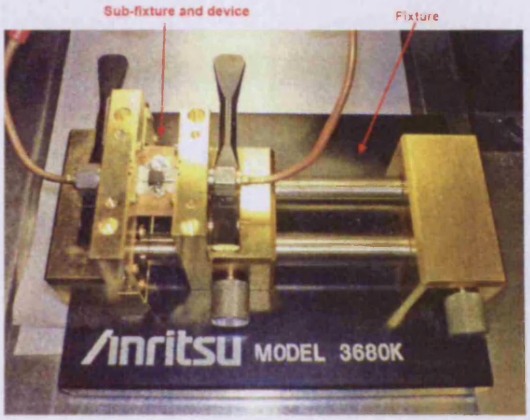


Figure 37 – device and test Fixture

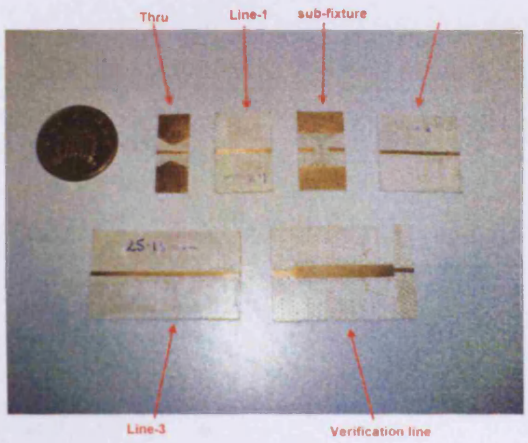


Figure 38 – calibration standards

The *Anritsu*-3680K test fixture and custom built calibration sub-fixture shown in Figure 37, together with the specially fabricated TRL calibration standards shown in Figure 38 were required for both s-parameter and waveform measurements. The use of a TRL calibration [49-51] allowed calibrated reference planes to be defined at the device package plane, which is approximately 1.5 mm away from the device die itself.

3.3.3.1 Bias-dependent behaviour

The graph in Figure 39 shows the gain-phase behaviour of the CF015-11 MESFET device as a function of input drive level and device gate bias measured at 1.8 GHz. This graph is interesting for a number of reasons, one of which is that it is possible to explore device behaviour in the context of both Adaptive-bias (AB) and Input-attenuation (IA) Doherty realisations, where control is achieved using gate/base bias and relative drive magnitude respectively. For example, when considering the AB Doherty, it is possible to define a trajectory of the required adaptive-bias voltage as a function of applied input power, and observe the expected change in gain-phase.

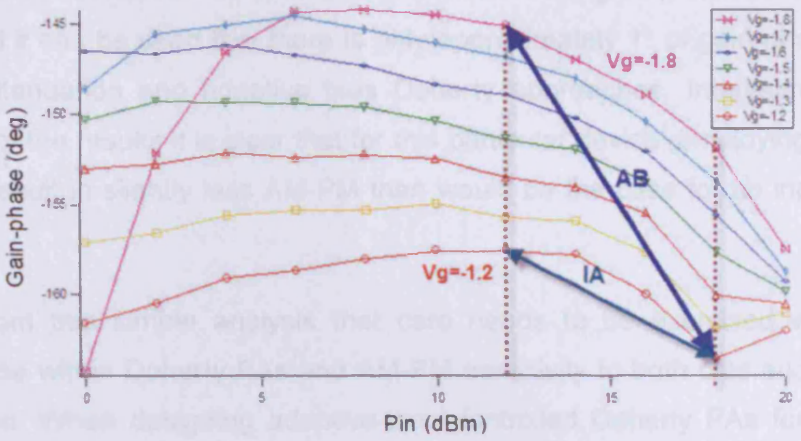


Figure 39 –bias dependent gain-phase(CF015-11 MESFET)

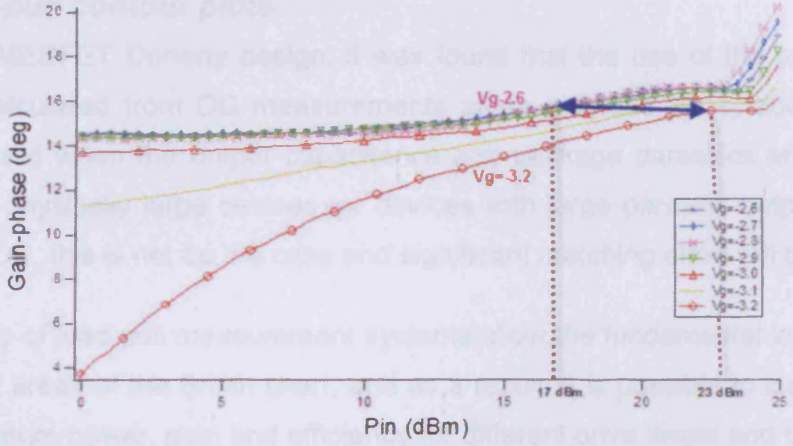


Figure 40 – bias dependent gain-phase (Mitsubishi GaAs FET)

It is clear for instance from the trajectories shown in Figure 39 that when using the CF015-11 MESFET as an *auxiliary* device in an adaptive-bias arrangement, AM-PM conversion of approximately 15° can be expected over the upper 6dB of dynamic range. This is compared to approximately 6° for the same device used in an input attenuation Doherty arrangement, as illustrated by the 'IA trajectory'. This is an effect that clearly has significant implications for the phase-critical Doherty PA, which becomes apparent in later measurements where it is shown for instance that in order to achieve optimum performance, the relative input phase of the stimulus applied to *main* and *auxiliary* devices needs to be dynamically adjusted in response to the magnitude of applied drive.

It must be stated however that this is considered to be a device specific effect. This conclusion has been drawn from the outcome of a similar experiment using similar sized GaAs FET devices supplied by *Mitsubshi*. Over comparable drive and conduction angle

variations, the device can be seen to exhibit a much lower gain-phase variation with drive and bias, and it can be seen that there is only approximately 1° of gain-phase change for both input attenuation and adaptive bias Doherty approaches. Interestingly, on closer examination of the results it is clear that for this particular device, employing adaptive-bias will actually result in slightly less AM-PM than would be the case for an input-attenuation approach.

It is clear from this simple analysis that care needs to be exercised when selecting devices for use within Doherty PAs and AM-PM sensitivity to both bias and drive need to be considered. When designing adaptive-bias controlled Doherty PAs for example, the use of devices with significant bias dependent gain-phase can be expected to result in degraded performance due to phase misalignment at the output.

3.3.4 Load-pull contour plots

In the GaAs MESFET Doherty design, it was found that the use of the optimum design impedance calculated from DC measurements alone provided acceptable results. This can be expected when the output capacitance and package parasitics are known to be small, but for physically large devices, or devices with large parasitic output capacitance such as LDMOS, this is not be the case and significant matching effort will be required.

The availability of load-pull measurement systems allow the fundamental load to be varied over specified areas of the Smith chart, and as a result, it is possible to identify the loads that yield optimum power, gain and efficiency for different drive levels and bias conditions. For design, it is usual to present this information in the form of contour plots such as the examples shown in Figure 41, Figure 42 and Figure 43. Such plots allow intuitive interpretation and the consideration of performance 'trade-off' between the various parameters.

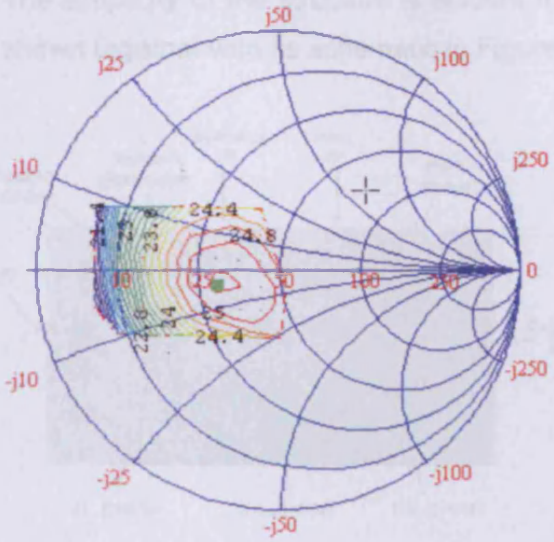


Figure 41 –MESFET P_{out} contours at 1dB compression point (Vg:-1.25V, Vd:5.5V)
Optimum Load for output power = (-0.25,-0.06), P_{out}=25.3 dBm, Efficiency=57.5%

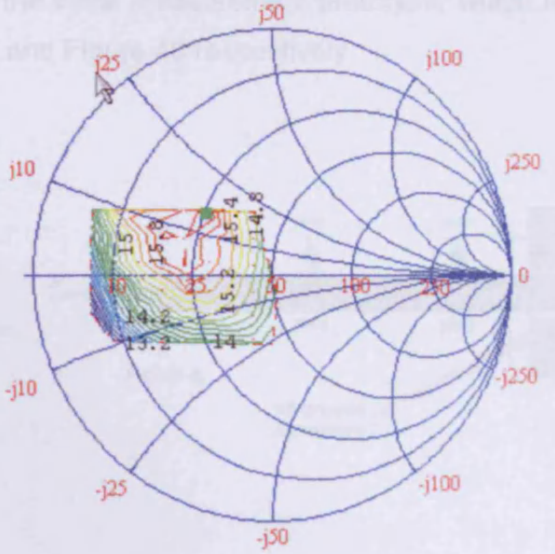


Figure 42 – MESFET Gain contours at 1dB compression point (Vg:-1.25V, Vd:5.5V)
Optimum Load for gain =(-0.28,0.25), P_{out}=24.5 dBm, Efficiency=62.7%

From Figure 41 for instance, it is clear that the fundamental load impedance that yields maximum output power for the GaAs MESFET devices used in the initial realisation is very close, both in terms of reactive and real components to the 25Ω predicted by earlier DC characterisation.

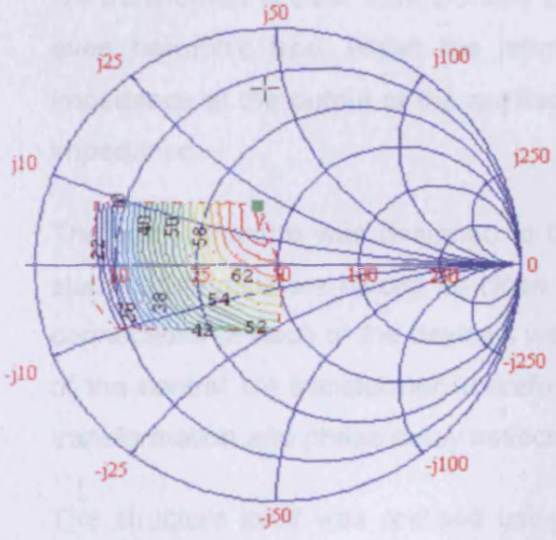


Figure 43 –MESFET Efficiency contours at 1dB compression point (Vg:-1.25V, Vd:5.5V)
Optimum Load for efficiency = -(0.08,0.25), P_{out}=24.3 dBm, Efficiency=71.1%

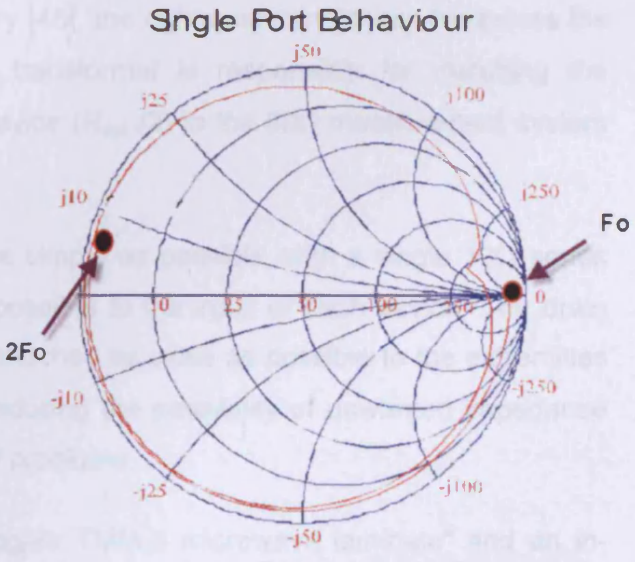


Figure 44 – one-port measurement between 1.8 and 3.6 GHz, looking into output of structure

The simplicity of the structure is evident from the initial measurement prototype, which is shown together with its schematic in Figure 45 and Figure 46 respectively.

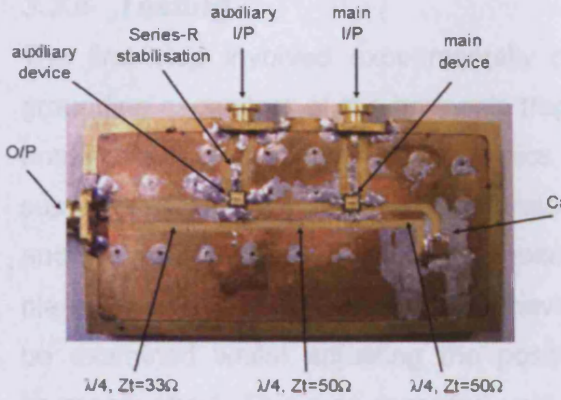


Figure 45 – Fabricated Doherty

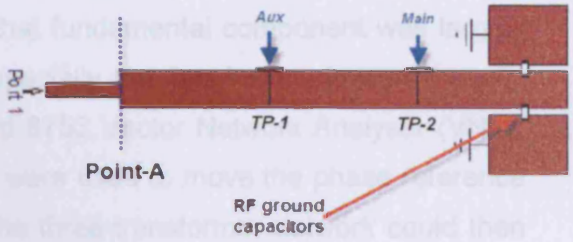


Figure 46 – layout of GaAs Doherty

3.3.5 Fabrication

The GaAs Doherty design for R_{opt}=25Ω was convenient as it allowed for an extremely simple and discontinuity-free output impedance transformation network, consisting of three identical λ/4 transformers each with a characteristic impedance (Z_T) of 25Ω. These were connected in series with the active devices attached directly to either end of the centre transformer, as shown in Figure 45 and Figure 46. Whereas the role of the centre λ/4 transformer is clear from Doherty theory [45], the rightmost transformer comprises the even harmonic trap, whilst the leftmost transformer is responsible for matching the impedance at the output of the *auxiliary* device (R_{opt} /2) to the 50Ω measurement system impedance.

The input structure was designed to be as simple as possible, with a single 10Ω series stabilisation resistors placed as close as possible to the input of each device. The drain connections of each of the device's were attached as close as possible to the extremities of the central λ/4 transformer, therefore reducing the possibility of unwanted impedance transformation and phase delay associated problems.

The structure itself was realised using Rogers TMM-3 microwave laminate[8] and an *in-house* milling process. The necessary device grounding was achieved using solder through ground-vias situated as close as possible to each active device, and the grounding capacitors of the harmonic trap shown in Figure 46. The rear of the board was

[8] The laminate used has a dielectric possessing εr=3.27 and T=30mil, with copper thickness=17.5 um.

in turn soldered to a 1 cm thick brass chassis in order to offer both physical protection and an effective ground.

3.3.6 Testing

The first step involved experimentally determining the value and position of the RF grounding capacitors of the harmonic trap such that fundamental component was largely unaffected, whilst even order harmonics, and especially the 2nd harmonic were heavily suppressed. Using a single-port calibrated Agilent 8753 Vector Network Analyser (VNA), and with reference to Figure 46, port extensions[9] were used to move the phase reference plane from Port-1 to *point-A*. The behaviour of the three-transformer network could then be examined whilst adjusting the position and value of the capacitors providing the harmonic short. This was repeated until the required behaviour was achieved, which is specifically a high impedance at the fundamental and low impedance at the second harmonic. The measured results in Figure 44 show clearly how at the fundamental frequency, the capacitive short is transformed to a near open, and at the second harmonic to a near short. As the transforming structure is so simple, it was reasonable to assume that the same capacitive short would be transformed to an open at the output of the *main* device (*TP-1*), on to a short at the output of the *auxiliary* device, and finally back to an open at *point-A*. Using the same rationale, it was also considered fair to assume that at the second harmonic, the capacitive short would be transformed to a short at the *main* device, to a short at the *auxiliary* device output, and again to a short at *Point-A*.

So far in this chapter, all discussion has related to the GaAs Doherty measurement structure. The GaN Doherty (R_{opt}=50Ω) is discussed in detail in Chapter 6, and is very similar in design to the GaAs Doherty (R_{opt}=25Ω) structure. A slightly different approach was used when designing the this structure which involved injecting RF energy into the *main* and *auxiliary* device launch points of the *main* transforming transmission line structure, identified by labels *TP-1* and *TP-2* in *Figure* 46.

This was firstly achieved using a crude air-bridge structure in place of each device, with reasonable results. Improved results were achieved however by fabricating a small 50 Ω RF probe for use with the VNA. This involved using a short length of semi-rigid cable with the centre-conductor protruding slightly. As this was a good 50Ω line, the associated delay could be reliably removed from the measurement using an appropriate port extension, and the extra length of the protruding centre conductor (<1mm) had little effect at the frequencies of concern. This approach was found to be very effective in measuring the

[9] A port extension is a function of the 8753 VNA that allows the phase reference of the defined calibrated reference plane to be electrically shifted, relative to the calibrated reference plane.

fundamental and harmonic impedances that were presented by the passive structure, to both *main* and *auxiliary* devices.

The markers in Figure 47 shows the measured fundamental impedance seen by the *main* device at *TP-2* when the structure output was terminated into 50Ω, and the shorting capacitor placed in its final, optimum position. This was measured to be 93 + j12Ω. Ideally for this structure, an expected load of 50Ω will be transformed to $R_{opt}/2=25\Omega$ at the *auxiliary* device (*TP-1*), and then to $2R_{opt}=100\Omega$ at the *main* device (*TP-2*), so this is reasonably close to the design value.

Figure 48 shows the second harmonic impedance as seen by the *main* device at *TP-2*, which was measured to be 5.6 + j9.6Ω.

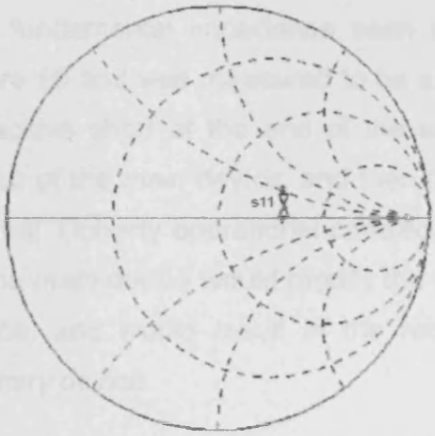


Figure 47 – s11 as seen by Main at 1.8 GHz

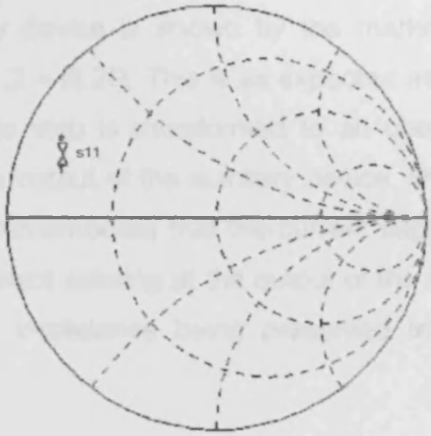


Figure 48 – s11 as seen by Main at 3.6 GHz

Although not the ideal short, this was considered as a reasonable result at this stage. The behaviour is further illustrated in Figure 49 which shows the transmission characteristics between the *main* device and the output port are shown. Marker (m1) identifies the point corresponding to the fundamental frequency of 1.8GHz, and shows approximately 1 dB of insertion loss, whilst marker m2 shows the second harmonic will be suppressed by approximately 15 dB.

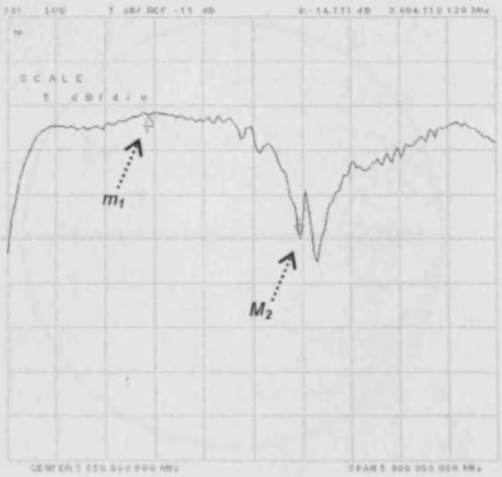


Figure 49 – s21 between Main device and output port at 1.8 GHz and 3.6 GHz (m1 and m2)

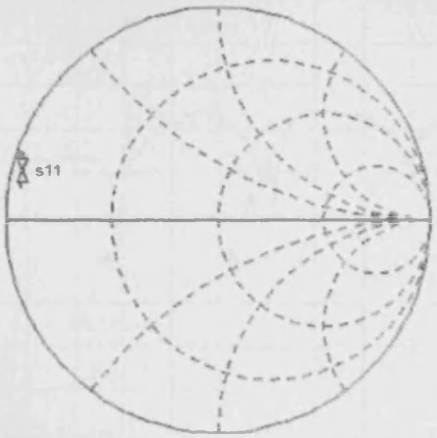


Figure 50 – s11 seen by auxiliary device at 1.8 GHz

The fundamental impedance seen by the *auxiliary* device is shown by the marker in Figure 50 and was measured to be a near short at 1.2 + j6.2Ω. This is as expected as the capacitive short at the end of the second harmonic stub is transformed to an open at output of the *main* device, and then to a short at the output of the *auxiliary* device. Under 'normal' Doherty operational conditions, it must be remembered that the current supplied by the *main* device would modify the passive impedance existing at the output of the *main* device, and would result in the required Doherty impedance being presented to the *auxiliary* device.

At the second harmonic, the transformation network effectively becomes a series of λ/2 transformers where the short caused by the capacitor is transformed to a short at the *main* device and then on to a further short at the *auxiliary* device output. This effect is illustrated by markers m1 and m2 in Figure 52.

The second harmonic short presented to the *auxiliary* device is shown again in Figure 51 and measured to be 6 + j13.7Ω. Although this second harmonic short is degraded in comparison to that offered to the *main* device, it is still considered adequate in offering suitable suppression to the even-order harmonics.

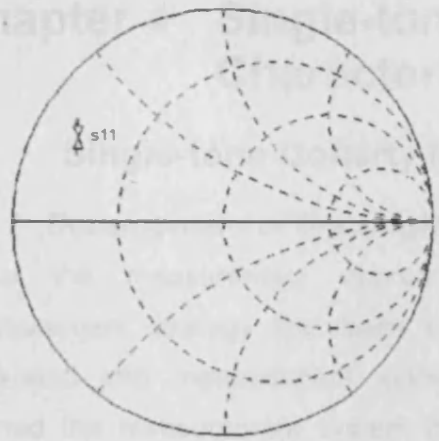


Figure 51 – s11 as seen by auxiliary at 3.6 GHz

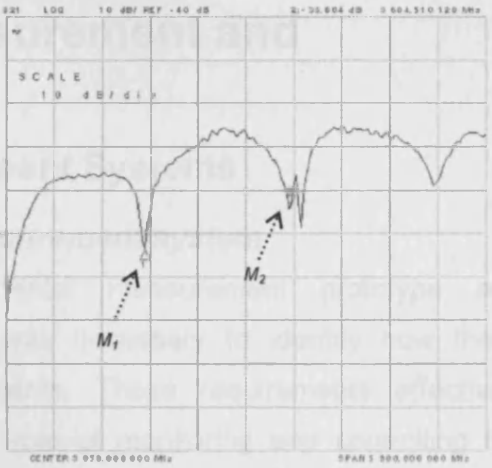


Figure 52 – s21 between auxiliary device and output port at 1.8 GHz and 3.6 GHz (m1 and m2)

3.4 Measurement Strategy

Once the measurement approach had been generally specified, some thought was given to the measurement system that was to surround, measure and control the experimental prototype, as well as to the various types of measurement that needed to be supported. This was a necessary step before realising any measurement system due to the large implications on measurement architecture.

An initial strategy was defined that involved two distinct phases of work. The first phase involved conducting simple, single-tone measurements of classical, input-attenuation and adaptive-bias Doherty structures. This would begin with manual control of the measurement environment using variable attenuators and variable phase delays, with the initial emphasis on the identification of any Doherty behaviour in the simple prototype. If successful, automated control of the measurement system would be implemented allowing more detailed measurements, perturbation analysis and optimisation.

The early assumption was that the first phase would lead to an increased understanding of fundamental Doherty interaction, as well as identifying optimisation strategies that would offer an improved efficiency and linearity trade-off in the Doherty PA. To allow the evaluation of linearity, a second phase of work was envisaged that involved developing the measurement system to support modulated behaviour.

Chapter 4 Single-tone Measurement and Characterisation

4.1 Single-tone Doherty Measurement Systems

4.1.1 Development of the single-tone measurement system

Once the measurement approach, experimental measurement prototype and measurement strategy had been specified, it was necessary to identify how these translated into measurement system requirements. These requirements effectively defined the measurement system that had the role of monitoring and controlling the behaviour of the prototype. These are identified in the following paragraphs.

4.1.1.1 Generation of main and auxiliary excitation signals

In order to support the dual-input measurement prototype, two independent, phase-coherent excitation signals were required with adjustable relative phase and magnitude. This flexibility allowed the required conditions needed for Doherty behaviour to be easily established and importantly, allowed perturbation of relative input phase and magnitude and the investigation of sensitivities of the Doherty structure together with various optimisation possibilities. These excitations were initially generated simplistically using a single RF source, power dividers, line stretchers and variable attenuators, and later, using two software controlled, independent, phase-coherent RF signal sources.

4.1.1.2 Provision of required bias environment

Precise control and measurement of drain and gate DC bias for both *main* and *auxiliary* devices was also necessary. Whereas the structure shared a common drain connection, independent control of gate bias was essential as for some Doherty implementations, the *auxiliary* gate bias needs to be changed dynamically with increasing input drive. This required an accurate, programmable DC power supply capable of measuring voltage and current, connected using both commercially available and custom, in-house designed bias networks.

4.1.1.3 Measurement of power spectrum

In order to calculate the important, gain and efficiency parameters of the Doherty structure it was necessary to measure the fundamental signal components within output power spectra. This was achieved this using a spectrum analyser.

4.1.1.4 Software control

Although it was possible to conduct simple measurements manually, measurement complexity, repeatability and required measurement time meant that an alternative approach was necessary that made use of software control and automation. This required

all key instruments to be connected to a control PC using the IEEE-488 General Purpose Information Bus (GPIB).

4.1.2 Looking for classical Doherty behaviour

Following fabrication of the early measurement prototype, the first measurements involved simply trying to detect what was at the time 'illusive' Doherty behaviour. Although the prototype Doherty structure was equipped with multiple input ports and designed to accommodate a number of Doherty implementations, for simplicity initial measurements were limited to using a single microwave source to synthesise the necessary phase coherent drive signals for the Doherty structure. This arrangement is shown in Figure 53.

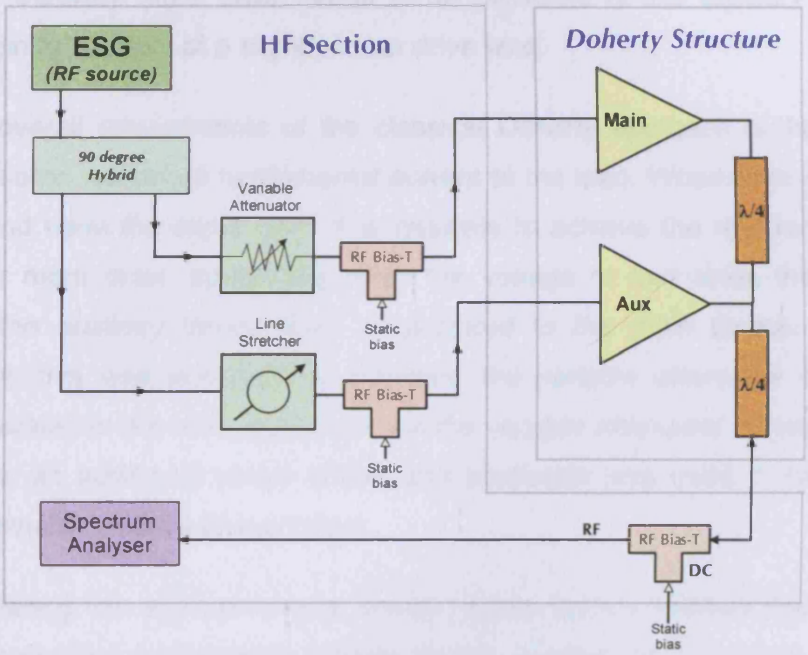


Figure 53 – simple Doherty measurement set-up

In this measurement system, a 90° hybrid coupler was used to split the CW power generated by the Agilent E-series Signal Generator (ESG) into two, equal magnitude phase coherent excitation signals, with a relative phase difference of 90°. In order to allow a degree of relative phase and magnitude control between the two inputs, a variable attenuator and variable phase-shifter (line stretcher) were inserted into *main* and *auxiliary* branches respectively. Commercial bias networks possessing a low-frequency bandwidth of 400MHz were used to supply DC to both gate and drain bias connections, with the structure output connected through a 20 dB attenuator to a spectrum analyser. All RF connectivity was via semi-rigid cable, which was necessary in order to minimise relative phase variation between inputs.

4.1.2.1 Measuring Doherty behaviour ~ a pseudo-classical approach

The simplest realisation of Doherty, i.e. the classical [21] or static offset-bias approach was employed as a means of validating the measurement approach, and for completeness is briefly discussed here. This realisation generally requires *main* and *auxiliary* devices to have dissimilar gain. This immediately presents a challenge when attempting to realise the classical, Doherty using the measurement prototype as this structure was designed to use identical *main* and *auxiliary* devices. The consequence of using the simple measurement structure in this way is that only a limited-performance form of classical Doherty is possible [22], which is achieved through modifications to both the classical, symmetrical input drive power division ratio, and the *auxiliary* bias condition. Specifically, relatively more drive needs to be delivered to the *auxiliary* device, which needs to begin to conduct at a slightly lower drive level.

One of the overall requirements of the classical Doherty approach is that each device delivers the same maximum fundamental current to the load. When both devices are the same size and have the same gain, it is possible to achieve the required behaviour by arranging for more drive, specifically twice the voltage or four times the power, to be diverted to the *auxiliary* device than is delivered to the *main* device. For the initial measurement, this was achieved by adjusting the variable attenuator so that 6dB of attenuation existed in the *main* input path. As the variable attenuator introduced additional phase delays, an additional phase shifter and attenuator was used to compensate and restore the required relative phase offset.

When considering this approach more closely, it was quickly realised that the maximum available unsaturated fundamental current for the *auxiliary* device would be lower than that of the *main* device [52], due to the reduced conduction angle (class-C) mode of operation.

In order to overcome this problem, a compromise solution was adopted that involved adopting a lower than usual value of I_{Max} for both devices, corresponding to the maximum *auxiliary* fundamental current at maximum drive. For the *main* device, this involved operating some way within its maximum capability and hence at reduced Power Utilisation Factor (PUF). A similar method of employing similar sized devices in a classical, offset-static-bias Doherty configuration has since been documented in [22] and is termed '*Doherty-Lite*'.

For example, the maximum theoretical fundamental current expected from the *main* class-B device will be $I_{Max}/2$, where I_{Max} is the maximum device saturated DC current. The

class-C biased *auxiliary* device will not be able to deliver this and typically will be able to source a maximum fundamental current of $I_{Max}/2.2$, or 45% of I_{Max}. In order to adhere to classical Doherty theory and maintain the same maximum current values at maximum input drive, it is therefore necessary to use a larger *auxiliary* device, or if this is not possible as is the case here, to somehow limit the maximum *main* device fundamental current to the lower of these two values, i.e. $I_{Max}/2.2$.

The effect this limitation has on Doherty behaviour is illustrated in Figure 54 which shows ideal *main* and *auxiliary* fundamental current transfer characteristics as a function of Doherty input voltage (V_{in}), for both limited-classical and normal classical approaches. The reduction in *main* and *auxiliary* current is evident through the shift from point-A to point-B maximum current values.

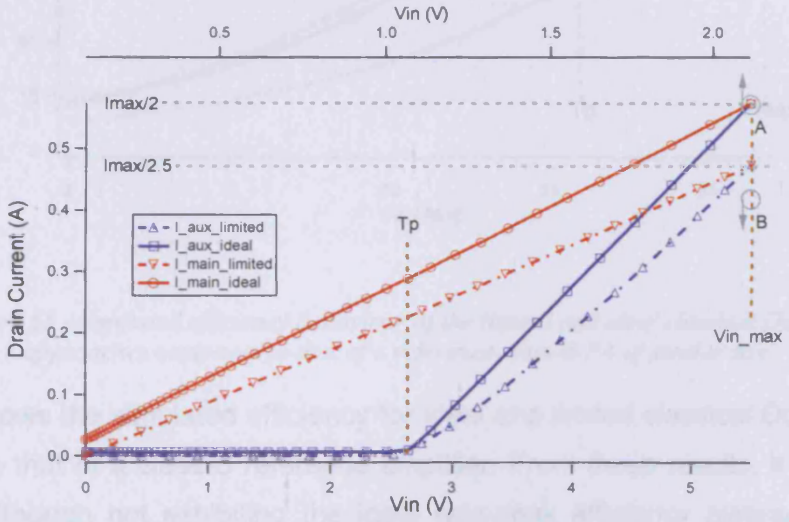


Figure 54 –simulated fundamental current behaviour between the limited and ideal classical Doherty approaches

The implications of using this approach are reduced maximum output power coupled with degradation in overall device efficiency due to reduced main device voltage swing. Although it is theoretically possible to recover some performance by moving the transition point, this involves increasing the load impedance. This was unfortunately not an option when using this measurement structure as the passive impedance environment had already been fixed during the design phase, and was based on the value of R_{opt} for the device used. R_{opt} had also been used to specify other critical circuit parameters such as the characteristic impedance of the *main* transforming line, together with other impedance transforming elements of the circuit.

In order to achieve optimum Doherty operation within the limited available structure, a number of steps were necessary. Firstly, the already asymmetrical input power split (6dB) needed to become even more asymmetrical (7dB) and was re-adjusted to allow still more drive to be delivered to the *auxiliary* device to compensate for its reduced relative gain. In addition to this, the gate bias voltage applied to the *auxiliary* device was adjusted to cause conduction at a slightly reduced drive level.

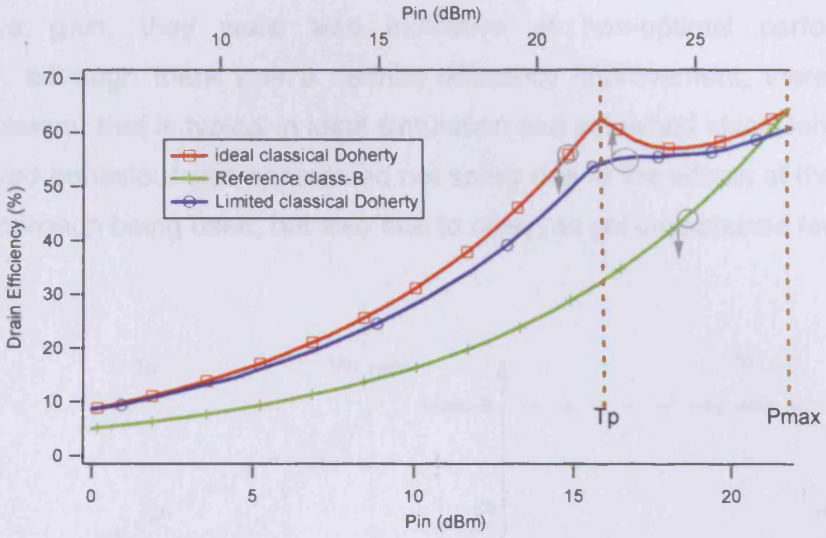


Figure 55 –simulated efficiency behaviour of the limited and ideal classical Doherty approaches compared to that of a reference class-B PA of similar size.

Figure 55 shows the simulated efficiency for ideal and limited classical Doherty structures together with that of a class-B reference amplifier. From these results, it is clear that the approach, although not exhibiting the ideal twin-peak efficiency plateau, is capable of producing relatively good and certainly identifiable Doherty plateau behaviour. This analysis was effective in demonstrating that the limited classical Doherty approach could be used at least as a proof of concept, and as a suitable vehicle through which it could be shown that the structure was capable of producing Doherty behaviour. Having said this, the approach would almost certainly not be viable in a commercial realisation due to the reduction in PUF and waste of *main* device periphery.

Using this approach, a typical classical Doherty measurement involved setting the bias conditions such that the *main* device was established in class-B and the *auxiliary* device in the required degree of class-C, such that *auxiliary* conduction commences at the transition point. The input drive relative power ratio was then checked using a power meter, and only then connected to the Doherty structure. The source power would then be increased to some value close to its pre-defined maximum, and the phase delay in the *auxiliary*

signal path adjusted until maximum power was observed, indicating the optimum relative input phase. The Doherty measurement prototype was then ready for initial characterisation using simple P_{in} / P_{out} sweep measurements,.

4.1.3 Investigating other Doherty implementations

Although the measurement results demonstrated the definite presence of Doherty behaviour through the observation of improved efficiency in the presence of non-compressive gain, they were also indicative of non-optimal performance. More specifically, although there was a definite efficiency improvement, there was no clear efficiency plateau that is typical in ideal simulation and published ideal Doherty behaviour. The observed behaviour was considered not solely due to the effects of the simple limited classical approach being used, but also due to other, as yet unexplained factors.

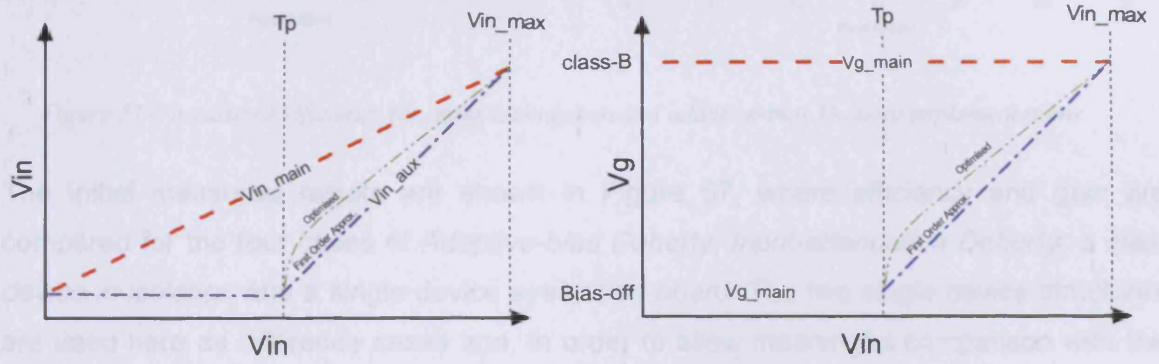


Figure 56 – profiles for input-attenuation and adaptive-bias Doherty implementations

In order to investigate these observations and to begin to consider other, more interesting Doherty realisations, a change to the measurement approach was necessary. Specifically, the measurement system needed to be able to support the dynamic modification of relative input magnitude and relative gate bias in order to implement input-attenuation and adaptive-bias Doherty realisations respectively.

Whereas in previous measurements, both of these parameters remained fixed over the entire operational dynamic range, there was now a need for them to become dynamic functions of input drive level. Simple classical Doherty design theory [21] was used to derive the first-order approximations of input-attenuation and adaptive-bias profiles, which were then applied manually at each point in the power sweep. These profiles are discussed in more detail in Chapter 2 and are shown in Figure 56, where both ideal asymptotic and optimised profiles are shown. In both of these cases, the optimised

profiles are effective in compensating for the 'soft' turn-on characteristic that is typical of the devices used.

It was evident that the manual adjustment at each point in the measurement was a very tedious process, but the simple approach was effective in providing the first comparison of two variations of the classical Doherty approach: input-attenuation and adaptive-bias.

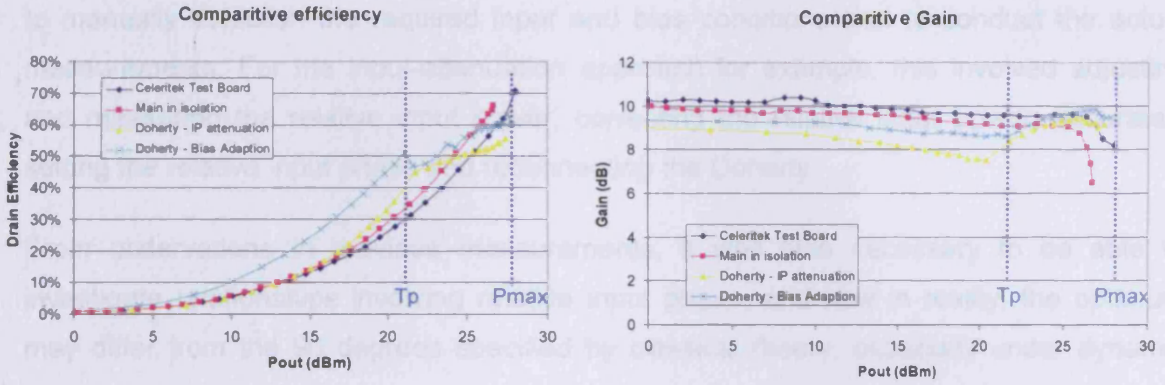


Figure 57 – measured efficiency for input-attenuation and adaptive-bias Doherty implementations

The initial measured results are shown in Figure 57, where efficiency and gain are compared for the four cases of *Adaptive-bias Doherty*, *Input-attenuation Doherty*, a *main device in isolation* and a single device *evaluation board*. The two single device structures are used here as reference cases and, in order to allow meaningful comparison with the two-device Dohertys, the output powers have been normalised by scaling the single device output power by a factor of two. The *main device in isolation* case consists of the measurement prototype without the *auxiliary* device being physically present and is useful in illustrating the required low power behaviour of the different Doherty structures.

Doherty behaviour is clearly evident in the form of enhanced efficiency over 6dB of dynamic range, in the presence of non-compressive gain for both Doherty approaches. The efficiency of the input-attenuation approach can be seen to be generally well behaved, but degraded in comparison to the adaptive-bias approach. This is anticipated due to the presence of a small quiescent current when using the input-attenuation approach, and the fact that the *auxiliary* device is biased in shallow class-B, and conducts throughout the entire region of dynamic range below the transition point. The adaptive-bias approach exhibits the most impressive efficiency up to the transition point, which then becomes erratic between the transition point and the point of Peak Envelope Power (PEP). There was one critical observation for the adaptive-bias approach, where it was noticed that the efficiency could be improved between the transition point and PEP by

making small manual adjustments in the relative input phase using the line stretcher in the *auxiliary* input signal path. This, together with the generally well behaved efficiency characteristic of the input-attenuation approach suggested that there was some form of dependency on relative input phase that was interesting and needed further investigation.

4.1.3.1 Automation and the control of relative input phase

One of the major disadvantages of the previous approach was the excessive time needed to manually establish the required input and bias conditions and to conduct the actual measurements. For the input-attenuation approach for example, this involved adjusting and measuring the relative input power, correcting the relative input power, accurately setting the relative input phase and reconnecting the Doherty.

From observations in previous measurements, it was also necessary to be able to investigate relationships involving relative input phase, and how in reality, the optimum may differ from the 90 degrees specified by classical theory, especially under dynamic drive and bias conditions.

With these requirements in mind, the measurement system was enhanced to allow much more detailed investigations into Doherty behaviour. Specifically, this involved the systematic perturbation of relative input phase, relative input magnitude and relative bias profile, together with the measurement of the effects of these perturbations in terms of key performance parameters including drain efficiency, gain, and AM-PM conversion. Performing these perturbations manually, using the existing arrangement was not a practical option and automation of the process became the only realistic option. This involved the replacement of manually adjustable phase and magnitude devices with programmable, phase-coherent instruments, and the development of a software based control environment.

4.1.3.2 Hardware changes

With reference to Figure 58, the line stretcher (phase shifter), variable attenuator and power divider were removed and replaced with two, independent microwave signal generators, ESG-1 and ESG-2. It was essential that the independent *main* and *auxiliary* RF signals applied to the measurement prototype were phase coherent, and this was achieved using the standard 10 MHz instrument synchronisation link available on these instruments. It must be stated that the viability of achieving precise phase coherence of two microwave frequency sources using a relatively low frequency (10MHz) synchronisation signal was an unknown quantity. It was understood for instance that any

phase noise, jitter or drift in the synchronisation signal would be transformed into much larger errors in the high frequency signal, so caution was exercised.

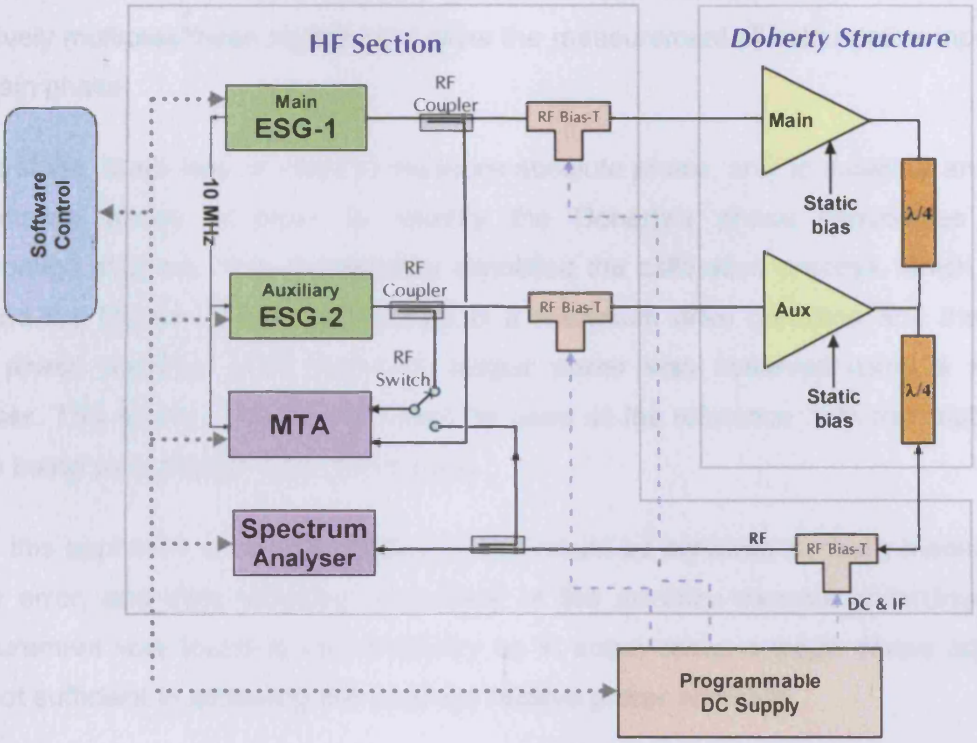


Figure 58 – multi-port measurement system

Achieving phase synchronisation is only half of the problem however and the standard 10MHz Phase Locked Loop (PLL) method discussed is only effective in locking the phase of the microwave sources at some arbitrary relative phase. It is necessary therefore to perform an additional step in order to align the relative input phase, following the synchronisation phase. In order to perform this alignment of the two RF signals, it was necessary to place 20 dB directional couplers at each input port to monitor the relative input phase. This measurement could be achieved using a Vector Network Analyser (VNA), but for this system, a Microwave Transition Analyser (MTA) was used. The MTA is essentially an RF oscilloscope with two coherent measurement channels, capable of measuring frequency components up to 40 GHz. The instrument is well-proven and is detailed in [53]. For this discussion, it can be assumed that the instrument can very accurately measure relative phase and absolute spectral power presented to its two channels, especially at the relatively low CW frequency of 1.8 GHz.

A further 20 dB directional coupler was included at the output of the measurement prototype to allow the measurement of any AM-PM conversion. As the MTA is a two channel instrument, it was necessary to include and interface some RF switching to effectively multiplex these signals and allow the measurement of both relative input phase and gain phase.

At this stage, there was no need to measure absolute phase, only to measure and control the relative phase in order to identify the Doherty's phase sensitivities through perturbation analysis. This dramatically simplified the calibration process, which typically involved the Doherty being established in a maximum drive condition and the relative input phase adjusted until maximum output power was observed using a spectrum analyser. This relative phase would then be used as the reference, with the relative input phase being varied either side of this point.

Using this approach, a desired relative phase would be achieved by firstly measuring the phase error, and then adjusting the phase of the *auxiliary* stimulus accordingly. A re-measurement was found to be necessary as in some cases a single phase adjustment was not sufficient in achieving the required relative phase accuracy.

4.1.3.3 Software environment

Development of a software environment was necessary to support system calibration, measurement control, data presentation and a user interface. As well as the control software, extensive post-processing software was necessary to analyse and interpret the measured data, allowing for example derivation of optimum conditions and presentation of the data in meaningful formats.

IGOR, a scripting language produced by *WaveMetrics* [26] was used to develop this functionality. This software platform offered a number of advantages at the time it was required, and was used extensively by the research group, offering good instrument communication interfaces through GPIB connectivity.

Once the adopted phase synchronisation and alignment approach had been verified (see section 4.1.5), the measurement system was configured as shown in Figure 58. Using this approach, significant advances in Doherty measurements were possible. Perturbation of parameters such as relative input phase quickly led to large amounts of generated measurement data, and following some experimentation, it was found that the most effective way of presenting this information was graphically, through the use of 3-dimensional surface plots. Some examples of this approach are shown in the efficiency and gain surfaces of Figure 59 and Figure 60, which show that sweeping the relative input

phase at each point in a power sweep measurement uncovered some interesting relative phase dependent behaviour. It is clear for instance that for these initial GaAs FET structures, performance, and specifically gain and efficiency are very much functions of relative input phase.

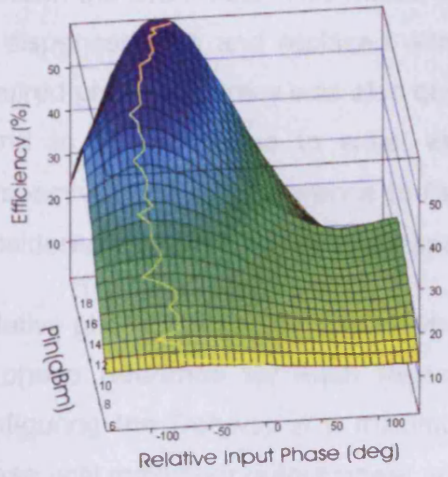


Figure 59 – efficiency vs. P_{in} vs. relative input phase

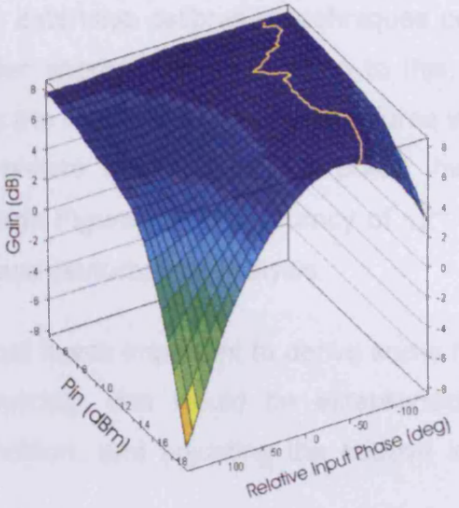


Figure 60 – gain vs. P_{in} vs. relative input phase

To highlight this behaviour, contours[10] of maximum efficiency and constant gain have been added to the surface plots of Figure 4 and Figure 3 respectively. The contours show how the relative input phase for maximum efficiency and constant gain deviate significantly in the high power region of operation. These results clearly show that in order to achieve maximum efficiency performance, it would be necessary to dynamically adjust the relative input phase such that it followed the identified contour, which for this particular device varies by up to 30° [31].

These results are discussed in detail later in this chapter, and are more typical for Doherty structures employing adaptive-bias control, which was seen to be the case in both GaAs MESFET and GaN Doherty measurement prototypes.

[10] Note that these contours are quite noisy compared to the relatively smooth surfaces. This is due to the fact that the contours have been extracted from the actual measurement data, typically 20x20 arrays of measured points, and the surfaces have been smoothed through some degree of interpolation. The contour 'noise' should NOT be interpreted as actual device behaviour.

4.1.4 Calibration and verification

4.1.4.1 System calibration requirements

Unlike the majority of measurement systems used by the research group, the Doherty measurement system calibration requirements were quite relaxed for a number of reasons. Initially, the interest was in only relative and not absolute phase relationships between the two inputs. This meant that the usual, extensive calibration techniques could be dispensed with and replaced with much simpler approaches. In addition to this, the required phase accuracy was also quite relaxed as the measured Doherty structures were found to be insensitive to small variations in relative input phase. To place this in perspective, and with reference to Figure 70 through Figure 75, an accuracy of ±2° was considered adequate for the necessary alignment and perturbation analysis.

Relative phase calibration is somewhat arbitrary, but it was important to derive some form of phase reference for each measurement. Typically, this would be established by configuring the Doherty in a maximum drive condition, and adjusting the relative input phase until maximum output power was observed.

In terms of magnitude accuracy, the power levels delivered to *main* and *auxiliary* Doherty inputs had a tendency to vary over time; an effect that was largely due to the inclusion of the necessary drive amplifiers. Although this drift could be minimised by allowing the amplifiers to stabilise, as well as the use of Automatic Gain Control (AGC) feedback, it was found that the required accuracy could not be guaranteed. An approach was adopted where the fundamental power incident at both *main* and *auxiliary* inputs was measured and corrected in advance of each measurement. This calibration step involved attaching a calibrated power meter to the *main* and *auxiliary* ports of the measurement system, and measuring the difference between the coupled power delivered to each MTA channel, and the incident power delivered to *main* and *auxiliary* ports of the measurement system. Simple error terms could then be calculated that allowed accurate measurement and correction of the powers incident to each port.

4.1.5 Validity of phase synchronisation approach

As mentioned earlier, the validity of the adopted approach of phase-synchronising high frequency signals using a relatively low frequency synchronisation signal is questionable. Although the phase measurement accuracy of the MTA is well established [53], the ability of the standard 10MHz synchronisation approach to maintain phase-lock of two high-frequency sources was a concern. This phase stability is critical, and must be achieved with sufficient accuracy and longevity for any measurement, following phase alignment to

be considered as accurate. It was therefore considered necessary to experimentally test this assumption.

In order to perform this experiment, two microwave sources ESG-1 and ESG-2 were synchronised via the 10MHz link with their outputs connected via semi-rigid coax to a 90 degree hybrid coupler. In order to observe the effects of phase noise and jitter at a relevant frequency, the CW frequency and power of each instrument was set to 2 GHz and -3dBm respectively. The relative phase was then adjusted until the combined voltage components cancelled, where the measured output power of the coupler reached a minimum. Power measurement was then recorded over a duration of 90 seconds in order to observe any effect of phase drift.

In order to place these results into perspective and to clarify the relationship between observed minimum power and phase accuracy, a simple ADS simulation was run to obtain the ideal cancellation profile. The simulated results are useful as a reference and from Figure 61, indicate for example that assuming ideal components, a relative phase accuracy between the two sources of approximately +/-2 degrees is required in order to obtain a cancellation null of -40dB. By overlaying the simulated and measured results, an indication of the effectiveness of the synchronisation approach emerges. It is clear for instance that the minimum measured power is -40 dB, so it is reasonable to assume that this approach, at 2GHz has an accuracy of ±2°.

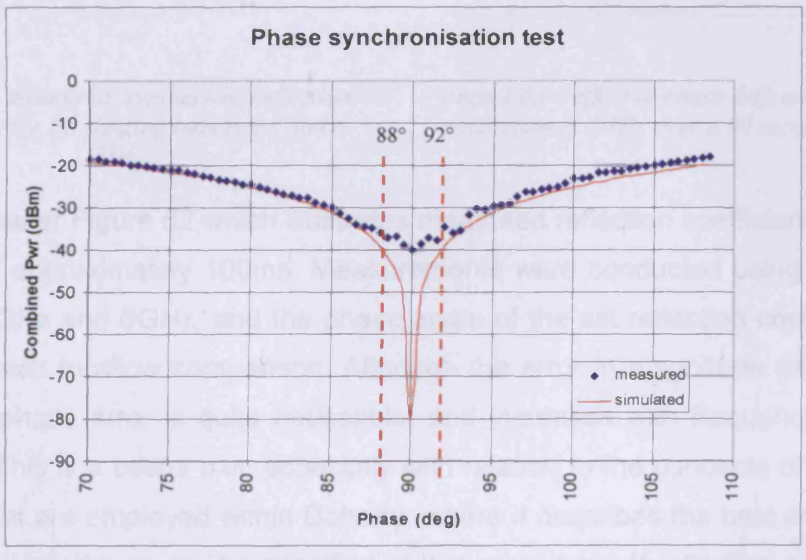


Figure 61 – simulated and measured signal cancellation

As a second, more reliable check, a simple load-pull arrangement was established involving a single ESG driving directly into port-1 of an Agilent 8753 VNA. The instruments were synchronised in the usual way using a 10 MHz synchronisation link, and the VNA set to CW (time sweep) mode with amplitude and frequency matching that of the ESG. This is a much more relevant test for the Doherty measurement system, as this involves simplistically simulating the behaviour of the *auxiliary* device in load-pulling the *main* device.

By measuring un-calibrated s11, and adjusting the ESG phase and magnitude, a stable and specific reflection coefficient was synthesised, in this case a short circuit ($\Gamma=1\angle 180°$). Multiple, time swept measurements were then taken over a period of 90 seconds to investigate the effect of phase jitter and drift in the 10 MHz synchronisation signal.

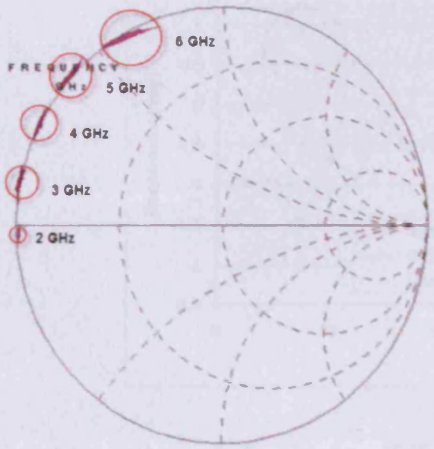


Figure 62 – measured, synthesised reflection coefficients for Fc ranging between 1 and 6 GHz.

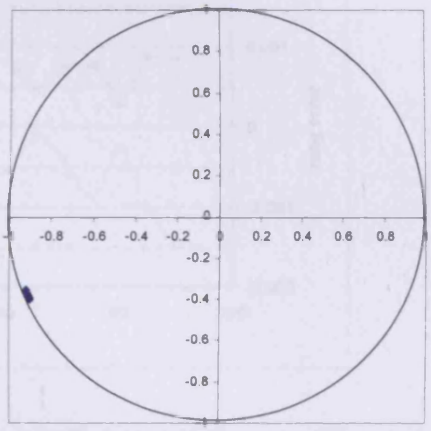


Figure 63 – effect of phase drift on reflection coefficient at 2GHz over a 90 second period.

Firstly, consider Figure 62 which illustrates measured reflection coefficients observed over a period of approximately 100ms. Measurements were conducted using five frequencies between 2GHz and 6GHz, and the phase angle of the set reflection coefficient has been offset for each to allow comparison. Although the error in magnitude can be seen to be small, the phase error is quite noticeable, and increases with frequency, which can be expected. This is a useful plot, especially with relation to the concepts of active harmonic load-pull that are employed within Doherty, where it describes the best accuracy to which a harmonic impedance can be specified at this magnitude of reflection coefficient. This is the best case however as it is only a measure of random error over a short time period of 100 ms, and ignores for instance the effect of phase drift.

Considering more closely the effects of drift, Figure 63 shows the results of a measurement where a reflection coefficient has been set, and a measurement taken every 5 seconds over a period of 90 seconds. The random noise, as observed above, is removed from each individual reflection coefficient measurement through averaging, and then plotted over a period of 90 seconds. This gives an effective measure of drift in both phase and magnitude of reflection coefficient at 2 GHz. The same data is presented in rectangular form in Figure 64, where the phase can be seen to be drifting by approximately 2 degrees/minute at 2 GHz, which translates to approximately 6 degrees/minute at 6 GHz. The magnitude has remained static with a drift of approximately 0.001.

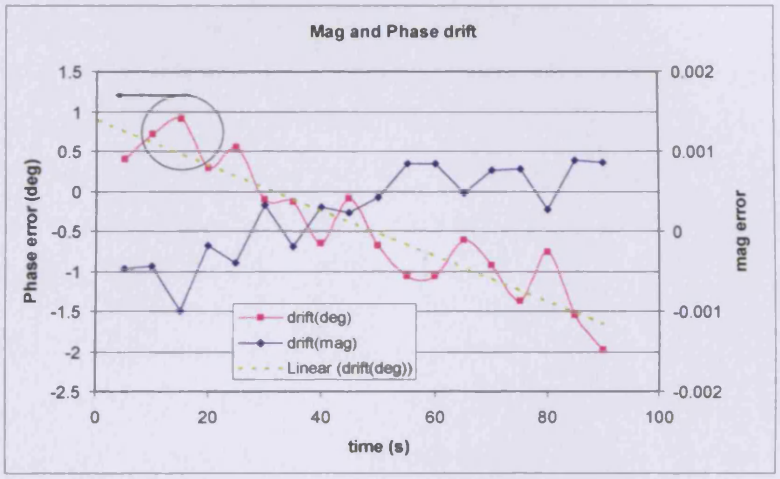


Figure 64 – analysis of effect of phase drift on reflection coefficient at 2GHz over a 90 second period.

To finalise this experiment, the random phase error results (excluding drift) are analysed statistically for each frequency, and presented in Table 1. At 2 GHz, it can be seen that a phase error of 0.86°(1SD) can be expected, and the maximum error that can be seen to be ±2°, which agrees with the first approach using cancellation as shown in Figure 61.

	Random phase Error excluding drift							
	Sd		Max		Min		p-p	
Freq (GHz)	Mag	Pha	mag	Pha	Mag	Pha	mag	pha
1	0.001045228	***0.410055***	0.996755	189.6884	0.989786	187.4165	0.00697	***2.271823***
2	0.001026687	***0.860117***	0.999284	189.0035	0.993272	184.912	0.006012	***4.09154***
3	0.002805192	***1.369231***	1.009444	188.6826	0.990582	181.5825	0.018862	***7.100088***
4	0.003525119	***1.096442***	0.992249	189.9963	0.974588	185.2498	0.01766	***4.746441***
5	0.004387204	***1.955524***	1.013911	189.8963	0.984898	180.2202	0.029013	***9.676099***
6	0.006425338	***2.47025***	1.004971	189.0582	0.969337	177.1944	0.035635	***11.86374***

Table 1 – statistical analysis of measurement results

From the results, it can be concluded that for the frequency range used for Doherty experiments (1.8 GHz), it will be very likely that the phase will be aligned to an accuracy within 1°, and will drift by no more than 2°/minute. So, as long as the measurement is conducted within a short time (10 seconds) of the phase alignment, the approach can be considered as valid.

4.2 Single-Tone Doherty Characterisation

Single-tone characterisation is a typical place to begin when investigating any PA and this is no different in the case of the Doherty. The following analysis utilises the single-tone measurement system introduced earlier in this chapter to firstly identify Doherty behaviour in early prototypes, and later to explore sensitivity and optimisation possibilities through perturbation of key parameters, specifically, relative input phase, relative input magnitude and relative bias profile.

Although the approach is common to all device technologies discussed in this thesis, this chapter aims to demonstrate the single-tone measurement system and characterisation approach through the measurement of the Doherty measurement prototype employing CF015-11 GaAs MESFET devices (see appendix-4). It is not the intention to present an exhaustive analysis of the different device technologies used within Doherty as this would be too lengthy an exercise, and is outside the intended scope of this thesis. Details of Doherty design using two different device technologies and their suitability to the Doherty application are presented in chapter 6.

4.2.1 Simple comparative measurements

The following set of measurements is important as it illustrates the presence of Doherty behaviour in early adaptive-bias and input-attenuation Doherty realisations and how these compare with two reference cases: a single-device mounted in a 50Ω evaluation board and a single device mounted in the *main* device position of the 25Ω Doherty measurement prototype.

4.2.1.1 CELERITEK MESFET test-board benchmark

The first experiment involved mounting a single CF015-11 GaAs MESFET device into a well-behaved and purpose built 50Ω test board in order to obtain base-line or reference data against which future Doherty structure data could be compared. The device was established in the same shallow class-B bias condition that was planned for the devices within the prototype Doherty structure, specifically V_D = 5.5V and V_G = -1.25 resulting in an I_{DQ} of approximately 20 mA. For the power sweep measurement the input drive power was increased up to and past the point of compression, whilst fundamental power, harmonic power and DC current behaviour were observed and measured. The data collected provided a behavioural benchmark against which future measurements employing the same devices could be gauged. Importantly, this data shows the natural spectral behaviour before harmonic suppression is attempted, and is summarised in *Figure* 65 below.

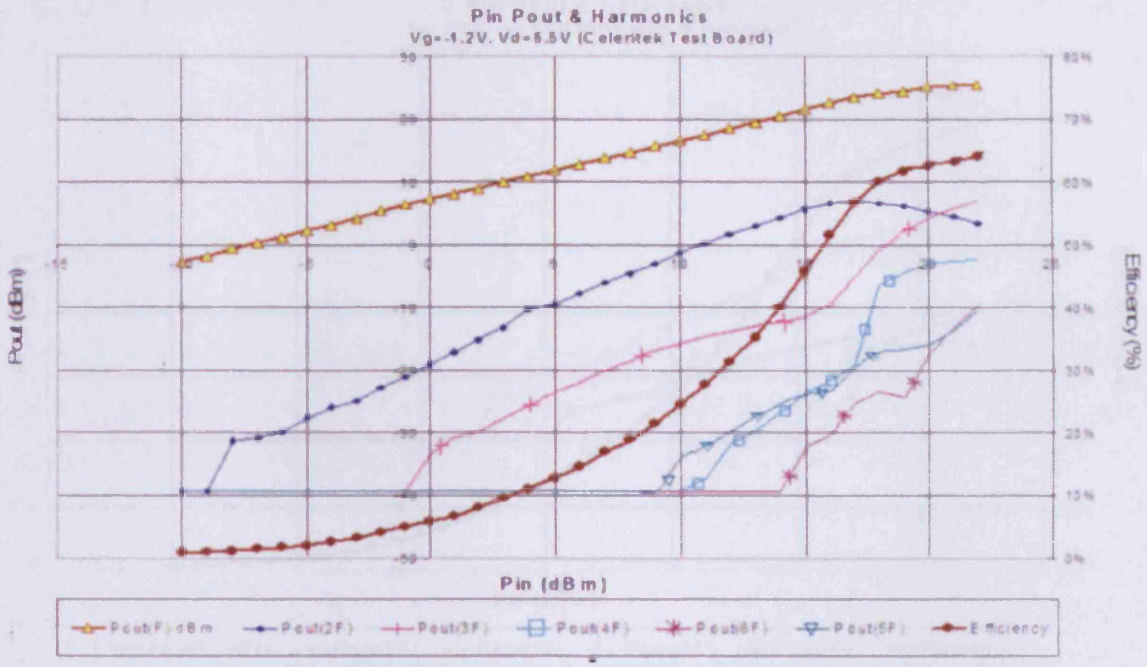


Figure 65 - CELERITEK HEMT in evaluation board

4.2.1.2 Single device in prototype structure

The next stage involved inserting a single, *main* device into the 25Ω prototype Doherty structure, the harmonic trap of which had been tuned as described in chapter 3. A comparative set of measurement results collected during a similar power sweep are presented in *Figure* 66 and clearly show the expected behaviour with significant suppression of even-order harmonic component. Specifically, second harmonic power is reduced by over 20 dB in comparison to that of *Figure* 65. The magnitude of the fundamental component at compression can be seen to be slightly reduced due to some unintentional loading of the fundamental component, and the efficiency can be seen to be slightly increased. Although the loading of the fundamental could be minimised by positional adjustment of the capacitive harmonic short, it was found that tuning resulted in a trade-off between second order harmonic suppression and fundamental gain, thus suggesting non-ideal behaviour of the harmonic trap.

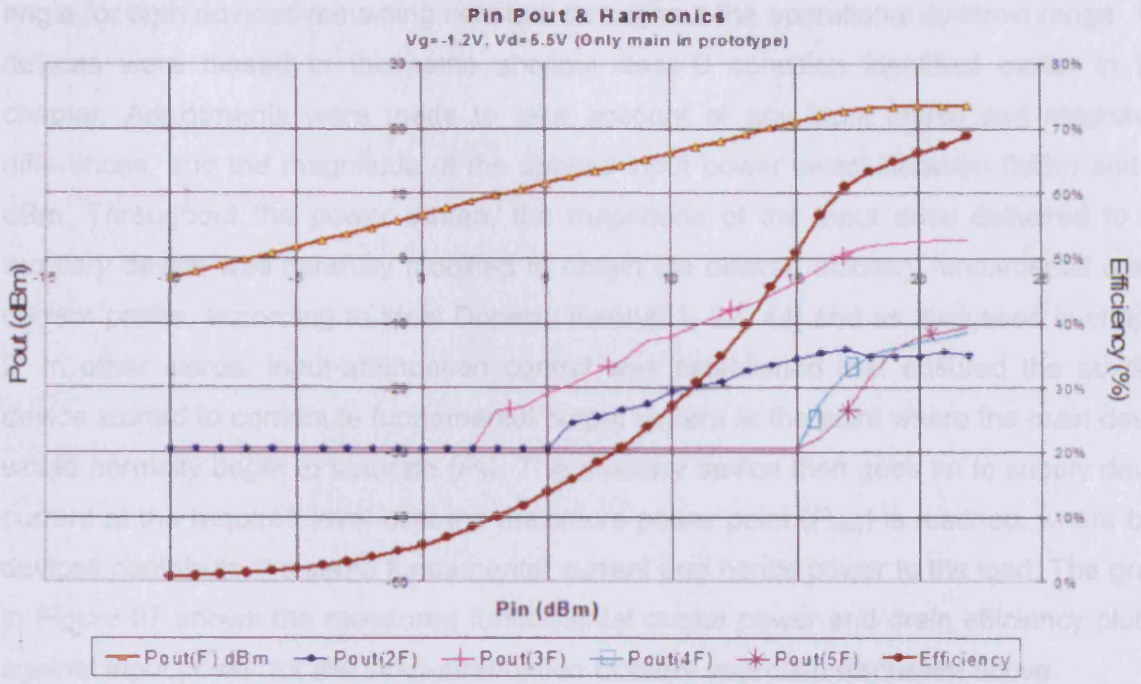


Figure 66 - main device alone in Doherty structure

4.2.1.3 Both devices in prototype structure with auxiliary device biased 'off'

The second, *auxiliary* device was then inserted into the prototype Doherty structure, and biased hard-off such that it was inactive throughout the power sweep. Further power sweep measurements were conducted that clearly showed that the presence of the *auxiliary* device presented no detrimental effect on previously established *main* device behaviour. This made sense as the off-state output parasitic capacitance of these devices was known to be relatively small[11]. It also indicated that the mounting of the *auxiliary* device and the physical presence of pads and bonding wires introduced no problematical reflective effects, at least at the fundamental frequency.

During the power sweep, the input power at the onset of saturation was noted, and this important value of P_{in} would be used to identify the transition power (P_T) that would be used in later Doherty measurements. At this stage, it was concluded that with both devices inserted and biased appropriately, the measurement structure behaved as expected and according to simulation in the low power region of operation.

4.2.2 Looking for Doherty behaviour – input-attenuation approach

The input-attenuation Doherty approach was chosen for initial investigations as it was considered to be the least complex in terms of harmonic generation with the conduction

[11] This is not always the case. LDMOS for example has an associated large, lossy output capacitance which can mean that the output will present a finite impedance which is frequency dependent.

angle for both devices remaining constant throughout the operational dynamic range. The devices were biased in the same shallow class-B condition identified earlier in this chapter. Adjustments were made to take account of any input phase and magnitude differences, and the magnitude of the applied input power swept between 0dBm and 20 dBm. Throughout the power sweep, the magnitude of the input drive delivered to the *auxiliary* device was carefully modified to obtain the desired *auxiliary* fundamental output current profile, according to ideal Doherty theory[21, 22, 44] and as discussed in chapter 2. In other words, input-attenuation control was established that ensured the *auxiliary* device started to contribute fundamental output current at the point where the *main* device would normally begin to saturate (P_T). The *auxiliary* device then goes on to supply device current at the required level until the maximum power point (P_{max}) is reached, where both devices contribute the same fundamental current and hence power to the load. The graph in *Figure* 67 shows the measured fundamental output power and drain efficiency plotted against input power for the input-attenuation Doherty approach discussed above.

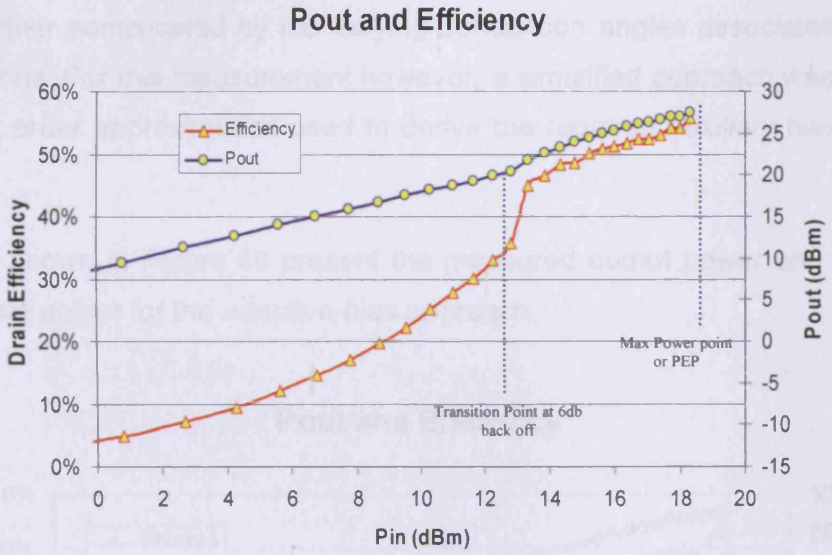


Figure 67 - measured P_{in}/P_{out} and efficiency for input-attenuation approach

Although far from optimal, Doherty behaviour is considered to be present. This conclusion was based on a number of observations: firstly, the combined fundamental power goes on to increase, although somewhat expansively from the transition point (P_T) for a further 6 dB of dynamic range, with no obvious sign of compression. Secondly, the average efficiency in the upper 6dB or high-power region ($P_T < P_{in} < P_{max}$) is 50% compared to 22% in the lower 6dB power region ($P_T\text{-}6 < P_{in} < P_T$) below the transition point. This compares to efficiencies of 39% compared to 16% respectively for the test-board reference amplifier

over a comparative dynamic range, as presented in *Figure* 65, and demonstrates an approximate 10% efficiency enhancement over 6dB of dynamic range.

4.2.3 Looking for Doherty behaviour – adaptive-bias approach

The notable disadvantage of the input-attenuation approach is the reduced efficiency in the low power region of input drive, which is a consequence of the small but ever-present *auxiliary* device quiescent current. In an attempt to improve the efficiency at the transition point, and for the entire region of input drive where only the *main* device is active, it is possible to bias the *auxiliary* device 'hard-off', such that it only becomes active when the transition point is reached. Using this approach, identical power can be delivered to both *main* and *auxiliary* devices through a simple symmetrical power splitter, and all the necessary conduction control implemented through appropriate adjustments of the *auxiliary* bias voltage.

The optimal relationship that relates *auxiliary* device bias voltage to *main* device input power is non-trivial however due to the non-linear growth of fundamental device current, which is further complicated by the varying conduction angles associated with changing bias conditions. For this measurement however, a simplified approach was adopted and a simple, first order approximation used to derive the required *auxiliary* bias voltages (See chapter 2).

The results shown in *Figure* 68 present the measured output power and drain efficiency vs. input drive power for the adaptive-bias approach.

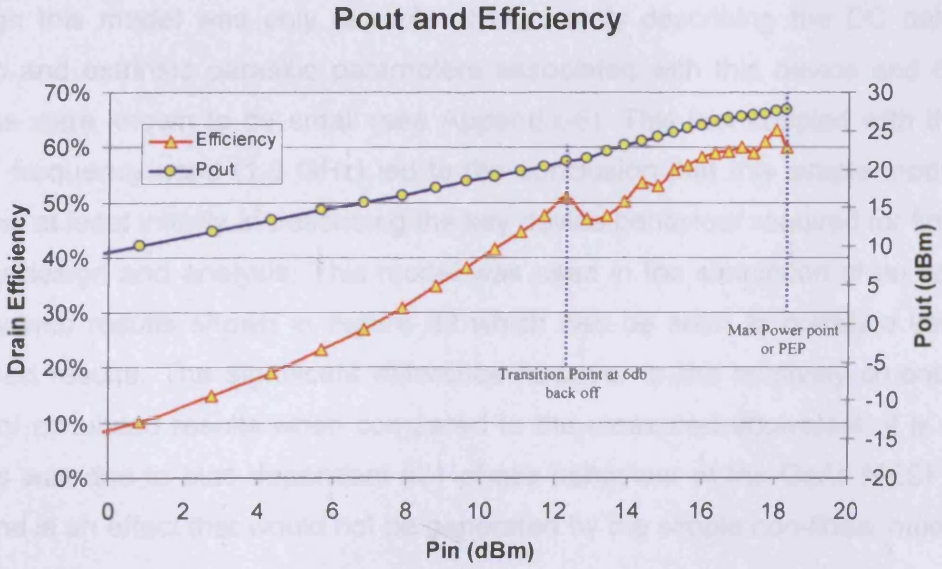


Figure 68 - measured P_{in}/P_{out} and efficiency for the adaptive-bias approach

As with the previous approach, Doherty behaviour is clearly present with a further improved average drain efficiency in the upper 6dB region ($P_T < P_{in} < P_T+6$) of 56% compared to a now much improved 36% in the lower power region below the transition point ($P_T-6 < P_{in} < P_T$), thus demonstrating a 16% efficiency enhancement over 6dB of dynamic range in comparison to the test-board reference amplifier.

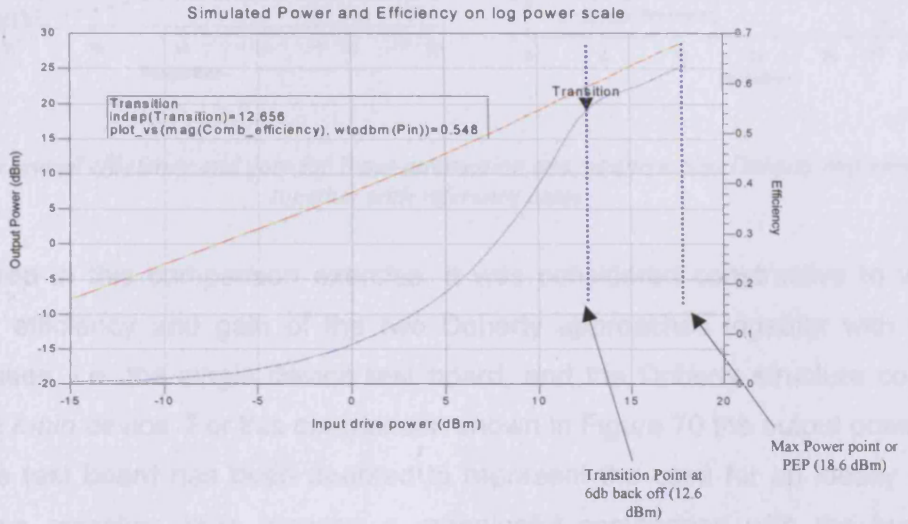


Figure 69 – ADS Simulated P_{in}/P_{out} and efficiency for the adaptive-bias approach

Using measured DC data, a polynomial representation of the device trans-conductance curve was extracted and used to generate a simple non-linear model in the form of a Symbolically Defined Device (SDD) component within the ADS simulation environment. Although this model was only capable of accurately describing the DC behaviour, the intrinsic and extrinsic parasitic parameters associated with this device and the leadless package were known to be small (see Appendix-6). This fact coupled with the relatively low RF frequency used (1.8 GHz) led to the conclusion that this simple model would be effective, at least initially in describing the key device behaviour required for first phases of Doherty design and analysis. This model was used in the simulation of an adaptive-bias Doherty with results shown in *Figure* 69 which can be seen to correlate very well with measured results. The significant difference however is the relatively smooth efficiency profile of simulated results when compared to the measured equivalent. It is now known that this was due to bias dependent s21 phase behaviour of the GaAs MESFET devices used and is an effect that would not be generated by the simple non-linear model used.

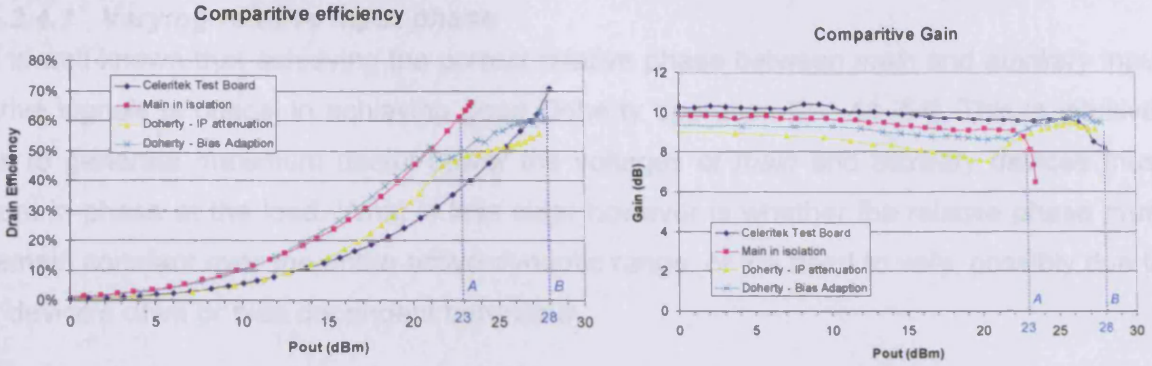


Figure 70 – measured efficiency and gain for Input-attenuation and adaptive-bias Doherty implementations, together with reference cases

As a final step in this comparison exercise, it was considered constructive to view the comparative efficiency and gain of the two Doherty approaches together with the two reference cases, i.e. the single device test board, and the Doherty structure containing only a single *main* device. For this comparison shown in Figure 70 the output power of the single device test board has been doubled to represent the case for an ideally coupled double device amplifier, thus allowing a meaningful comparison with the two-device Doherty realisations considered here.

The first observation is the low power region similarity between the efficiency profiles of *adaptive-bias* and *main-in-isolation* cases. This is of course expected as these structures are essentially identical in this region with the only difference being the presence of an inactive *auxiliary* device.

If the high power region is considered however, it is clear that the gain of the *main-in-isolation* case compresses at an input power of 23 dBm (point *A*), whilst the gain of the adaptive-bias does not start to compress until at least point *B*, some 5 to 6 dB further in the power sweep. The *main-in-isolation* case exhibits high efficiency in the high power region, but this is due to deep compression and saturation of the device, which is evident from the gain characteristic. The *adaptive-bias* case on the other hand exhibits a clear plateau of efficiency in the presence of non-compressive gain, and provides the most convincing Doherty behaviour.

The efficiency advantage of the Doherty over a conventional, similar periphery amplifier is clear from comparing the Celeritek test board case with both Doherty cases, although this is more pronounced for the adaptive-bias approach.

4.2.4 Optimisation through Parameter Perturbation

4.2.4.1 Varying relative input phase

It is well known that achieving the correct relative phase between *main* and *auxiliary* input drive signals is critical in achieving good Doherty operation [21, 44, 54]. This is intuitive, as to generate maximum useful power the voltages of *main* and *auxiliary* devices must sum in-phase at the load. What is less clear however is whether the relative phase must remain constant over the entire active dynamic range, or will need to vary, possibly due to a device's drive or bias dependent behaviour.

The initial approach in investigating this issue involved using algorithms within the measurement software to identify and track the optimum phase that existed during the power sweep measurement. This approach was limited however as it was difficult to detect maximum combined power at low *auxiliary* drive levels, and although it was possible to identify the presence of an optimum phase relationship, the technique did not provide an intuitive feel for the structure's behaviour.

An alternative approach was adopted where instead of attempting to locate the optimum relative phase at measurement time, a large number of power sweep measurements were made for a wide range of relative phases. The resulting three-dimensional dataset could then be analysed and post-processed in order to extract optimum phase relationships, and to construct descriptive surface plots that provided both the required analytical data, as well as the desired intuitive interpretation.

The following collection of figures shows output power, drain efficiency, gain and gain-phase of the GaAs MESFET Doherty structure using adaptive-bias control, plotted as functions of *main*-device input power between 5 dBm, and 20 dBm and relative input phase over ±120°.

By exploring the data and searching for maximum values, it is possible to identify the relative input phase that results in the maximum output power or efficiency for a given value of input power. This optimum phase is represented as a single contour superimposed on the surface plot.

Whereas Figure 71 suggests the optimum phase for maximum power is constant and unchanging with increasing drive, the optimum phase for maximum efficiency tells us a different story, and changes by approximately 30 degrees in the high-power region between 14 dBm and 20 dBm of input drive. This dependency of efficiency on relative input phase is a significant observation and is most noticeable in Figure 73, which when

rotated to reveal the side-view plot shown in Figure 72 illustrates the presence of a Doherty efficiency plateau whose profile compares very well with the earlier simulation results shown in Figure 69.

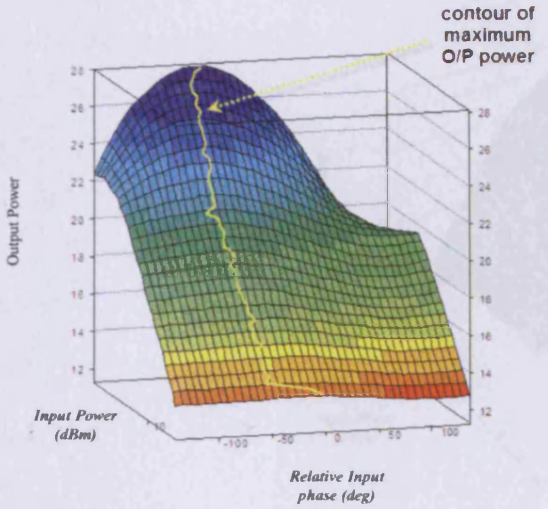


Figure 71 – swept input phase and output power

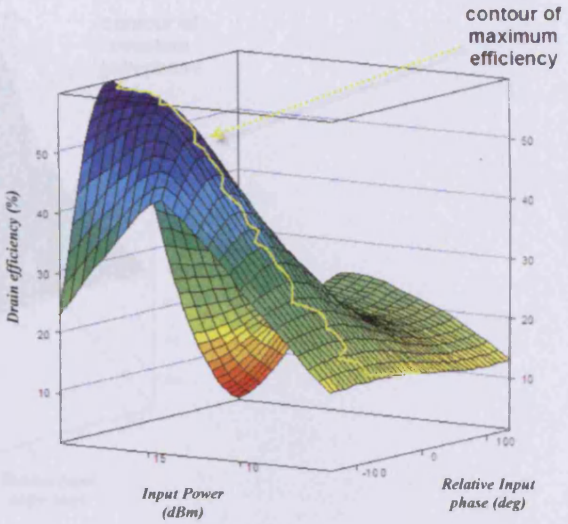


Figure 72 – swept input phase and drain efficiency

The plots of Figure 74 and Figure 75 show gain and gain-phase respectively as functions of both relative input phase and input power.

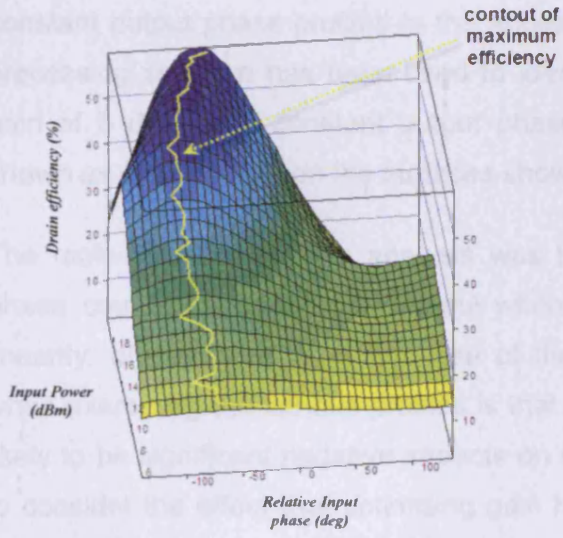


Figure 73 – rotated view of drain efficiency

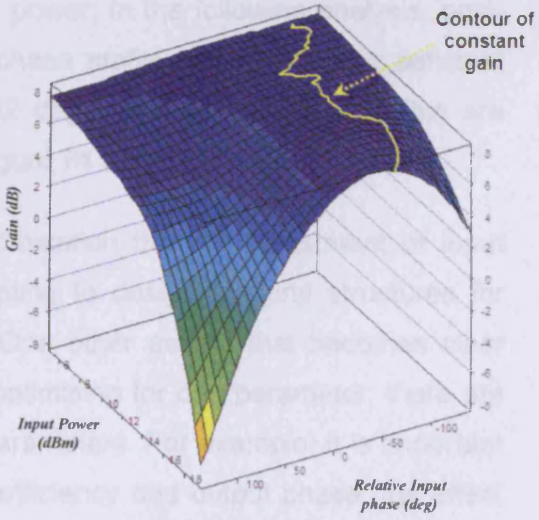


Figure 74 – swept input phase and gain

By studying these surface profiles, it is immediately apparent that the results reveal some quite complex non-ideal behaviour due to device interaction. On the other hand, the observation raises the interesting possibility that the Doherty structure can be optimised

and possibly linearised through the identification of constant gain and output phase contours, and the dynamic application of these contours to the relative input phase of the applied stimuli.

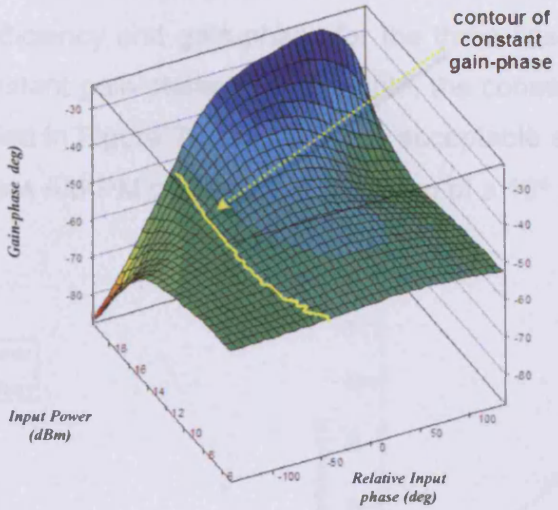


Figure 75 – swept input phase and output phase

Following the collection of data, post-processing software was written to identify the value of relative input phase that results in a specified, constant gain or gain-phase. In other words, relative input phase profiles were defined that related specific constant gain or constant output phase profiles to the applied input power. In the following analysis, post-processing software has been used to identify a phase profile that results in a constant gain of 8 dB and a constant output phase of –52 degrees. The identified profiles are shown as distinct lines on the surfaces shown in Figure 74 and Figure 75.

The motivation behind this analysis was that optimisation through adjustment of input phase could prove extremely useful when attempting to design Doherty structures for linearity, efficiency or a compromise of the two. One other aspect that becomes clear when examining the various profiles is that when optimising for one parameter, there are likely to be significant negative impacts on other parameters. For example, it is important to consider the effect that optimising gain has on efficiency and output phase, the effect that optimising efficiency has on gain and output phase and finally the effect that optimising output phase has on gain and efficiency.

Only specific cases are considered in this analysis, for instance optimising efficiency by seeking the phase that results in absolute maximum efficiency for all values of P_{in}. This approach is only so useful however as realising such a specific goal may result in poor

overall performance when in fact an acceptable compromise may exist. The analysis does serve however to highlight the *'trade-offs'* that exist if such an optimisation scheme were pursued.

The following figures show a set of graphs that allow the direct comparison of the key parameters of gain, efficiency and gain-phase for the three cases of optimum efficiency, constant gain and constant gain-phase. For example, the consequences of achieving the flat gain profile identified in Figure 76 results in the acceptable efficiency profile shown in Figure 77, but significant AM-PM behaviour, in the form of a 10° phase variation, shown in Figure 78.

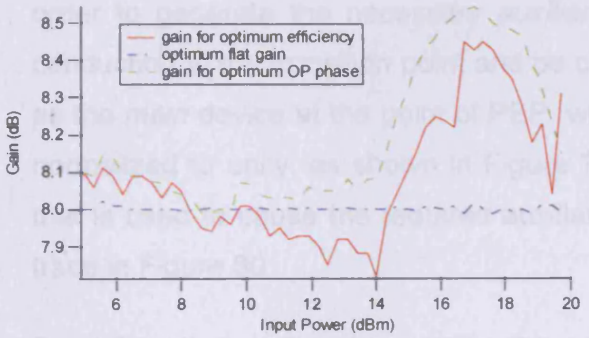


Figure 76 – AM-AM for different optimisations using relative input phase

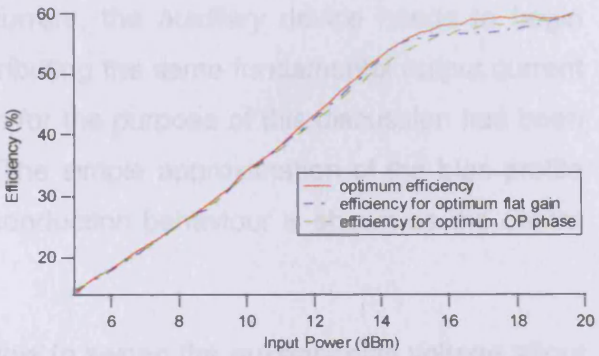


Figure 77 – efficiency variation for different optimisations using relative input phase

Similarly, the consequences of optimising for constant output phase are a flat phase profile in Figure 78 with again an acceptable efficiency profile shown in Figure 77, but significant AM-AM behaviour in the form of a 0.5 dB gain expansion, shown in Figure 76.

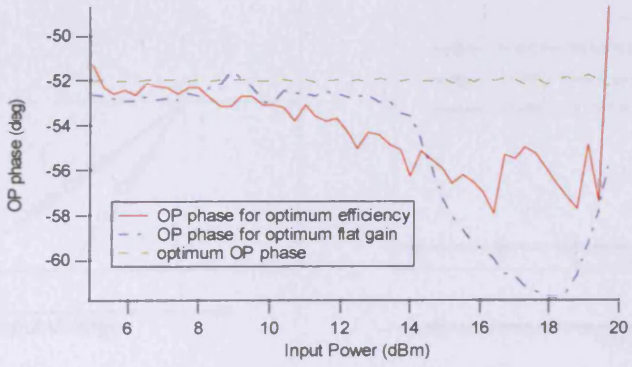


Figure 78 – AM-PM for different optimisations using relative input phase

When searching for constant gain or constant gain-phase solutions, care needs to be exercised when multiple solutions exist. As an example, consider the gain profile shown in

Figure 74 where there are clearly two different routes a contour of constant gain could follow around the raised area of gain expansion. When the surfaces are considered together, it is clear that one path will lead to the high efficiency shown in Figure 77, and the other to a very different and degraded efficiency profile.

4.2.4.2 Varying the auxiliary bias point

In an adaptive-bias Doherty structure such as the one used for the measurements detailed in this section, conduction control of the *auxiliary* device is achieved by synthesising an *auxiliary* bias voltage as a function of input drive power. *Main* device bias is held at a pre-defined value and relative input drive magnitude and phase are also held constant throughout the power sweep. As has been stated elsewhere in this thesis, in order to generate the necessary *auxiliary* current, the *auxiliary* device needs to begin conducting at the transition point and be contributing the same fundamental output current as the *main* device at the point of PEP, which for the purpose of this discussion has been normalized to unity, as shown in Figure 79. The simple approximation of the bias profile that is used to cause the required auxiliary conduction behaviour is shown as the centre trace in Figure 80.

By shifting the *auxiliary* bias profile, it is possible to sweep the *auxiliary* bias voltage about its normal profile, and in the same way as was used in the previous section, power sweeps were conducted for a set of *auxiliary* bias profiles as shown in Figure 80, allowing three dimensional surface plots to be generated.

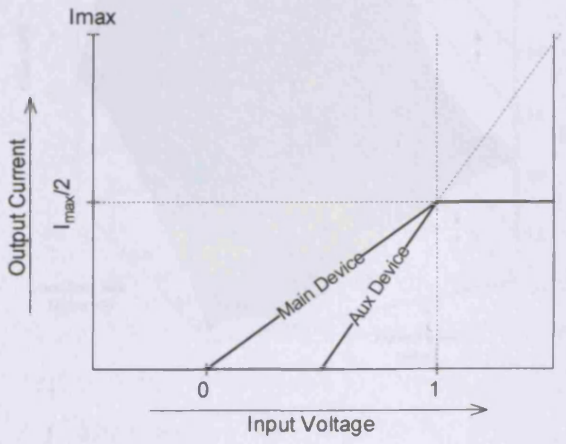


Figure 79 – ideal fundamental current for classical Doherty structure

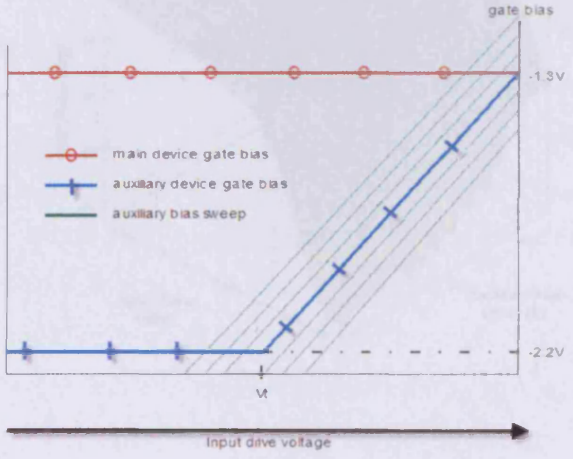


Figure 80 – ideal and swept gate bias profiles

The following set of graphs describe the structure behaviour for an *auxiliary* bias offset sweep over ±0.6V of the nominal *auxiliary* bias voltage profile, and for values of P_{in} swept between 5 dBm and 20 dBm.

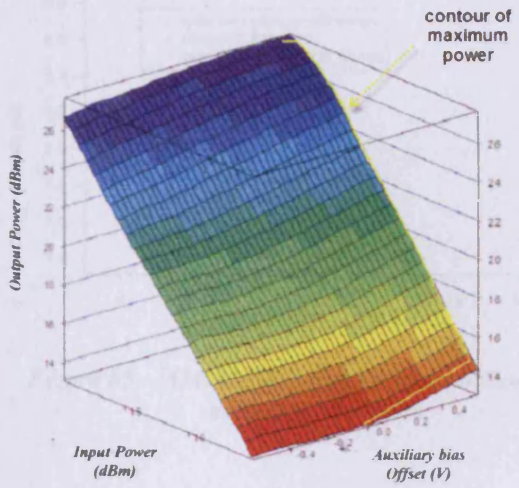


Figure 81 – swept auxiliary bias offset and output power

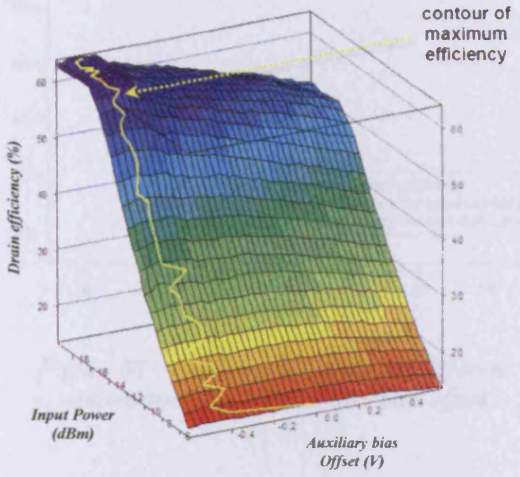


Figure 82 – swept auxiliary bias offset and drain efficiency

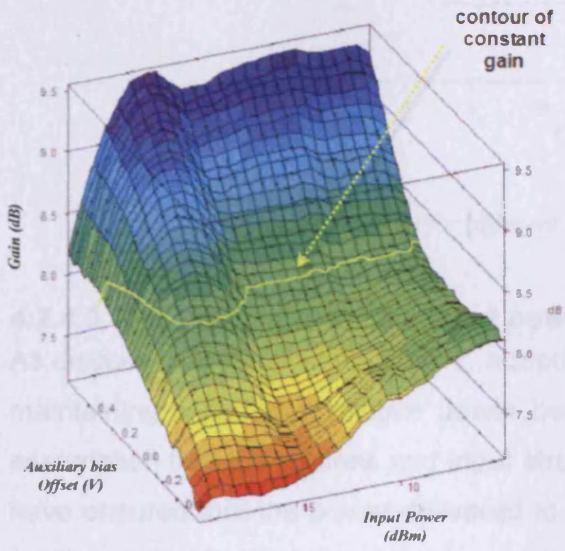


Figure 83 – swept auxiliary bias offset and gain

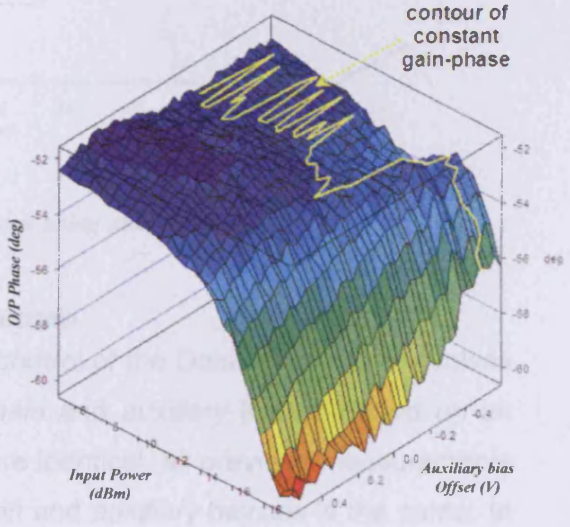


Figure 84 – swept auxiliary bias offset and output phase

As was the case for relative input phase, the gain and phase profiles indicate that similar optimisation is possible through the dynamic adjustment of the usual *auxiliary* bias voltage profile. The surfaces shown in Figure 83 and Figure 84 present the identified optimum

bias offset as a single contour, for a constant gain of 8.0 dB and constant output phase of –52 degrees respectively. As in the previous section, the consequences of using such optimum *auxiliary* bias profiles are shown in the following set of comparison graphs.

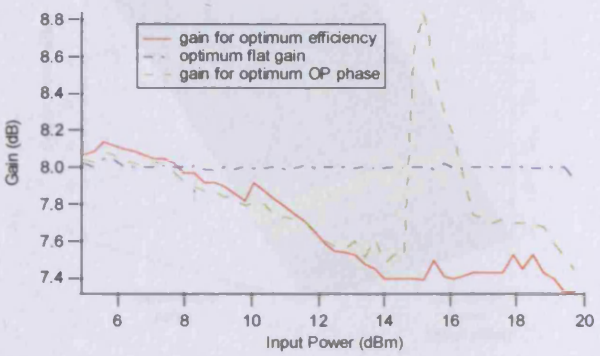


Figure 85 – AM-AM for different optimisations using auxiliary bias offset

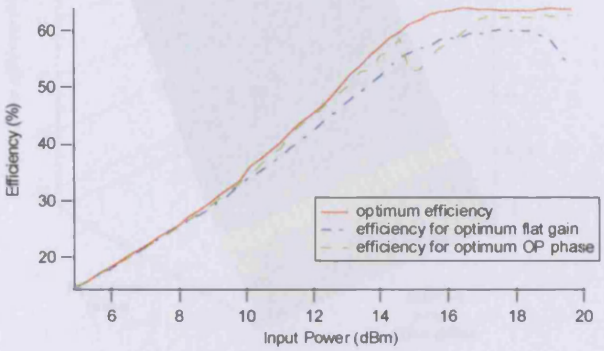


Figure 86 – efficiency variation for different optimisations using auxiliary bias offset

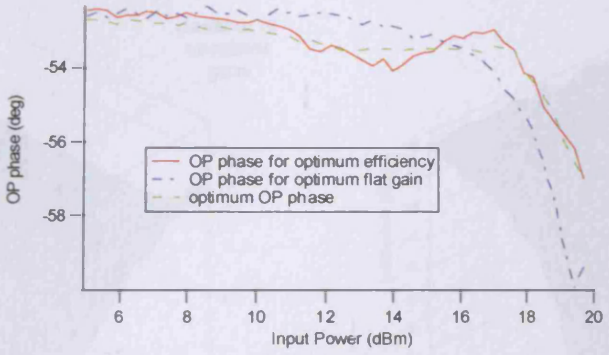


Figure 87– AM-PM for different optimisations using auxiliary bias offset

4.2.4.3 Varying the auxiliary input power magnitude

As discussed in detail in Chapter 2, adaptive-bias control of the Doherty structure involves maintaining a constant relative power between *main* and *auxiliary* inputs. Based on an assumption that the devices and input structures are identical, all previous measurements have ensured that the power delivered to both *main* and *auxiliary* devices is the same. In reality small differences in device gain and changes in input reflection coefficient lead to non-ideal behaviour. In order to explore these possibilities further and identify optimum behaviour, the usually symmetric power ratio between *main* and *auxiliary* input power was varied by ±1 dB during power sweeps.

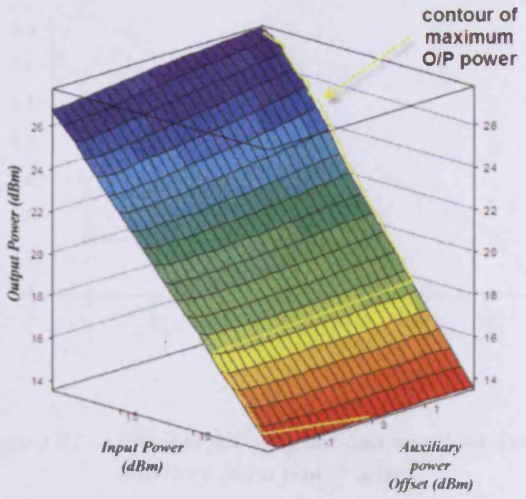


Figure 88 – swept auxiliary bias offset and output power

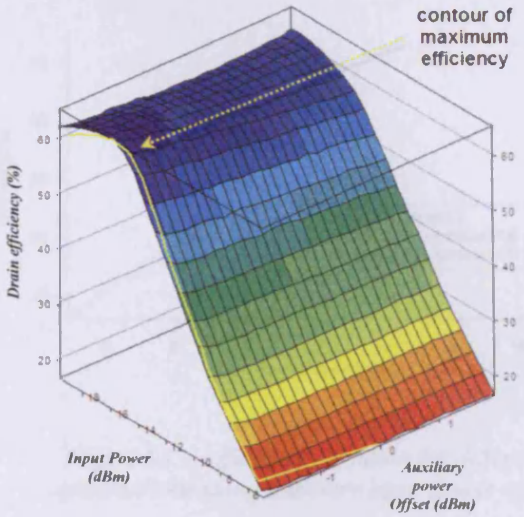


Figure 89 – swept auxiliary bias offset and drain efficiency

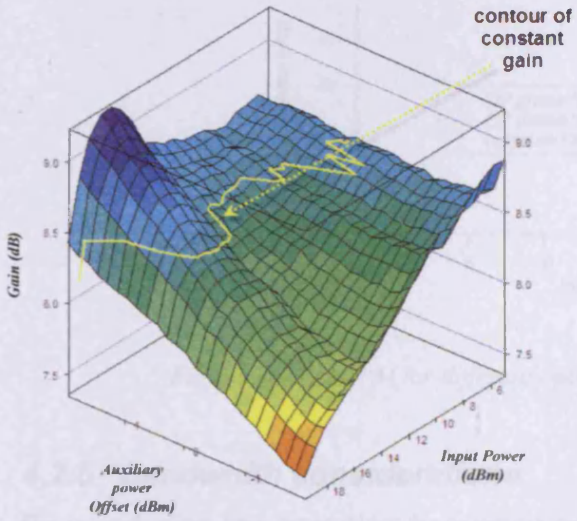


Figure 90 – swept auxiliary bias offset and gain

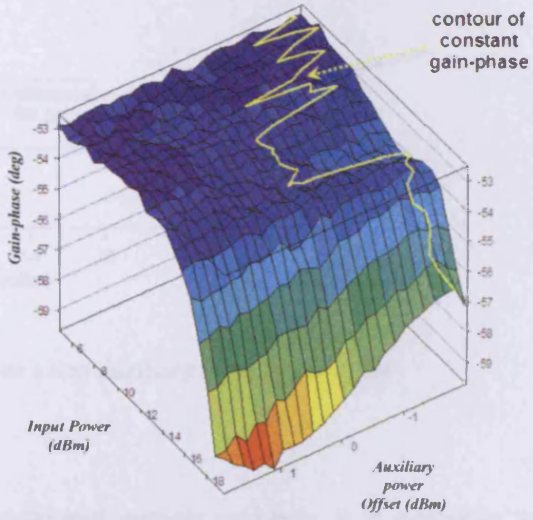


Figure 91 – swept auxiliary bias offset and output phase

The graphs in Figure 88 to Figure 91 show the structure behaviour when the *auxiliary* input power is varied by 2 dBm either side of its normal value during power sweeps between 0 dBm and 20 dBm. As in the previous sections, the gain profile and to a lesser degree, the gain-phase profile indicates that optimisation is possible. Figure 90 and Figure 91 show the identified optimum *auxiliary* input power magnitude offset as a distinct trace, for a constant gain of 8.5 dB and constant output phase of –52 degrees respectively.

The consequences to other parameters when employing this optimum *auxiliary* input drive profile are illustrated in the following graphs.

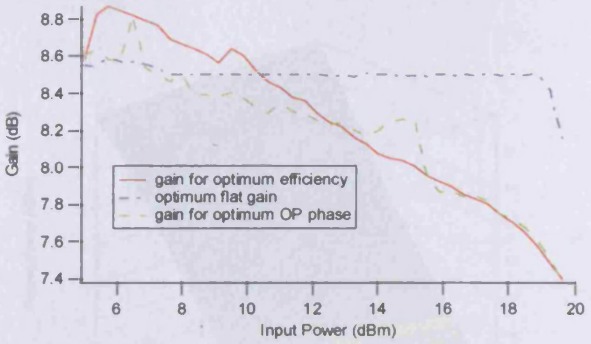


Figure 92 – AM-AM for different optimisations using auxiliary input power offset

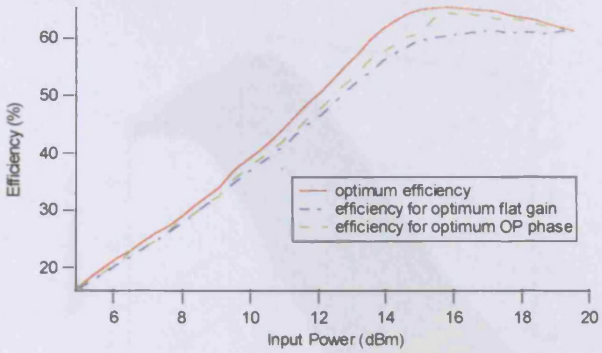


Figure 93 – efficiency variation for different optimisations using auxiliary input power offset

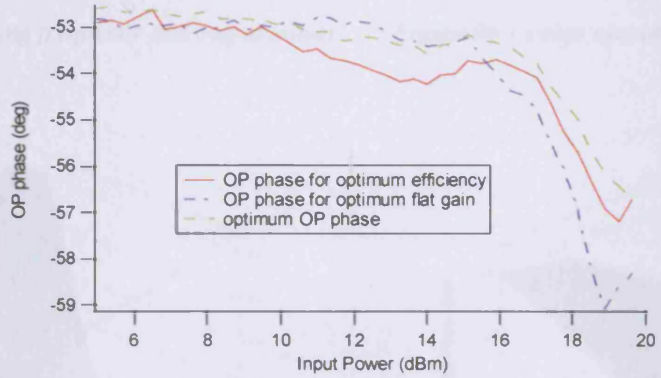


Figure 94 – AM-PM for different optimisations using auxiliary input power offset

4.2.5 Bandwidth considerations

By introducing the operating frequency as an additional sweep variable, it is possible to explore the behaviour of the Doherty structure over a given bandwidth.

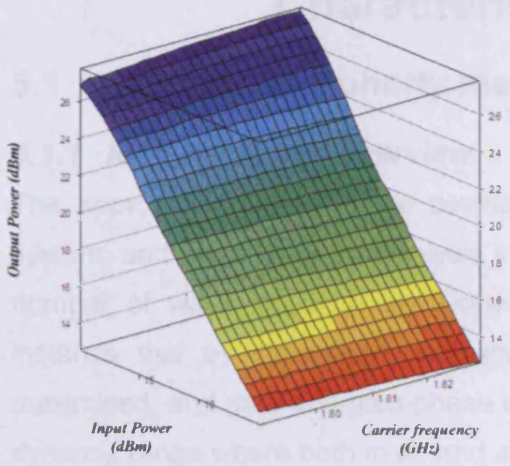


Figure 95 – swept operating frequency and output power

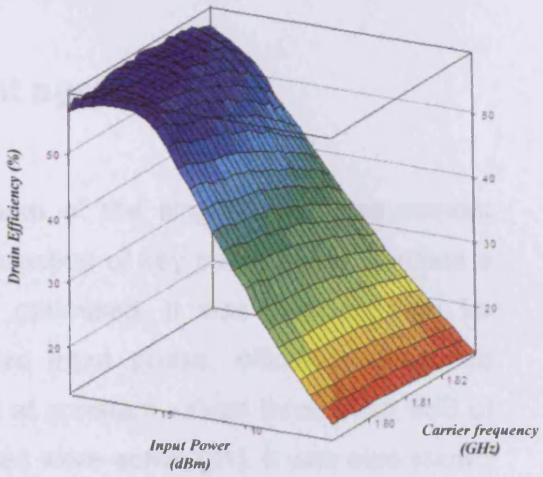


Figure 96 – swept operating frequency and drain efficiency

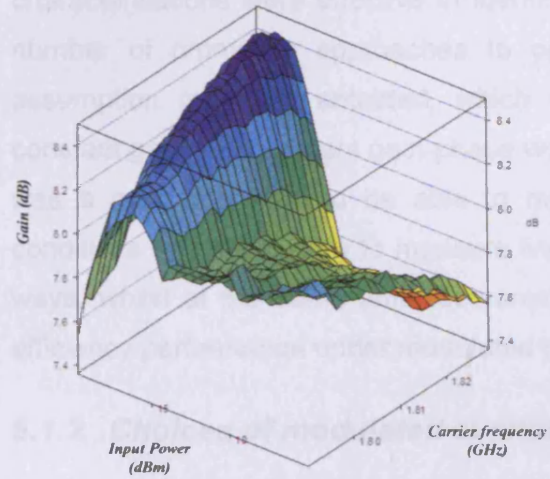


Figure 97 – swept operating frequency and gain

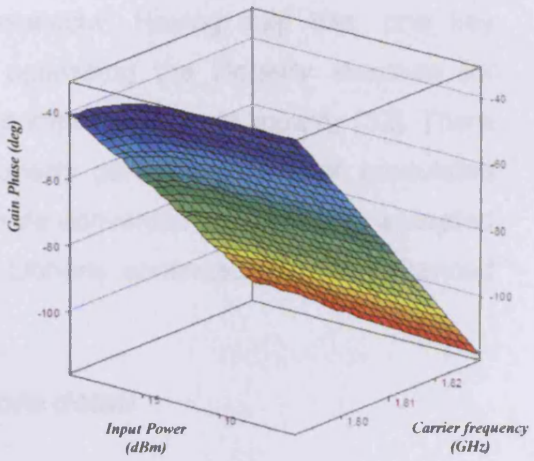


Figure 98 – swept operating frequency and output phase

The above graphs show the behaviour of the structure when the fundamental operating frequency is varied by 40 MHz between 1.79 and 1.83 GHz. Although reasonable performance is maintained over the given bandwidth, AM-AM and AM-PM behaviour changes significantly with frequency.

Chapter 5 Multi-tone Measurement and Characterisation

5.1 Multi-tone Doherty measurement systems

5.1.1 Motivation and overview

The approach adopted in the development and use of the single-tone measurement system, and specifically the analysis involving perturbation of key parameters identified a number of ways in which the Doherty could be optimised. It was demonstrated for instance that by dynamically adjusting the relative input phase, efficiency could be maximised, and gain and gain-phase could be held at constant values throughout 6dB of dynamic range where both *main* and *auxiliary* devices were active [31]. It was also shown that similar optimisation was possible through the dynamic adjustment of other parameters, specifically the relative input magnitude and relative bias profile.

It is clear that the single-tone measurement system and subsequent single-tone characterisations were effective in identifying some interesting Doherty behaviour and a number of promising approaches to optimise behaviour. Having said this, one key assumption remained untested, which was that optimising the Doherty structure for constant gain and constant gain-phase would lead to improvements in linearity [32]. There was a need therefore to be able to measure Doherty performance under modulated conditions and specifically to measure linearity in more conventional and widely accepted ways, whilst at the same time, demonstrating the Doherty continued to offer enhanced efficiency performance under modulated conditions.

5.1.2 Choices of modulated excitation in more detail

5.1.2.1 Modulation overview

In order to fully explore and characterise the Doherty PA, it is clearly necessary to measure the response not only to a single-tone stimulus but also a modulated excitation. The obvious choice would be to opt for real-life modulation schemes such as GSM-EDGE and W-CDMA with linearity being measured using established methods such as Error Vector Magnitude (EVM) and Adjacent Channel Power Ratio (ACPR). Although possible, this approach does not present a complete solution for Doherty characterisation for a number of reasons. Firstly, the complexity of the modulation envelopes associated with these continuous modulation schemes means that comparison between single-tone and modulated behaviour becomes difficult due to envelope averaging effects. Secondly, the base-band control signals that are necessary in implementing some Doherty approaches such as adaptive-bias and input-attenuation are functions of the instantaneous envelope

magnitude, and therefore themselves become complex, harmonically rich and difficult to synthesise. Because of the complexity and non-repetitive nature of continuous modulation, the synthesis of base-band signals that are phase coherent with the modulation envelope becomes highly problematical.

Although traditional two-tone excitation is easier to synthesise and control in comparison to continuous modulated excitation, it has one significant disadvantage when used for characterising Doherty amplifiers: measured key parameters will be averaged over the two-tone modulation envelope, and as a result do not compare well to single-tone equivalents. An alternative approach has been developed that allows the meaningful comparison of key performance data to single tone equivalents, as well as the measurement and characterisation of Doherty linearity.

An engineered form of three-tone excitation has been implemented that allows a characterisation approach where the depth of modulation can be varied whilst the Peak Envelope Power (PEP) remains at some static, pre-determined level. This property offers an advantage over the traditional two-tone approach in that specific areas of an amplifier's dynamic range and transfer characteristic can be excited. Although this feature may be advantageous in many PA applications, it is particularly useful in the case of the Doherty PA as there is a specific interest in characterising the 6dB area of dynamic range extending from the maximum power point (P_{max}) to the notional Doherty transition point (P_T), over which both devices are active and interacting with each other.

5.1.2.2 Single-tone excitation

Single-tone excitation is extremely important as a measurement tool and allows many aspects of Doherty behaviour to be explored and characterised. Whilst harmonic behaviour and key performance parameters such as gain, efficiency, and drain current are effective in describing the degree and quality of efficiency enhancing behaviour observed, linearity indicators are restricted to measures of gain and gain phase over dynamic range, both of which are ideally constant in a linear PA. This approach is only of limited use however as ultimately any optimisation approach based on single-tone measurements will need to be validated using some form of modulated excitation.

A single-tone excitation with peak voltage amplitude a, frequency f_1 and phase ϕ can be described by (17) and the resulting PA current described by the Taylor series in (18).

$$V_i(t) = a.\cos(2\pi f_1 t + \phi) \tag{17}$$

$$I_o(t) = A_1 V_i(t) + A_2 V_i^2(t) + A_3 V_i^3(t) + \cdots A_n V_i^n(t) \quad (18)$$

The general non-linear process of amplification will generate spectral components, here limited to the third order, described the by the equations, in Table 2.

$\frac{A_2 a^2}{2}$	*DC term*
$A_1\left[1+\left(\frac{3A_3 a^2}{4A_1}\right)\right]a\cos\theta$	*Fundamental term*
$\left(\frac{A_2 a^2}{2}\right)\cos 2\theta$	*Second order term*
$\left(\frac{A_3 a^3}{4}\right)\cos 3\theta$	*Third order term*

Table 2 – spectral generation due to single-tone excitation, limited to third order

5.1.2.3 Two-tone excitation

For many years, two-tone modulation was the excitation of choice in characterising PA linearity. Nowadays however, the use of two-tone modulation as a stimulus is generally being replaced by more relevant and application focused measurement techniques such as EVM and ACPR. Whereas EVM is a direct measure of the accuracy of the amplification process, ACPR is the direct measurement of the frequency components generated in close proximity to the *main* carriers, which results from spectral spreading. Two-tone excitation offers a way of quantifying PA linearity through the measurement of inter-modulation distortion products that occur due to the mixing processes described in [55], and that appear in proximity to the carrier frequencies. The advantage of two-tone over other, more complex modulation schemes is that mixing products are easily measured, limited in number and appear at very specific frequency locations, which can prove useful in both the measurement and analysis of modulated behaviour.

Consider for example the transfer function for a PA described by the Taylor series described in (18) which is excited by the two-tone modulation described in (19)

$$V_i(t) = a\cos(2\pi \cdot f_1 t) + a\cos(2\pi \cdot f_2 t) \quad (19)$$

In this case, the non-linear properties of the transfer function will generate an output spectrum of increased complexity, described to the third order by the equations in Table 3 where $\theta_n = 2\pi \cdot f_n t$.

$A_2 a^2$	*DC term*
$A_1 a\left[1+\left(\frac{9A_3a^2}{4A_1}\right)\right](\cos\theta_1+\cos\theta_2)$	*Fundamental term*
$\left[\left(\frac{A_2a^2}{2}\right)\cdot(\cos 2\theta_1+\cos 2\theta_2)\right]+A_2a^2\left(\cos(\theta_1+\theta_2)+\cos(\theta_1-\theta_2)\right)$	*Second order terms*
$\left(\frac{A_2a^3}{4}\right)\cos 3\theta_1+\cos 3\theta_2+\left(\frac{3A_2a^3}{4}\right)[\cos(2\theta_1+\theta_2)+\cos(2\theta_1-\theta_2)]\cdots$	*Third order terms*
$+\frac{3A_3a^3}{4}(\cos(2\theta_2+\theta_1)+\cos(2\theta_2-\theta_1))$	

Table 3 - spectral generation due to single-tone excitation, limited to third order

Observation of the magnitude and phase of specific inter-modulation products under different modulation rates can provide an insight into other important behaviour [56], and specifically the memory effects that are inherent in most PA structures. These effects are typically analysed by considering specific behaviour such as the asymmetry that may exist between pairs of inter-modulation terms, usually the 3rd order products either side of the carrier components [57].

The graph in Figure 99 shows a simulated two-tone modulation envelope, where a high modulation frequency of approximately 1/7th of the carrier frequency has been used to allow visibility of both RF and modulation envelope. The I and Q component base-band signals that describe this modulation are shown in Figure 100.

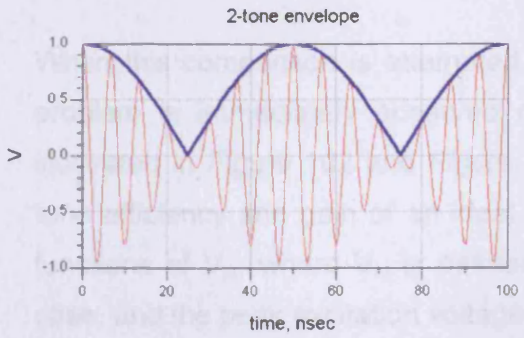


Figure 99 – two-tone envelope showing the instantaneous magnitude of the base-band component

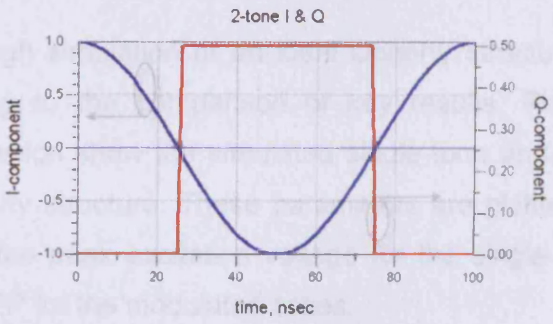


Figure 100 – I and Q base-band waveforms describing the two-tone envelope

From these plots, it is clear that for the two-tone modulation scheme, the instantaneous RF magnitude will be zero each time the I-component crosses the zero axis, at which point a phase inversion occurs. In order to obtain a modulation envelope possessing a desired PEP, two tones ω_1 and ω_2 of magnitude PEP - 6dB will be required and the modulation rate will be $\omega 1$-$\omega 2$ where there are two 'pulses' of RF per cycle of modulation.

The Peak-to-Average Ratio (PAR) of this modulation is 3 dB, and its Probability Density Function (PDF) in relation to a classical Doherty efficiency characteristic is shown in Figure 101.

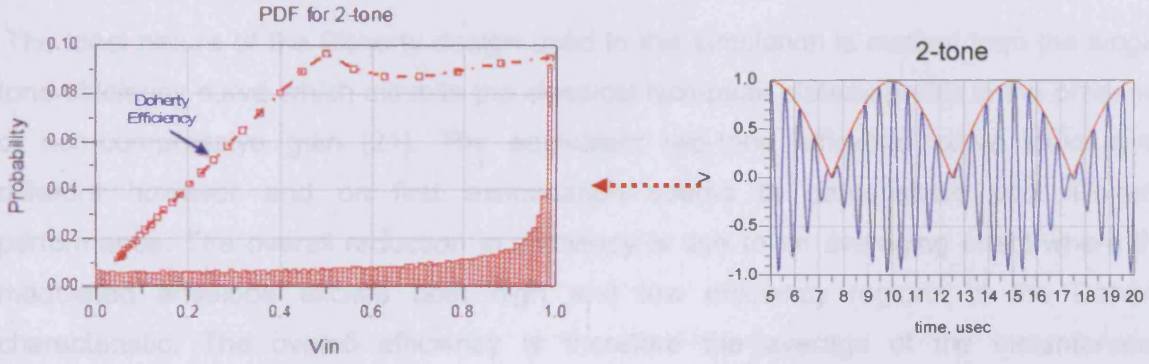


Figure 101 – PDF of two-tone modulation with ideal Doherty efficiency characteristic

During development of the measurement system and the introduction of different types of excitation, it was considered important to retain the ability to verify correct and explainable Doherty behaviour, regardless of the modulated excitation used, as well as to be able to show consistency when comparing results using these different excitations. For example, following the very first simulations and measurements using modulated signals, there was an obvious need to compare the single-tone and two-tone efficiency of the simulated and measured PA structures in order to gain confidence and show that the approach was effective in both cases.

When this comparison is attempted through simulation of an ideal Doherty structure, a problem is immediately observed relating to the comparison of key results. This is illustrated in *Figure* 102 and *Figure* 103 which show the simulated single-tone and two-tone efficiency and gain of an ideal Doherty structure. These parameters are plotted as functions of V_{in}, where V_{in} is defined as the peak excitation voltage for the single-tone case, and the peak excitation voltage at PEP for the modulated cases.

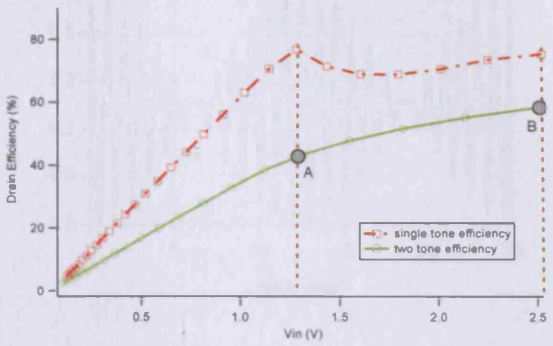


Figure 102 – ideal single-tone and two-tone Doherty efficiency

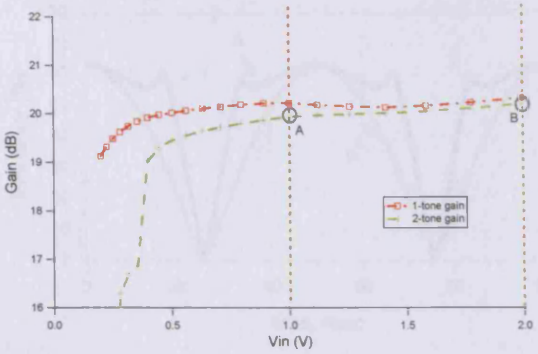


Figure 103 – ideal single-tone and two-tone Doherty gain

The ideal nature of the Doherty design used in this simulation is evident from the single-tone efficiency curve which exhibits the classical twin-peak plateau profile in the presence of non-compressive gain [21]. The equivalent two-tone efficiency curve looks quite different however and on first examination seems to demonstrate poor Doherty performance. The overall reduction in efficiency is due to an averaging effect where the modulated envelope excites both high and low efficiency regions of the Doherty characteristic. The overall efficiency is therefore the average of the instantaneous efficiencies over the entire modulation cycle, and will therefore always be lower and 'featureless' in comparison to the single-tone case.

If single-tone and two-tone gain are considered in the same way, as shown in Figure 103, a much more favourable comparison is observed, especially over the dynamic range of interest which exists between V_{in_max} and $V_{in\_max}/2$. This is due to the gain being a more constant function of input drive than efficiency over dynamic range, which is an observation that demonstrates the problem: whereas some single-tone and two-tone Doherty performance parameters compare favourable, the critical parameter of efficiency does not.

Figure 104 illustrates this problem in the time domain, and shows a classical two-tone envelope for the two cases of *PEP*: the first causes the ideal Doherty to develop a peak output power of $P_{max}/4$ corresponding to input voltage of $V_{in\_max}/2$, whilst the second causes a peak output power of P_{max} corresponding to an input voltage of V_{in_max}. Figure 105 shows an envelope domain representation of Doherty efficiency for the two cases of PEP.

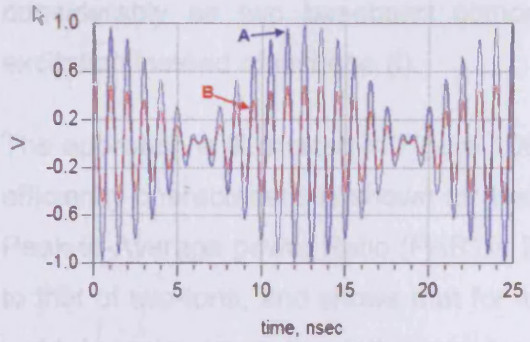


Figure 104 – two-tone envelope for two cases of PEP

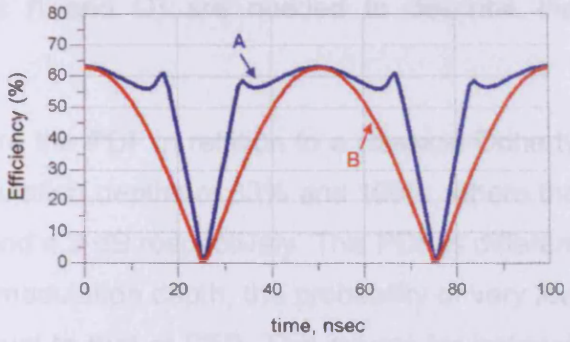


Figure 105 – two-tone instantaneous Doherty efficiency for two cases of PEP

Viewed in this way, it becomes clear how averaging can cause a problem when using efficiency as a performance indicator.

So, although both single-tone and two-tone results are completely valid and effective in accurately describing the Doherty's efficiency response to a two-tone power sweep, the results require some interpretation and an appreciation of the averaging problem. At first glance, they may convey poor performance due to the absence of the classical Doherty indicator of an efficiency plateau in the presence of non-compressive gain, which is in contrast clearly visible in the single-tone case.

From both data presentation and data validation perspectives, it would clearly be advantageous to use an excitation that allows both meaningful modulated analysis and yields performance results that are easily comparable with the single-tone case.

5.1.2.4 Three-tone

Other problems relating to two-tone excitation stem from the fact that the two signals comprising the modulation will have opposite phase, and will completely cancel twice every modulation cycle resulting in a modulation envelope with infinite dynamic range. This property can sometimes be problematical, for example when there is no interest in how a DUT responds to very low envelope power levels, as is the case with the Doherty

Another way to synthesise a suitable modulated excitation is to use a symmetrical three-tone approach and the addition of a carrier component to the classical two-tone modulation. By careful manipulation of the relative and absolute tone magnitudes, the PEP can be fixed whilst the modulation depth can be varied, thus providing complete flexibility of the excitation envelope. Although it is possible to achieve variable modulation depth using asymmetrical 2-tone, the resulting RF envelope will contain both phase and magnitude information, and from a measurement perspective, this complicates matters

considerably as two baseband components (I and Q) are needed to describe the excitation instead of just one (I).

The approach is illustrated in Figure 106 where the PDF in relation to a classical Doherty efficiency characteristic is shown for two modulation depths of 33% and 100%, where the Peak-to-Average power Ratio (PAR) is 2 dB and 4.2 dB respectively. This PDF is different to that of two-tone, and shows that for 100% modulation depth, the probability of very low instantaneous power is relatively high and equal to that of PEP. This means for instance that if 100% three-tone modulation is used in place of two-tone to excite an amplifier, the observed average efficiency will be slightly lower. The important difference between two and three-tone as an excitation however is that the PDF profile of three-tone can be moved and located anywhere in a PA's dynamic range, as shown in Figure 106.

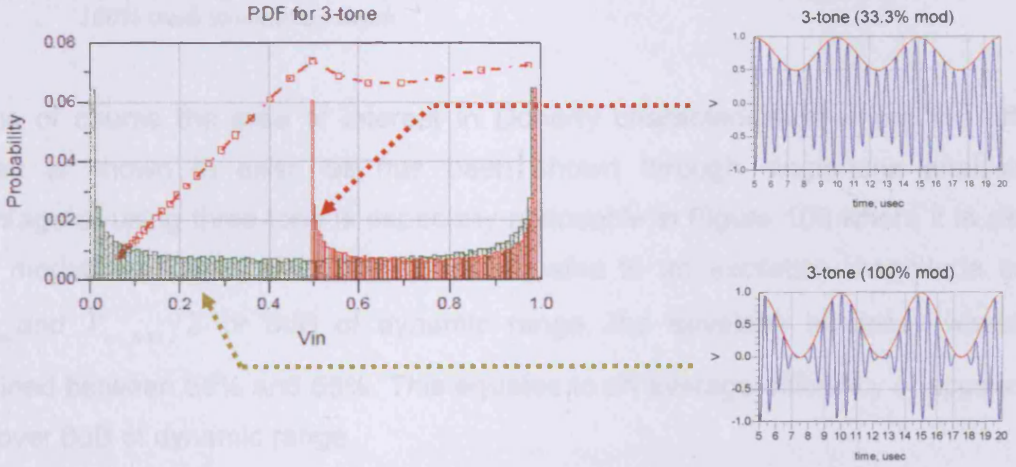


Figure 106 – PDF characteristics of three-tone modulation

This approach is very attractive from a Doherty perspective as it allows specific areas of the transfer characteristic to be excited. More specifically, this type of modulation has the ability to explore Doherty behaviour over the dynamic range of interest, which typically exists between the point of maximum power and the transition point. The advantage is further illustrated in Figure 107, where three modulation envelopes have been generated possessing modulation depths of 0%, 33.3% and 100%. If PEP, which is the same in all cases, is selected to correspond to the maximum input power to be delivered to the Doherty, then the 33.3% modulation would excite the area of dynamic range between PEP and the transition point (PEP-6dB); whereas 100% modulation would excite the complete Doherty characteristic.

When comparative efficiency and gain is considered for both single-tone and three-tone as shown in Figure 108 and Figure 110, it is clear that maintaining a constant PEP and

sweeping modulation depth will result in a much improved and meaningful comparison to the single-tone efficiency, in the high power region between V_{in_max} and the transition point (P_T).

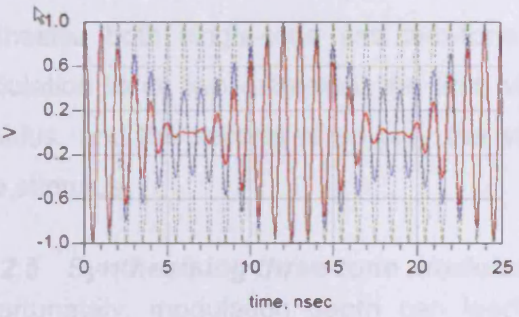


Figure 107 – three-tone envelope for three different cases of 0% (green), 33.3% (blue) and 100% (red) modulation depth

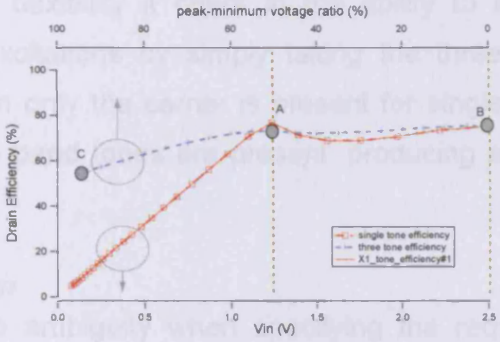


Figure 108 – ideal single-tone and three-tone Doherty efficiency

This is of course the area of interest in Doherty characterisation where the efficiency plateau is known to exist, as has been shown through single-tone analysis. The advantage of using three-tone is especially noticeable in Figure 109 where it is clear that for a modulation depth of 33.3%, which equates to an excitation magnitude between V_{in_max} and $V_{in\_max}/2$ or 6dB of dynamic range, the envelope efficiency waveform is contained between 55% and 65%. This equates to an average efficiency of approximately 60% over 6dB of dynamic range.

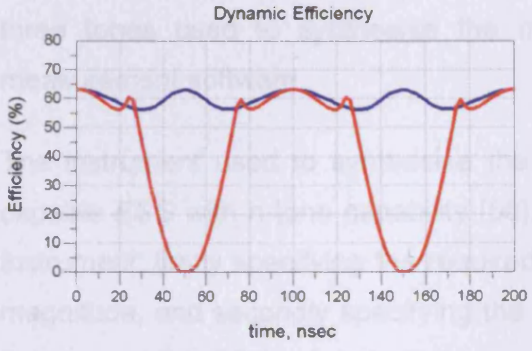


Figure 109 – efficiency waveforms for two cases of 33.3% and 100% modulation depth.

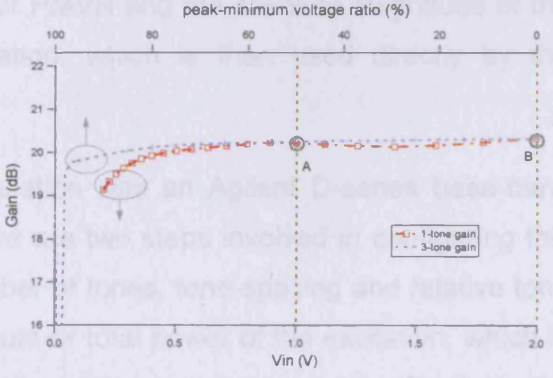


Figure 110 – ideal single-tone and three-tone Doherty gain

It is interesting to note that when the modulation depth approaches 100%, the resulting envelope physically resembles that of two-tone at maximum power. As the envelopes will

be very similar at this point, the measured Doherty performance can be expected to be similar. This is apparent when comparing point-B in Figure 102 with point-C in Figure 108, where the resulting efficiencies are 58.4% and 55% respectively.

Another advantage of this approach is the flexibility it offers in the ability to easily synthesise both single-tone and two-tone excitations by simply taking the three-tone modulation to its two extremes; the first when only the carrier is present for single-tone stimulus, and the second when only the side band tones are present, producing a two-tone stimulus

5.1.2.5 Synthesising three-tone modulation

Unfortunately, modulation depth can lead to ambiguity when specifying the required, specific Doherty modulation conditions. For example, a modulation envelope that will excite the characteristic between $V_{in\_\max}$ and $V_{in\_\max}/2$ will require a modulation depth of 33%, which is not completely obvious. For reasons of clarity an additional parameter is introduced which expresses the degree of modulation in terms of Peak-to-Minimum Voltage Ratio (*PMVR*). This is a more meaningful measure for use in specifying Doherty measurements as it is effectively the ratio of the maximum and minimum envelope voltage magnitudes. For example, the above modulation envelope that is designed to excite the PA's characteristic between $V_{in\_\max}$ and $V_{in\_\max}/2$ will be defined by a *PMVR* value of 50%, and not the usual 33.3% used when specifying modulation depth.

From a measurement system perspective, an important relationship is defined between the required value of PEP, modulation depth or PMVR and the absolute magnitude of the three tones used to synthesise the modulation, which is then used directly by the measurement software.

The instrument used to synthesise the modulation was an Agilent D-series base-band capable *ESG* with n-tone capability [58]. There are two steps involved in configuring this instrument; firstly specifying the required number of tones, tone-spacing and relative tone magnitude, and secondly specifying the absolute or total power of the excitation, which in the case of the *ESG* refers to the average power of the modulation and is effectively the sum of the individual tone powers. This process is summarised in Figure 111 and Figure 112.

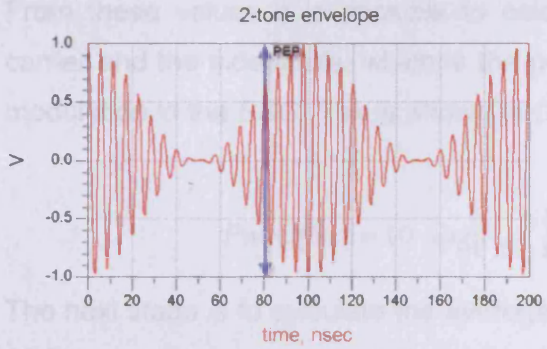


Figure 111 – simple three-tone envelope at 100% modulation with PEP

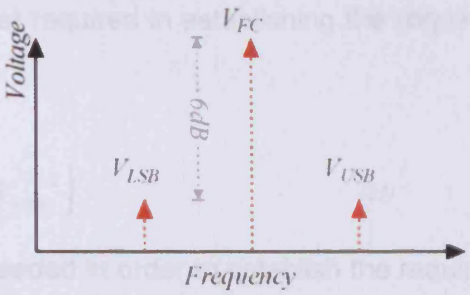


Figure 112 – spectral equivalent of modulation envelope

It is known that the Peak Envelope Power (PEP) occurs when all the tone vectors sum in-phase, so a notional variable VPEP can be defined in terms of spectral voltages, which represents the peak envelope voltage. This is further explained in Appendix 6.

$$V_{PEP} = V_{FC} + V_{USB} + V_{LSB} \tag{20}$$

V_{PEP} can also be defined in terms of *PEP* in a 50 Ω environment, as shown in (21).

$$V_{PEP} = \sqrt{PEP(Watts) * 100} \tag{21}$$

Classically, modulation depth as defined in (22).

$$Modulation\_Depth = \frac{V_{\mathrm{mod}}}{V_{carr}} \quad *100 \tag{22}$$

Given a required value of PEP, it is possible to calculate the voltage components for each tone. Firstly, the modulation index is defined in (23).

$$m\_index = \frac{Modulation\_Depth}{100} \tag{23}$$

It is then possible to derive the individual voltage components, as shown in (24)

$$V_{FC} = \frac{V_{PEP}}{[1 + m\_index]} \quad V_{USB} = \frac{m\_index \cdot V_{PEP}}{[2 + (2 \cdot m\_index)]} \quad V_{LSB} = \frac{m\_index \cdot V_{PEP}}{[2 + (2 \cdot m\_index)]} \tag{24}$$

From these values it is possible to calculate a relative power difference between the carrier and the sidebands, which is the power offset required in establishing the required modulation in the *ESG*. This is shown in (25)

$$PwrOffset = 10 \cdot \log\left[V_{FC}{}^{2}\right] - 10 \cdot \log\left[V_{USB}{}^{2}\right] \tag{25}$$

The next stage is to calculate the average power needed in order to establish the required PEP at the modulation depth used. This power will be the sum of the powers due to the voltage components in (24) into 50 Ω, and is given by (26) This is the value used to set the *ESG 'front panel'* power.

$$P\_ESG = 10 \cdot \log\left[\frac{\left[V_{FC}{}^{2}\right]}{100} + \frac{\left[V_{USB}{}^{2}\right]}{100} + \frac{\left[V_{LSB}{}^{2}\right]}{100}\right] \tag{26}$$

5.1.3 A multiple port, multiple stimulus Doherty measurement system

5.1.3.1 Analysing the requirements

A range of new measurement requirements had emerged from extensive single-tone analysis and characterisation, which had significant hardware and software implications for the evolving Doherty measurement system. The most significant of these concerned the synthesis of independent RF input excitations, and the control of their relative phase and magnitude, along with *main* and *auxiliary* bias voltages. It has been shown in [31] how establishing these parameters as custom functions of input drive can provide an optimisation approach for the Doherty PA. It was shown for instance that efficiency can be maximized by dynamically adjusting the relative input phase in response to the magnitude of the input drive. The consequence of integrating this approach in to the modulated measurement system was that any synthesised control of the *auxiliary* or *main* device needed to be in direct and immediate response to the instantaneous magnitude of the applied modulation.

5.1.3.2 Aligning phase

The single-tone phase synchronization and alignment problem discussed earlier in this chapter had now expanded to include not only synthesised RF components, but critically the various base-band components that would need to be generated in order to support the different variations of the Doherty that were planned. These included dynamic bias signals for the adaptive-bias Doherty realisations, some form of dynamic amplitude control for the input-attenuation Doherty, as well as dynamic phase control for perturbation and optimisation of relative input phase.

The correct phase-alignment and synchronisation of the various synthesised RF and base-band signals was essential, both relative to each other and to the applied modulation envelope. This became the significant and underlying technical challenge in this phase of work.

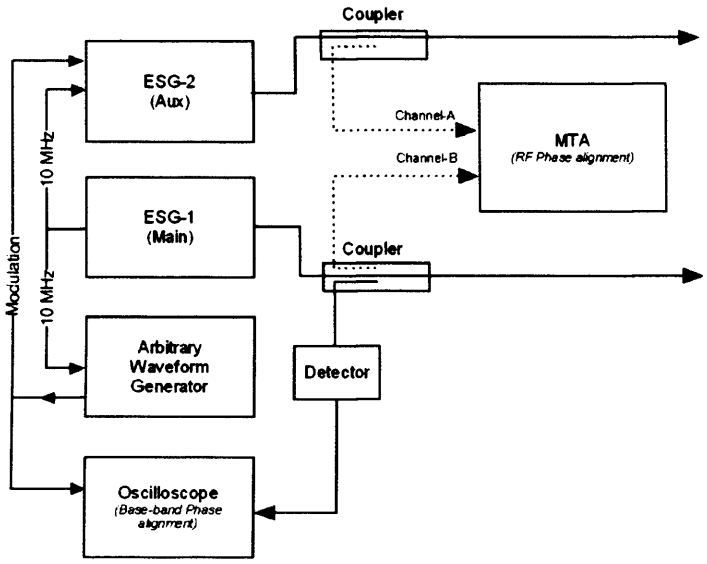


Figure 113 – envelope alignment using detected envelope

Initially, a simple approach was adopted and is shown in Figure 113, where before applying modulation, the two RF signals were aligned using the MTA and the approach discussed in Chapter 4. The required two-tone modulation was then established using the AM functionality of the *main* signal source *(ESG-1)* and the instantaneous envelope magnitude was monitored using a simple coupled power detector. A low frequency Arbitrary Waveform Generator (AWG) was used to synthesise a modulation signal possessing the necessary frequency, amplitude and DC offset, which was then applied to the Low Frequency (LF) modulation input of the *auxiliary* signal source (*ESG-2)* as AM modulation. Envelope alignment involved using a digital storage oscilloscope to capture and download both the detected and synthesised base-band waveforms, and using simple FFT processing, which was implemented as part of the IGOR control software, comparing the fundamental phase of these waveforms. The phase of the AWG was then adjusted such that *main* and *auxiliary* envelopes were phase coherent.

Although the simple diode detector is very effective in the detection of RF amplitude, it cannot measure RF phase. This leads to a limitation in this approach when used with two-tone excitation as the output voltage of the diode detector will resemble a full-wave rectified waveform, whilst the modulation is a zero-centred sine wave. There is therefore an ambiguity that exists as the fundamental component of the detected signal will be twice

the frequency of the applied modulation. It therefore becomes impossible to determine which half of the full-wave rectified detector output corresponds to the positive half of the modulation, and which corresponds to the negative half.

Another problem with this approach is the unavoidable non-linearity that is introduced into the modulated excitation due to the analogue AM mixer within the *auxiliary ESG*. Although this is a high quality instrumentation based mixer, any non-linear behaviour introduced at this stage is clearly non-ideal and will negatively impact the accuracy of any future linearity measurements.

The first of these problems can only be avoided by moving away from the use of traditional two-tone excitation and removing the associated ambiguity. Figure 116 shows a pure 2-tone modulation envelope together with its representative base-band modulation signals. On examination of the spectral composition of the RF envelope, it is clear that there will be very little or no energy at the modulation frequency.

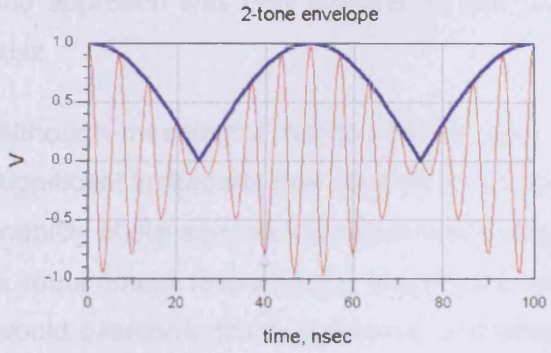


Figure 114 – two-tone envelope and ideal detector output

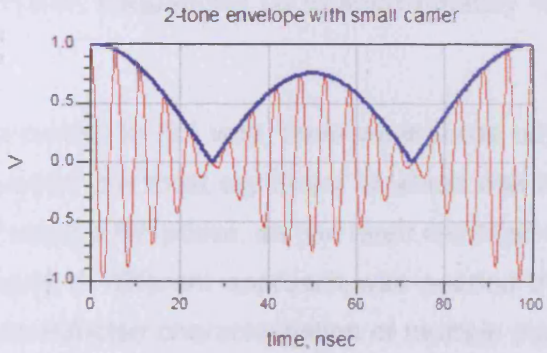


Figure 115 – modified two-tone envelope and ideal detector output

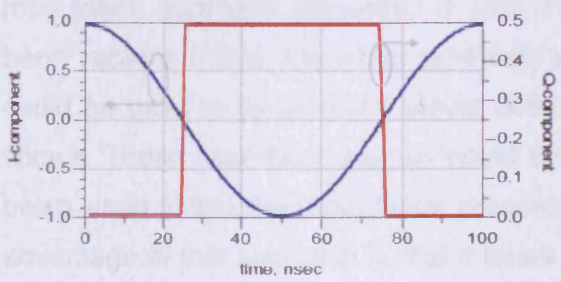


Figure 116 – I and Q component signals

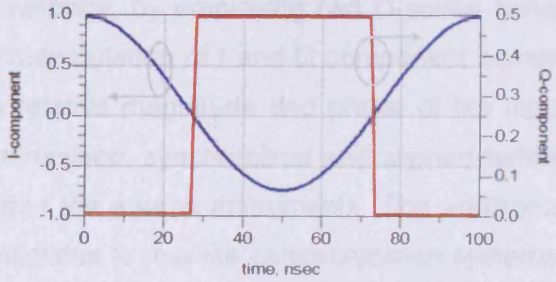


Figure 117 – I and Q component signals of modified envelope

This is to be expected as two-tone modulation is a form of Double Side-Band, Suppressed Carrier (DSB-SC) modulation that has sidebands at frequencies Fc-Fm and Fc+Fm, thus giving a tone spacing of 2Fm, which is reflected in the observed base-band signal. The lack of Fm component in the base-band detected envelope signal makes reliable alignment with the original modulation impossible. Figure 117 shows the case where a small amount of carrier is introduced to the modulation, effectively synthesising three-tone excitation. This addition establishes a tone spacing equal to Fm, which in turn generates a small amount of Fm component in the base-band detected envelope waveform. This small additional frequency component was effective in allowing the *auxiliary* base-band modulation to be aligned with the *main* modulated carrier.

An additional problem in using the detected envelope for synchronization includes delay and frequency dependent attenuation. The delay is introduced into the detector output waveform due to the frequency dependent behaviour of the element, which is essentially an RF diode coupled with a low-pass filter. The consequence of these limitations was that the approach was only suitable for low modulation frequencies up to approximately 100 kHz.

Although meaningful measurements were conducted in this way, there were some other significant limitations that needed to be addressed; the most significant of which was the inability of the approach to dynamically adjust relative RF phase, as had been identified as a requirement following the single-tone analysis. A different approach was needed that would overcome these problems, and allow unrestricted characterisation of multiple input Doherty structures.

Whilst analysing these problems together with the direction the research was taking, it was clear that most of the observed issues could be resolved by moving to a base-band modulation approach discussed in [45]. For instance, by employing two D-series base-band capable *ESG*s, the direct synthesis and manipulation of I and Q component signals could be used to dynamically adjust both the relative magnitude and phase of the input stimuli. These base-band signals could be synthesised, synchronized and aligned before being used within the modulation process within the source instruments. The additional advantage of this approach is that it bears similarities to real-life communication systems, where access to such base-band elements of the modulation process may well be an option.

Instead of detecting the modulation only after it has occurred, the base-band I and Q component signals produced by the *main ESG* could be used directly to describe the

instantaneous magnitude and relative phase of the modulation envelope delivered to the input of the Doherty's *main* device. Through careful choice of modulation, the phase or quadrature components can be minimised. For example, using three symmetrical tones to synthesise pure, classical AM allows the I-component alone to be used as a reference and to fully describe the magnitude of the modulation envelope delivered to the *main* device. The advantages of this approach over the previous AM based approach are numerous, and include a much higher modulation bandwidth, allowing modulation frequencies up to tens of MHz to be used, as well as providing a signal with improved spectral purity due to the use of I-Q modulation as opposed to the earlier AM modulator approach. The additional and significant advantage that must be stressed is the ability to employ I & Q component signals to dynamically control both the relative input magnitude and the relative input phase of the modulated excitation delivered to the Doherty.

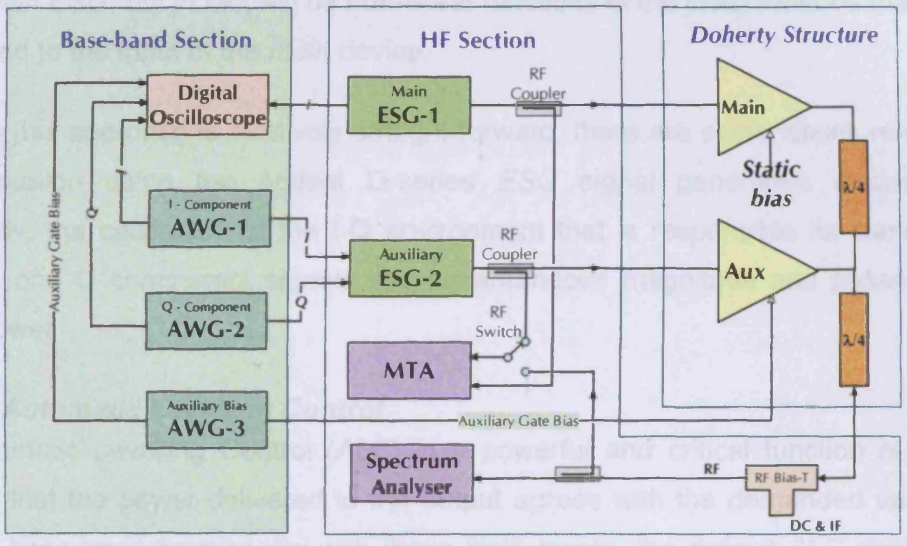


Figure 118 – measurement system with full base-band control

5.1.3.3 Using I & Q component signals to synthesise co-phased modulation

In this approach, the '*main*' signal source (*ESG*-1) is equipped with real-time base-band functionality, and is used as a 'master' instrument, establishing the required modulation, and generating I and Q component signals describing the modulated RF signal delivered to the *main* device. The '*auxiliary*' signal source (*ESG*-2) is effectively a 'slave' instrument that accepts I and Q signals and uses them to create *auxiliary* modulation of the required magnitude and base-band phase. Both sources are linked using the standard 10 MHz synchronisation signal, with RF phase alignment being achieved using the approach discussed in chapter 4.

A number of different Doherty realisations needed to be supported that included adaptive-bias and input-attenuation. Adaptive-bias, as its name suggests relies upon dynamically adapting the *auxiliary* bias voltage in response to the instantaneous modulation envelope magnitude applied to the *main* device. As full control is achieved through bias, the *auxiliary* and *main* modulated stimuli can be identical. This is convenient from a base-band excitation perspective as it can be achieved by directly connecting I and Q component outputs from *ESG*-1 to I and Q inputs of *ESG*-2.

In realising the input-attenuation Doherty however, it is the *auxiliary* I and Q component signals that need to be synthesised, with bias for both *main* and *auxiliary* devices remaining static. As conduction is controlled through dynamic variations in the relative magnitude of *main* and *auxiliary* modulated input signals, the I and Q component signals that need to be delivered to the *auxiliary ESG* are no longer identical to those generated by the *main ESG*, but in fact will be non-linear functions of the instantaneous magnitude of RF applied to the input of the *main* device.

Although this approach is relatively straight-forward, there are some issues relating to its implementation using the Agilent D-series *ESG* signal generators discussed, and specifically, the calibration of the I-Q environment that is responsible for translating the applied I and Q component signals into instantaneous magnitude and phase of carrier output power.

5.1.3.4 Automatic Levelling Control

The Automatic Levelling Control (*ALC*) is a powerful and critical function of the *ESG*, ensuring that the power delivered to the output agrees with the demanded value. When enabling base-band functionality with these instruments, the default *ALC* state is active and can cause a potential problem when using low modulation frequencies. When using external I and Q modulation, the *ALC* acts to hold the signal generators average output power at a constant level, regardless of variations in I and Q component signal inputs. Although rapid variations (>1kHz) in I and Q will cause the required modulation, slower variations will be considered as drift by the *ALC and* removed. The *ALC* can be thought of as possessing a high pass filter response with a corner frequency of 1 kHz.

5.1.3.5 Power-search

For modulation rates below 1 kHz and for the reason stated above, the *ALC* must be switched off and replaced by another means of maintaining output power accuracy. *Power-search* is an internal calibration routine that can be used by the *ESG* when *ALC* is disabled. Whereas *ALC* continually monitors and corrects the output power, power-search is a *'one-shot'* process, executed when required. When using external I-Q modulation,

power-search will scale the RF vector magnitude described by I and Q component signals against either an internal or external voltage reference. This is described in (27) which simply states that the magnitude of the applied modulation will be scaled according to the chosen voltage reference. Under normal circumstances, the *ESG* is configured to use a precise, internally generated 0.5V as the reference. In some circumstances however, it may be beneficial to use some other reference between 0 and 2V. This is made possible by using the '*external reference*' option which causes the *ESG* to perform a power search calibration based upon a reference that is calculated using the input I and Q component signals I_{IP} *and* Q_{IP}, as described by (28).

$$\sqrt{I^2 + Q^2} = Vref \tag{27}$$

$$Vref = \sqrt{I_{IP}{}^2 + Q_{IP}{}^2} \tag{28}$$

As an example, consider the case with no applied modulation and an applied I-component of +0.5V DC. Performing a *power search* using the internal reference will cause the *ESG* to accurately deliver the demanded power, set via the front panel. Any change in I-component DC value will cause a linear change in output voltage magnitude. This is illustrated in Figure 119 which illustrates how the ESG responds to a range of positive and negative I-component DC levels when using three different reference voltages. The internal reference was used for the 0.5V case, with external reference being used for the other two cases.

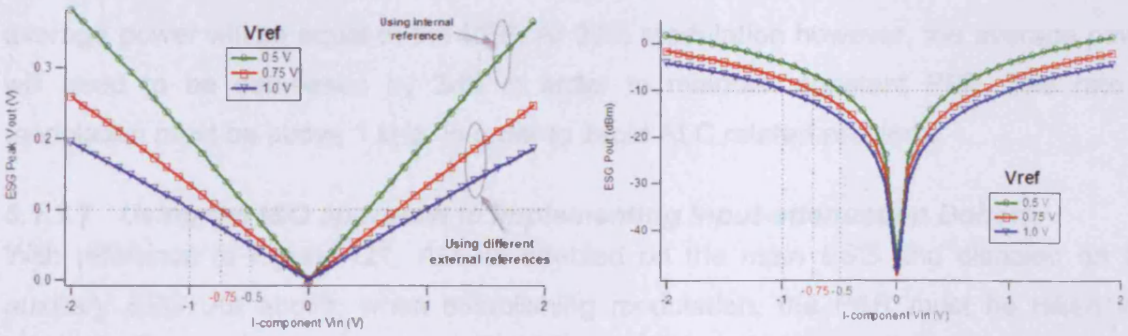


Figure 119 – I and Q scaling using ESG Power-Search calibration with both internal and external reference

If the *ESG* is now modulated by replacing the I-component DC value with a sinusoid voltage ranging between 0V and 0.5 V, a *power search* conducted in the same way using

the internal reference will cause the ESG to deliver a Peak Envelope Power (PEP) that is equal to the power set or front-panel power. It is important to note that the average power will be significantly lower.

In both of these examples, the output voltage will scale linearly with the voltage applied to the I-component input. It is important to note that if this same experiment was conducted with *ALC* on, the average output power would always agree with the set or demanded power, and would not respond as required to the applied I component drive.

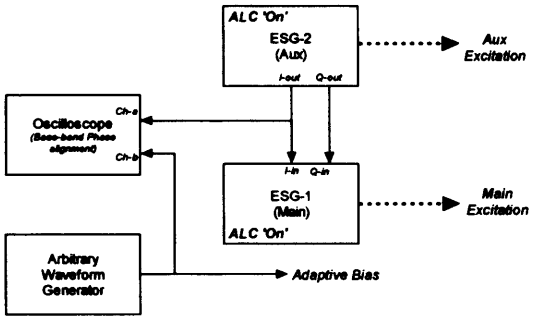


Figure 120 – adaptive-bias arrangement

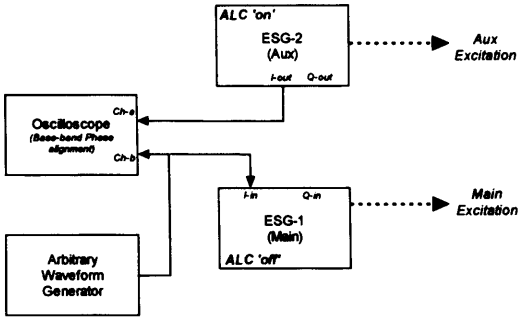


Figure 121 – input-attenuation arrangement

5.1.3.6 Using the I&Q approach to Implementing Adaptive-bias Doherty

With reference to Figure 120, the *ALC* on both *main* and *auxiliary* ESGs should be enabled. For a given average or 'set' *ESG* power, the value of PEP will increase as modulation depth increases. This increase will be according to the Peak to Average Ratio (PAR) characteristic of the modulation. Therefore, in order to achieve the required variable depth of modulation with a constant PEP, the average power of both ESGs must be decreased as the modulation depth increases. For example at 0% modulation, the average power will be equal to the PEP. At 33% modulation however, the average power will need to be decreased by 3dB in order to maintain constant PEP. The rate of modulation must be above 1 kHz in order to avoid ALC related problems.

5.1.3.7 Using the I&Q approach to Implementing Input-attenuation Doherty

With reference to Figure 121, *ALC* is enabled on the *main ESG* and disabled on the *auxiliary ESG*. As above, when establishing modulation, the PAR must be taken into account when realising a specific PEP for the *main ESG* modulation. As *ALC* is disabled on the *auxiliary ESG* and replaced with a power search method using the internal reference, the value of PEP will equal the power value 'set' via the front panel. Because of this, there is no need to reduce the average or 'set' power as described above, as the *auxiliary* modulation is scaled directly by the synthesised *auxiliary* I-component signal.

5.1.3.8 Controlling base-band impedance

Earlier developments resulted in a measurement system that allowed investigations into the single-tone and modulated behaviour of classical, input-attenuation and adaptive-bias Doherty structures. During the linearity measurements significant asymmetry was observed in the side-band carrier components. Following further investigation of this asymmetrical behaviour, it was found that ill-defined impedances presented to the low frequency IF components were the major contributing factor.

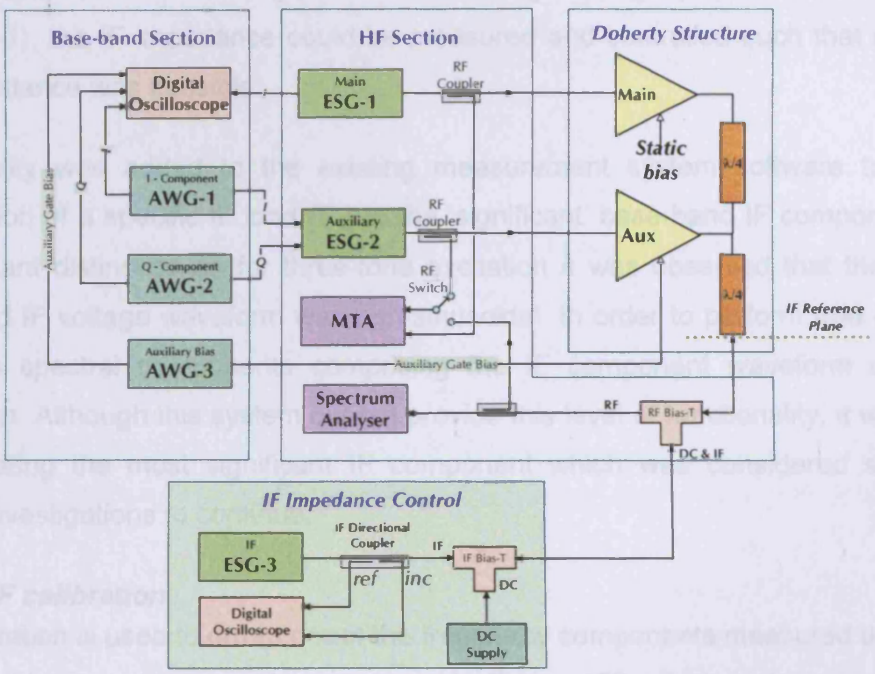


Figure 122 – complete multi-port measurement system

This was quickly remedied with the addition of a large decoupling capacitor to ground on the drain bias network, designed to present a short circuit condition to the low frequency IF component. This has previously been demonstrated, in traditional PA designs to be the optimum IF load condition for linearity [56].

Considering the observed effects, the possibility arose that the Doherty structure was particularly sensitive to the impedance of the low frequency bias network used. It was thought that this sensitivity was due to the *main* device output voltage remaining in close proximity to the *main* device knee-region, throughout the upper portion of dynamic range. Whilst in this state, any excursions or 'wobble' of the dynamic load-line, for instance due to DC supply re-modulation or electrical memory effects [57] would be more likely to cause the output voltage to interact with the knee region and linearity to degrade. Initial investigations and supporting simulations suggested that this was indeed the case, and

reinforced the argument that the linearity of the Doherty structure may be more sensitive to variations in base-band impedance than an equivalent 'conventional' amplifier.

In order to further investigate this idea through measurement, a further enhancement of the measurement system was necessary, which was to include IF load-pull and measurement capability similar to that used in [56]. This comprised a second, low frequency oscilloscope, a low frequency signal source, IF bias network and IF directional couplers and is shown in Figure 122. Following a single-port calibration step (see Appendix-1), the IF impedance could be measured and controlled such that perturbation of IF impedance was possible.

Functionality was added to the existing measurement system software to allow the presentation of a specific IF load (Γ_A) to the 'significant' base-band IF component. This is an important distinction as for three-tone excitation it was observed that the measured base-band IF voltage waveform was non-sinusoidal. In order to perform true IF load-pull, all of the spectral components comprising the IF component waveform would need termination. Although this system did not provide this level of functionality, it was effective in terminating the most significant IF component which was considered sufficient for linearity investigations to continue.

5.1.3.9 IF calibration

This calibration is used to error correct the frequency components measured using the low frequency bias network arrangement shown in Figure 122, which is described in detail in Appendix-1.

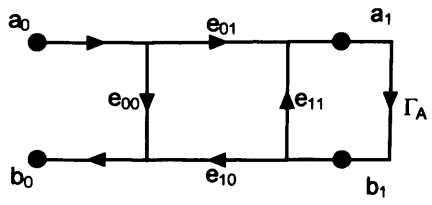


Figure 123 – signal flow graph representation of simplified IF arrangement

In summary, by using a simple one port, Short, Open and Load (SOL) calibration procedure the e_{00}, e_{0110} and e_{11} error terms can be computed. These terms can then be used in to calculate the actual IF load Γ_A measured at the output port of the Doherty structure.

$$\Gamma_A = \frac{\Gamma_M - e_{00}}{e_{10}e_{01} + \Gamma_M e_{11} - e_{00}e_{11}} \quad (29)$$

The calibration procedure used was verified by measuring s-parameters using an Agilent 8753 Vector Network Analyser (VNA). The VNA was calibrated to a known reference plane using the industry standard SLOT calibration and then one port connected to the system at the IF reference plane identified in Figure 122, and used to measure the impedance of a load synthesised by the developed measurement system.

5.1.4 Verification

5.1.4.1 System calibration requirements

In terms of calibration, the significant difference between modulated and single-tone systems is the additional complexity due to the introduction of base-band control.

It is important for instance that changes in synthesised I and Q components cause appropriate and expected changes in the relative and absolute instantaneous magnitude of the *main* and *auxiliary* modulation. For this reason, it is essential that the base-band calibration techniques discussed in section 5.1.3.3 be used, i.e. either *ALC* or *power-search*.

As well as employing the instruments own calibration capabilities, it is also important to validate correct behaviour of excitation prior to performing a measurement. This involved observing the *main* and *auxiliary* RF envelopes, and comparing to the ideal case. The adopted method was to initially use Agilent's ADS to simulate ideal excitations. This involved conducting a modulation depth sweep and observing both *main* and *auxiliary* envelopes both in the time and frequency domain.

Figure 124 shows the simulated base-band, envelope and spectral response of *main* and *auxiliary* excitation used in the input-attenuation approach at 52% modulation depth. One possible validation approach is to directly compare simulated and measured spectral behaviour of the modulated waveforms at each point in the modulation depth sweep.

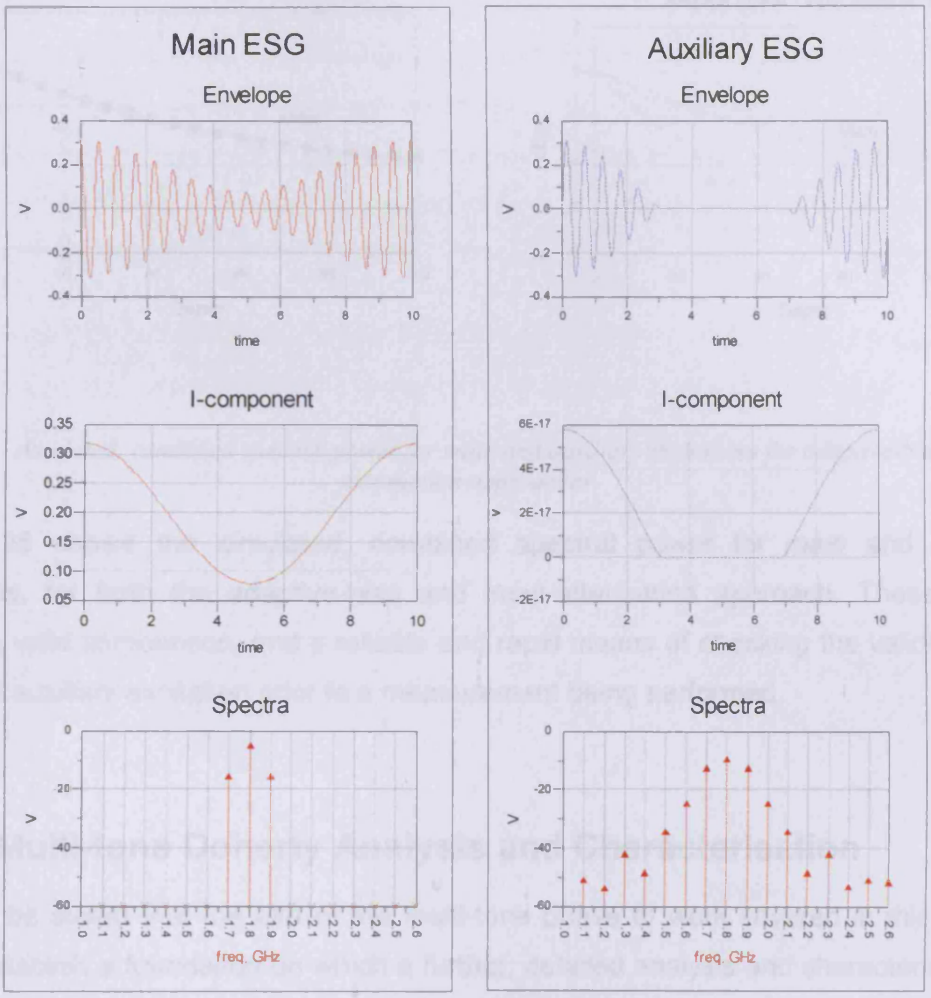


Figure 124 – RF envelope, base-band I component and spectral response of main and auxiliary excitation used in the input-attenuation approach at 52% modulation depth

Although this is possible in the case of the input-attenuation Doherty, the *auxiliary* excitation becomes 'pulse-like' at reduced input drive below the transition point. This is illustrated in Figure 124, where it can be seen that the *auxiliary* excitation can contain significant spectral complexity, making this type of measurement difficult and time consuming.

Another, more practical validation involves using a calibrated power meter to directly measure the combined spectral power or average envelope power of the modulated carrier, which will have very specific profiles when plotted as a function of modulation depth.

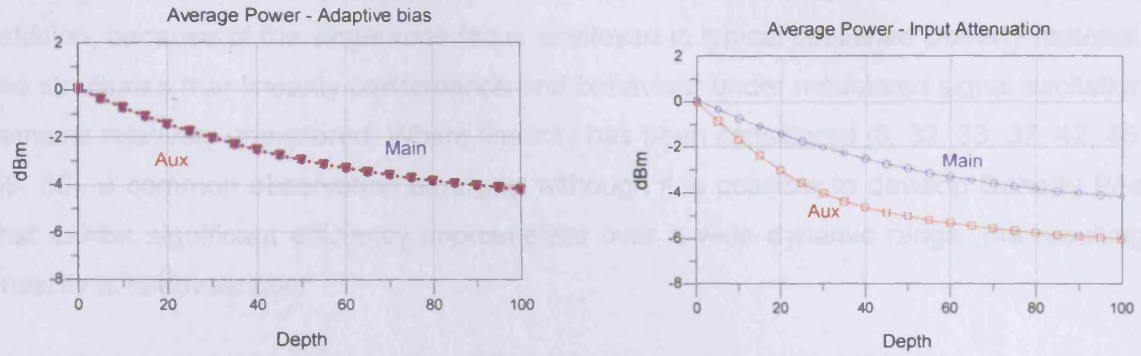


Figure 125 – simulated, combined spectral power for main and auxiliary excitations for adaptive-bias and input-attenuation approaches

Figure 125 shows the simulated, combined spectral power for *main* and *auxiliary* excitations, for both the adaptive-bias and input-attenuation approach. These curves provide a valid comparison, and a reliable and rapid means of checking the validity of the *main* and *auxiliary* excitation prior to a measurement being performed.

5.2 Multi-tone Doherty Analysis and Characterisation

It should be stated that the aim of the multi-tone phase of work covered in this chapter was to establish a foundation on which a further, detailed analysis and characterisation of measured Doherty linearity could be based, and not the analysis itself. This specifically involved the development of a multi-tone measurement system and measurement approach, the use of which in more completely characterising Doherty linearity will form part of the future work definition. Having said this, some theoretical and model-based analysis work has been conducted together with some modulated measurements to validate the functionality of the measurement system, and is presented here.

This chapter is written in two parts: the first section aims to explore, develop and analyse Doherty linearity by building upon basic Doherty principles, the use of simple simulation and in particular, through the visualisation of modulated interaction within the structure in the envelope domain. The second part aims to illustrate through more realistic simulation and measurement how the issues of linearity and limited bandwidth are closely coupled and together, conspire to limit the linearity performance of the Doherty structure.

5.2.1 A practical analysis of ideal classical Doherty linearity

The fact that the Doherty is theoretically a linear structure [22] is often overlooked. In addition, because of the single-tone focus employed in typical published Doherty material, the structure's true linearity performance and behaviour under modulated signal excitation remains relatively unexplored. Where linearity has been considered [8, 32, 33, 37, 42, 45, 59, 60], a common observation emerges: although it is possible to develop Doherty PAs that exhibit significant efficiency improvement over a wide dynamic range, the resulting linearity is relatively poor.

In the first part of this analysis, the IGOR software environment [26] has been used as a simulation tool for ideal analysis. This approach was considered sensible as it allowed Doherty behaviour to be explored at the most fundamental level, using highly idealised device models.

5.2.2 Creation of 3-tone modulation

The first step in this analysis involved synthesising pure, 100% Amplitude Modulation (AM) as a suitable modulated excitation. A simple IGOR function was written that produced an envelope of specific Peak-to-Min Voltage Ratio (PMVR) with a maximum magnitude normalised to unity, as shown in Figure 126 and Figure 127.

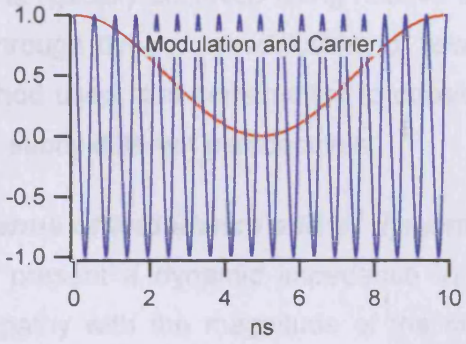


Figure 126 – modulation and carrier

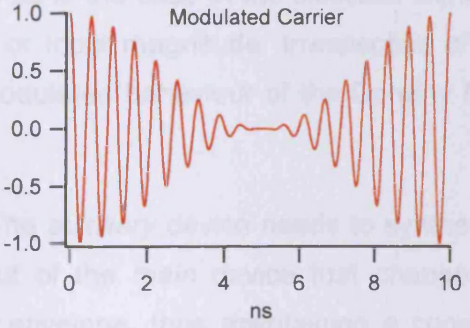


Figure 127 – envelope following multiplication

This pure AM can be considered as identical to that which is used in the multi-tone measurement system and other ADS simulations, where it is synthesised using three-tones of specific frequency spacing and relative magnitude. For this ideal analysis a carrier frequency (Fc) of 1.8GHz has been used, together with a high modulation frequency (Fm) of 100 MHz in order to allow good visibility of both carrier and envelope components in the time domain.

5.2.3 Achieving Doherty behaviour

For this analysis, the conventional classical Doherty schematic is presented in a slightly different form as shown in Figure 128 and comprises a single modulated source, which is used to drive both *main* and *auxiliary* branches of the Doherty structure.

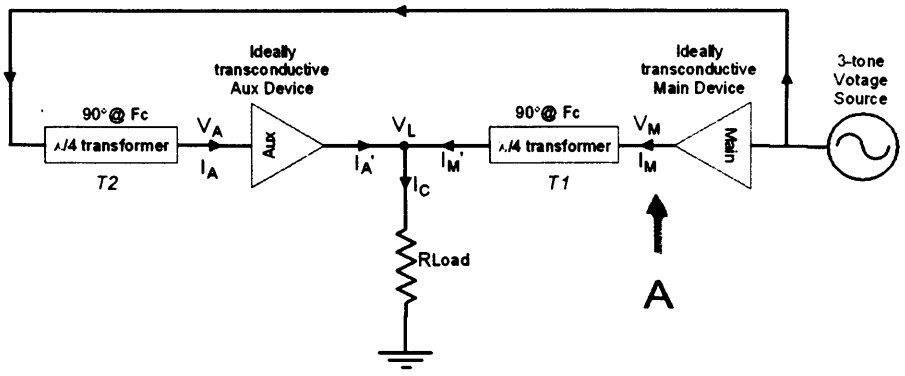


Figure 128 - alternative Doherty schematic

When considering modulated Doherty behaviour, an intuitive starting point is to focus on the impedance environment that needs to exist at the output of the *main* device. This is a function of the instantaneous envelope magnitude and must cause a constant voltage, high efficiency state to exist over the entire high-power region of operation. Synthesising the necessary dynamic impedance environment is the primary role of the *auxiliary* device and is typically achieved using relative static bias as is the case in the classical Doherty, or through dynamic modification of relative bias or input magnitude. Irrespective of the method used, it is constructive to consider the modulated behaviour of the Doherty from two, subtly different perspectives:

In terms of impedance and of dynamic load: The *auxiliary* device needs to synthesise and present a dynamic impedance to the output of the *main* device that changes in sympathy with the magnitude of the modulation envelope, thus maintaining a constant voltage swing in the high-power region of operation.

In terms of voltage, current and active load-pull: The *auxiliary* device needs to generate an output RF current envelope with specific phase and magnitude properties such that when transformed to a voltage through the *main* λ/4 combining element (T1), it partly cancels the *main* device voltage waveform, thus maintaining a constant *main* voltage envelope throughout the high power region of operation.

Figure 129 and Figure 130 show the normalised base-band *auxiliary* current and dynamic load waveforms that must exist, and that are ideal functions of the original 100% AM modulation signal magnitude shown in Figure 127.

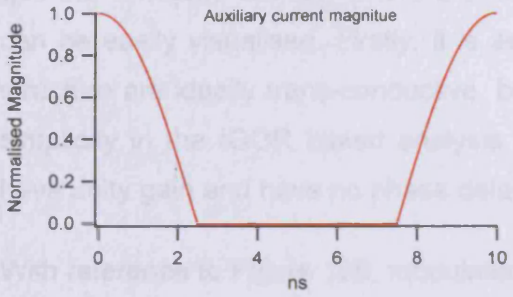


Figure 129 – auxiliary current profile

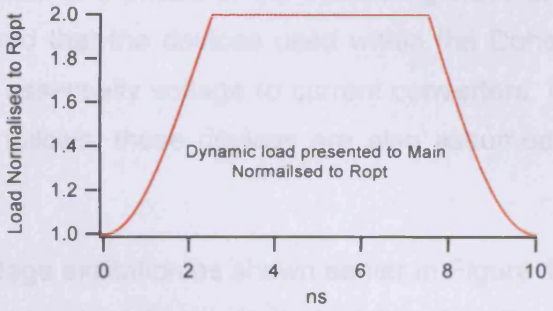


Figure 130 – dynamic load (normalised to Ropt)

By plotting these base-band waveforms against the voltage magnitude of the original modulation signal, the envelope transfer characteristics can be obtained and are presented in Figure 131 and Figure 132.

Although the dynamic load approach is useful in the simulation domain where the direct synthesis of dynamic impedance is straight-forward, in terms of practical

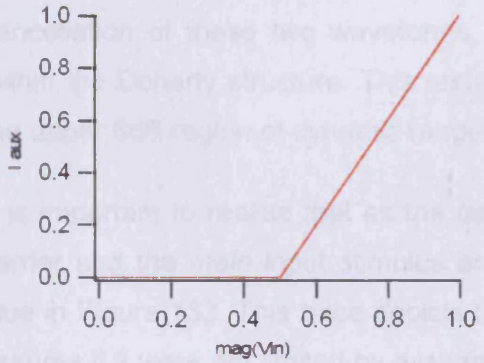


Figure 131 – auxiliary current vs. input voltage magnitude - transfer characteristic

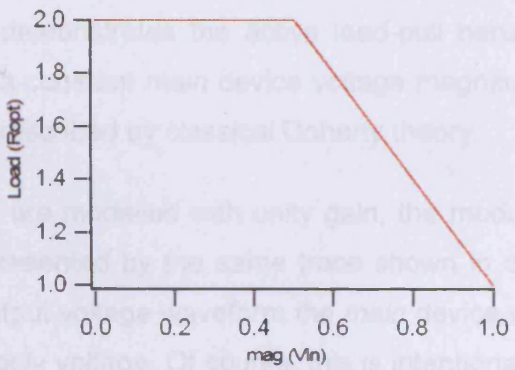


Figure 132 – dynamic Load vs. input voltage magnitude - transfer characteristic

realisation of Doherty structures and Doherty measurement systems, it is more appropriate to consider the active load-pull approach however and the concept of synthesising *auxiliary* device envelopes containing RF current waveforms of the correct phase and amplitude prescribed by the dynamic transfer function in Figure 131 above.

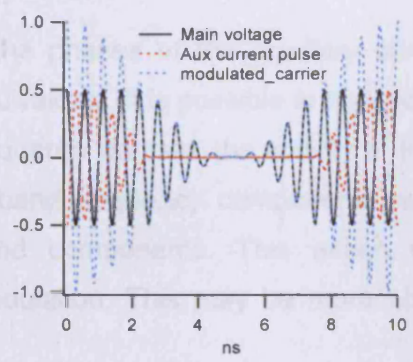
5.2.4 Envelope analysis

5.2.4.1 Doherty interaction in the envelope domain

To fully appreciate the modulated activity within the Doherty structure, it is constructive to use the envelope domain where the magnitude and phase of the interacting waveforms can be easily visualised. Firstly, it is assumed that the devices used within the Doherty structure are ideally trans-conductive, being essentially voltage to current converters. For simplicity in the IGOR based analysis that follows, these devices are also assumed to have unity gain and have no phase delay.

With reference to Figure 128, modulated voltage excitation as shown earlier in Figure 127 is generated by the source and following injection into the structure, is delayed by the λ/4 delay-line (T2) before passing on to the input of the *auxiliary* device. Here it is effectively converted to a current according to the *auxiliary* device transfer characteristic described in Figure 131, resulting in a 'pulse' of *auxiliary* RF current of the required profile. This current waveform then passes on to the output of the *main* device through the *main* λ/4 line (T1). A total of 180 degrees of phase shift is imparted on the fundamental component of the 'current-pulse' modulation, which ensures that the RF arrives at the output of the *main* device 180 degrees out of phase with the waveform generated by the *main* device effectively arriving from the other direction. Figure 133 shows the 'collision' and part-cancellation of these two waveforms, and demonstrates the active load-pull behaviour within the Doherty structure. This results in a constant *main* device voltage magnitude in the upper 6dB region of dynamic range, as prescribed by classical Doherty theory.

It is important to realise that as the devices are modelled with unity gain, the modulated carrier and the *main* input stimulus are represented by the same trace shown in dotted blue in Figure 133. This trace depicts the output voltage waveform the *main* device would assume if it were not limited by available supply voltage. Of course, this is intentional with the *main* device operating into a load of $2R_{opt}$ and achieving maximum-voltage and hence its high-efficiency state prematurely.



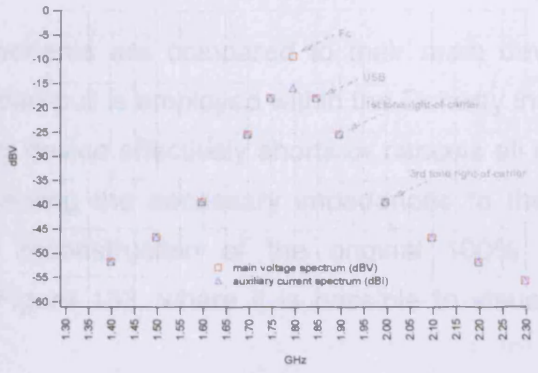


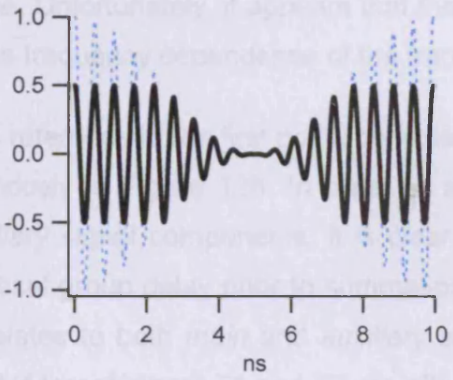
Figure 133 - envelope interaction at the main device output

Figure 134 – main voltage and auxiliary current spectral components (100% AM)

5.2.4.2 Spectral Behaviour

In order to better understand how the combination of the various signals within the modulated Doherty structure relates to overall linearity, the *main* device voltage and *auxiliary* device current time-domain waveforms that are present on opposite sides of the *main* combining transformer (T1) are calculated and shown in Figure 135 and Figure 136. These are then converted into the frequency domain and shown in Figure 134. Note that in the time domain plots, the dotted modulated carrier trace is added for reference only.

The immediate observation from Figure 134 is the *main* and *auxiliary* RF envelopes result in rich voltage and current spectra with components located at Fc ± nFm, where n is a positive integer. It is important to note that these spectra correspond to the inter-modulation frequencies for the modulation used. The significant observation however is the magnitude of the normalised *main* and *auxiliary* spectral components, which are identical with the exception of Fc, which differs in this case of 100% modulation by 6.6 dB.



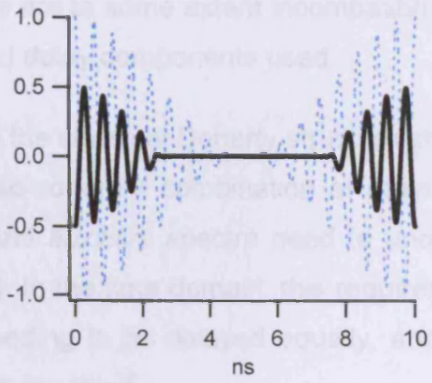


Figure 135 - main device output voltage envelope

Figure 136 - auxiliary device output current envelope

If the phases of the *auxiliary* current components are compared to their *main* device equivalents, it is possible to appreciate how load-pull is employed within the Doherty in the frequency domain: the activity of the *auxiliary* device effectively shorts or cancels all out-of-band frequency components, whilst presenting the necessary impedances to the in band components. This action results in reconstruction of the original 100% AM modulation. This may be more obvious in Figure 133, where it is possible to visualise

summation of the two time domain envelopes, resulting in a reconstructed AM envelope, which by definition will not contain any out of band frequency components.

In summary to this section, it is important to understand how the *main* voltage and *auxiliary* current waveforms combine at the output of the *main* device, resulting in a constant voltage, high efficiency state in the upper 6dB region of operation. It should also be clear that the *main* and *auxiliary* waveforms are spectrally rich with frequency components that are co-located with the inter-modulation frequencies. It follows that correct Doherty operation relies on the precise vectoral addition and subtraction of these components at the load, allowing the original modulation envelope to be accurately recovered. It is reasonable therefore to be concerned about this summing process and the implications to linearity if, for whatever reason, the various spectral current components are not correctly terminated and are allowed to develop voltage components at the load.

5.2.5 Bandwidth limitation of the Doherty

There are two distinct and equally valid design goals that exist for the Doherty structure that apply to both single-tone and modulated operation: the first is to achieve the correct phasing of *main* and *auxiliary* signals when they combine at the load, and the second is to achieve a constant *main* device output voltage magnitude in the upper 6dB of dynamic range. Unfortunately, it appears that these two goals are to some extent incompatible due to the frequency dependence of the transforming and delay components used.

With reference to the first point, consider once more the classical Doherty structure shown previously in Figure 128. In order to achieve phase-coherent combination of *main* and *auxiliary* signal components, it is clear that *main* and *auxiliary* spectra need to undergo identical group delay prior to summation at the load. In the time domain, this requirement translates to both *main* and *auxiliary* envelopes needing to be delayed equally, and the two λ/4 transformers T1 and T2 are effective in achieving this[12].

A different perspective is gained however if the activity at the output of the *main* device is considered more closely. Firstly, all frequency components of the modulated source signal entering T2 will be exposed to two λ/4 delays before emerging to load-pull the *main* device at point-A. This results in the carrier component being delayed by exactly 180 degrees and emerging with opposite phase to the fundamental component generated by the *main* device, which is exactly what is required to present the necessary impedance for correct Doherty behaviour. If the modulation around the carrier is considered separately however,

[12] *Note - if the auxiliary drive is being synthesised independently of main, then care has to be taken to ensure that both RF and modulation are delayed by the correct amount, i.e., 90 and (Fm/Fc)*90 degrees respectively.*

it is clear that the envelope will be delayed by (Fm/Fc)*180°, which in this example results in a 5° misalignment between the *auxiliary* and *main* RF envelopes at the output of *main* device.

It can be shown that the misalignment of *main* and *auxiliary* RF envelopes at the *main* device output results in 'miss-timing' of the *auxiliary* load pull effect, and as a consequence distortion of the expected constant magnitude *main* device voltage envelope. The magnitude of this distortion can be seen to increase with modulation frequency.

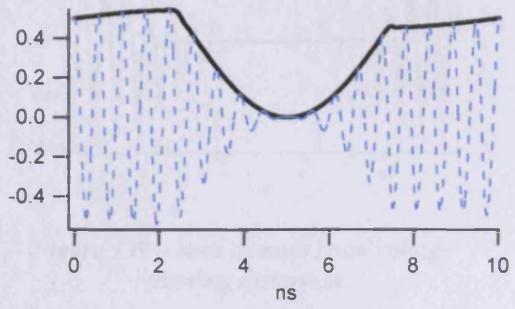


Figure 137 –main voltage envelope of classical Doherty structure

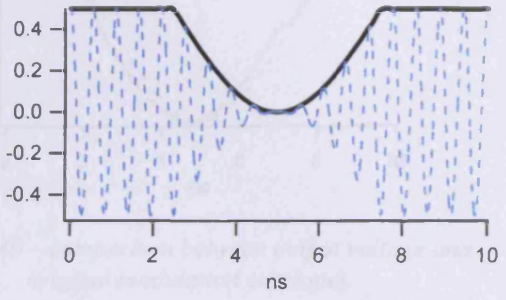


Figure 138 –main voltage envelope of following pre-distortion of auxiliary current pulse

The effect is illustrated in Figure 137 where in the first instance the delayed envelope arriving at the *main* device can be seen to produce significant distortion of the *main* output voltage envelope. This distorted voltage must ultimately propagate to the load and has a number of consequences and implications, including the worrying potential of increased proximity of the *main* device's load-line to its own knee region, risking increased and asymmetrical inter-modulation distortion.

In order to explore ways of countering this effect, the *auxiliary* envelope was experimentally pre-distorted by introducing a phase shift of -(Fm/Fc)*90° to take account of the transformer delay, whilst the RF was left unchanged. It can be seen from Figure 138 that the constant voltage behaviour can be easily restored.

At first glance, it appears that the problem has been cured through phase pre-distortion. Unfortunately however, this was found not to be the case as the phase offset introduced into the *auxiliary* envelope resulted in another phase misalignment, this time at the load. When considering both extremes, no change in the overall linearity is observed in terms of the magnitude of residual[13] frequency components. Pre-distorting the *auxiliary* current

[13] The term 'residual' is used here to describe voltage spectra that remain following the non-ideal vectoral cancellation process described earlier in this chapter.

pulse can therefore be considered as shifting the problem from one side of transformer T1 to the other, and not as improving the overall linearity. In other words, the problem either exists at the *main* device, or at the load, or at both.

One possible advantage of engineering the constant voltage at the *main* device however is it reduces the risk of the *main* device output voltage interacting with the knee region, and hence may offer an improved linearity / efficiency trade-off.

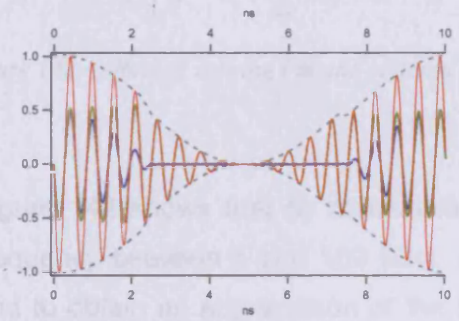


Figure 139 – time domain Load voltage showing distortion

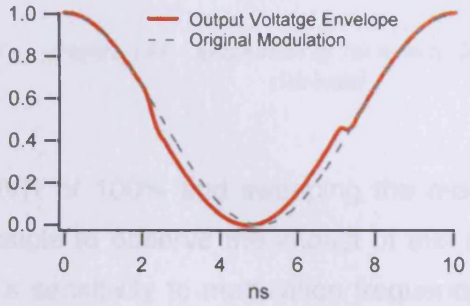


Figure 140 – comparison between output voltage and original modulation envelopes

Looking more closely at the summing of these components at the load, the distortion caused by the misaligned envelopes becomes more obvious, and can be seen in Figure 139 as a 'kink' in both sides of the load voltage envelope caused by the asymmetrical *main* voltage envelope, which is clearly visible through the comparison of the original modulation with the output voltage envelope Figure 140.

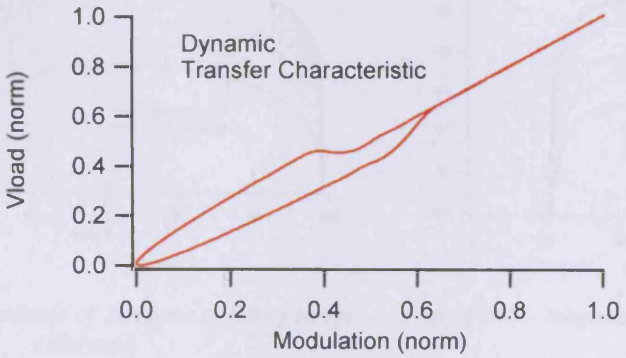


Figure 141 –Doherty transfer characteristic showing distortion

By taking this one step further, and extracting the envelopes for both the original modulation waveform and the output envelope, it is possible to illustrate the distortion by plotting the dynamic transfer characteristic.

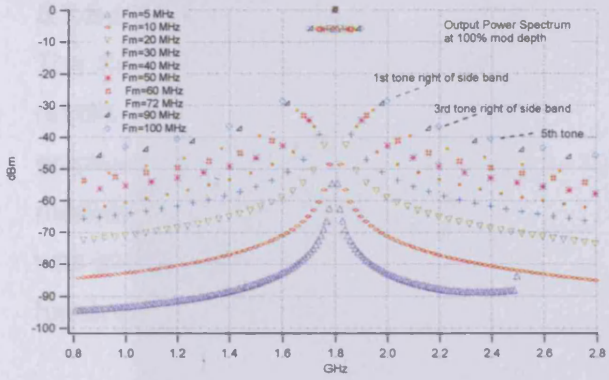


Figure 142 – effect of varying Fm and residual distortion

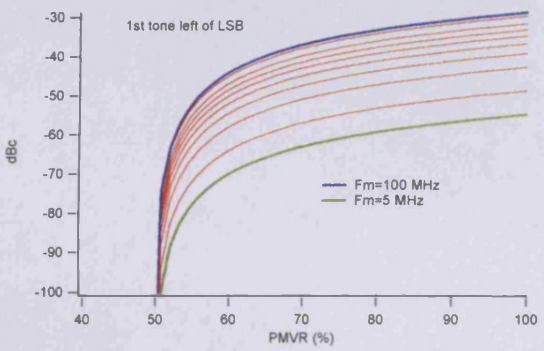


Figure 143 – magnitude of 1st tone to left of lower sideband

Figure 142 shows that by maintaining a PMVR of 100% and sweeping the modulation frequency between 5 and 100 MHz, it is possible to observe the impact of this problem and to obtain an appreciation of the Doherty's sensitivity to modulation frequency. What emerges is interesting, and shows patterns of behaviour in the residual tones, which can be seen to increase in magnitude with modulation frequency. By sweeping both PMVR and modulation frequency, it is also possible to gain an idea of the growth of residual tones for different values of modulation frequency. Figure 143 to Figure 145 for instance show the response to modulation frequencies ranging between 5 MHz and 100 MHz for values of PMVR ranging between 40% and 100%.

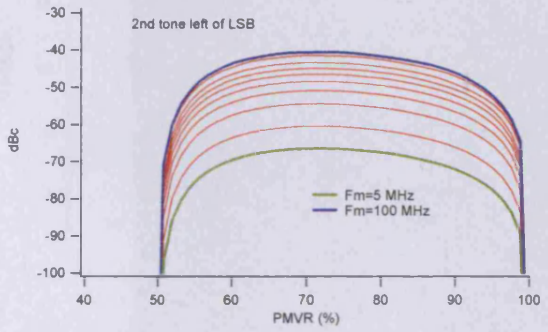


Figure 144 – magnitude of 2nd tone to left of lower sideband

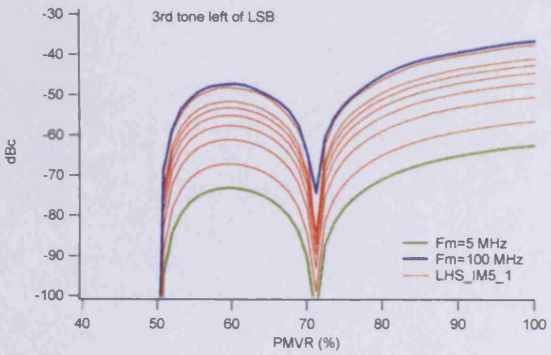


Figure 145 – magnitude of 3rd tone to left of lower sideband

5.2.6 Corroboration of theory through ideal ADS simulation

So far in this analysis, all simulation of Doherty behaviour has been conducted through ideal concepts, implemented using the IGOR programming language. In order to bring this ideal analysis one step closer to reality, a more realistic Doherty structure was simulated using ADS and relatively ideal device models.

5.2.6.1 Simulation Approach

The initial task was to demonstrate some parity between the simple IGOR experimental results, and those generated by a more realistic but still relatively ideal ADS simulation employing an input-attenuation Doherty approach. Using a pure AM excitation with a modulation frequency of 10 MHz in both ADS and IGOR simulations, modulation depth was swept between 0 and 100 % and spectral re-growth around the carrier and side-band tones observed[14].

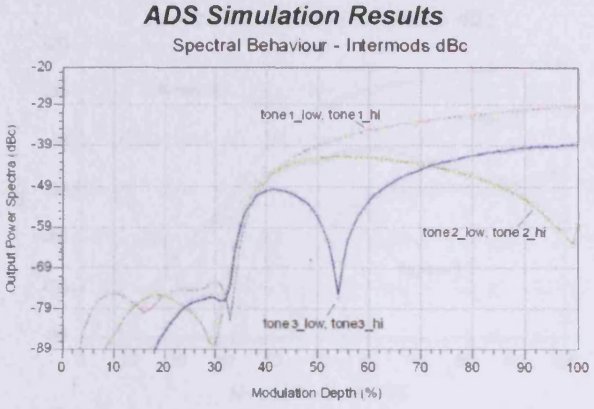


Figure 146 – tones around carrier (ADS simulation)

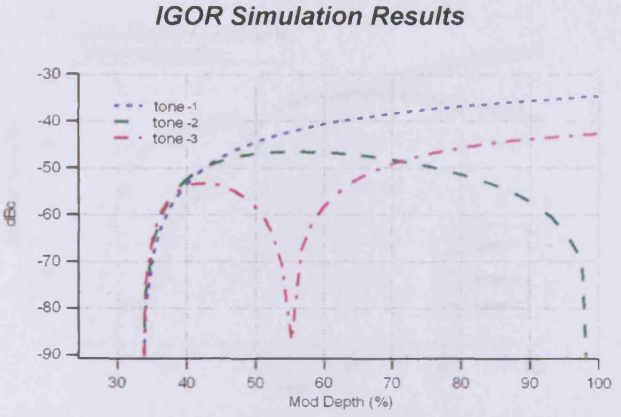


Figure 147 – tones around carrier (IGOR simulation)

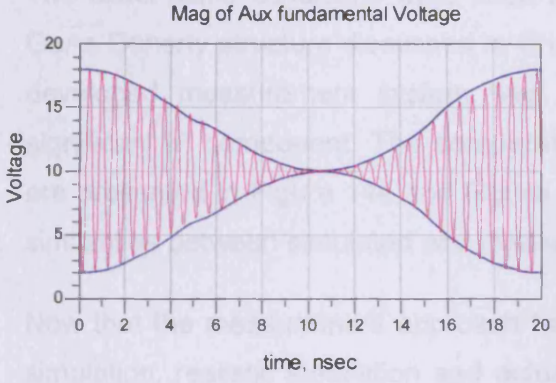


Figure 148 – output envelope (ADS simulation)

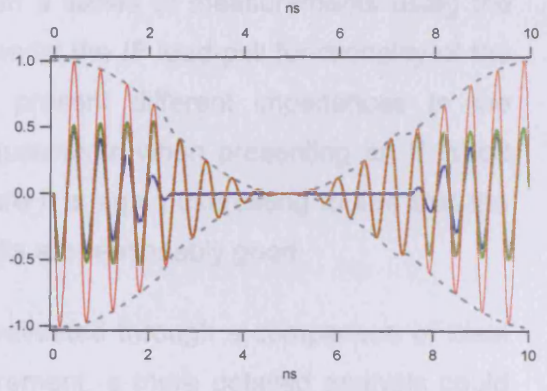


Figure 149 – output envelope (IGOR simulation)

The similarity between ADS and IGOR approaches is clear in both the frequency domain representations of Figure 146 and Figure 147, as well as in the time domain envelope representations of Figure 148 and Figure 149. Specifically the distortion is clearly visible in both instances of the RF envelope.

[14] For this analysis, spectral re-growth is defined in terms of tones either side of the carrier. For example, tone-1 refers to the first pair of tones closest to the side-bands, i.e. at Fc±2Fm, tone-2 to Fc±3Fm, and so on. This is the approach used in Figure 142.

5.2.7 Comparison of simulation and measured results

The final comparison presented here is between a further ADS simulation of the same adaptive-bias Doherty approach, but this time employing a vendor supplied models of a Fujitsu FLK-102XV FET device used for both *main* and *auxiliary* devices, which were both biased in class-B. The structure was excited by a 10 MHz modulation envelope of fixed PEP synthesised using the three-tone approach discussed earlier in this chapter, and with a modulation depth varying between 0 and 100%.

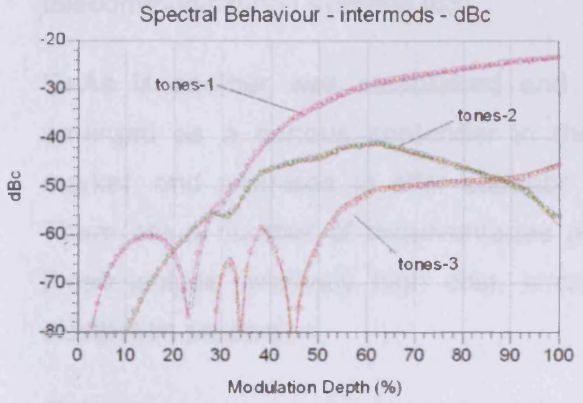


Figure 150 – tones around carrier (ADS simulation using vendor supplied model)

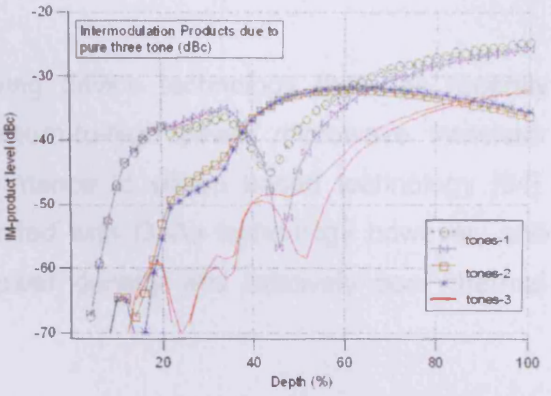


Figure 151 – tones around carrier (measured)

The exact same conditions were used to establish a series of measurements using the GaAs Doherty structure discussed in Chapter 2, whilst the IF load-pull functionality of the developed measurement system was used to present different impedances to the significant IF component. The comparative measurements when presenting an IF short are presented in Figure 144 and Figure 145, where it is again interesting to see that the similarities between simulated and measured results are reasonably good.

Now that the measurement approach had been validated through a comparison of ideal simulation, realistic simulation and actual measurement, a more detailed analysis could begin looking at the sensitivity of Doherty linearity to modulation frequency, testing the assertions made earlier in this chapter.

Chapter 6 Doherty Measurement Prototypes

There are a number of possibilities when considering potential device technologies for use within Doherty PA structures. For base-station applications, silicon LDMOS is a technology that continues to evolve and offer excellent performance and value for money, and tends to be the device technology of choice in commercial Doherty PA developments [36, 61, 62]. The ability of LDMOS to continue in its dominant role is debatable however in light of the power, speed, efficiency and linearity requirements of future-generation mobile telecommunications systems [63].

GaAs is another well established and evolving device technology that has recently emerged as a serious contender in the medium-to-high power microwave transistor market, and promises to offer superior performance to silicon based technology [64]. There are a number of disadvantages associated with GaAs technology however, and these include relatively high cost, limited power density and relatively poor thermal dissipation properties.

GaN based device technologies have for some time been generating significant interest in the microwave PA community due to a number of attractive characteristics that are highly relevant to efficient and linear PA design [65]. The high breakdown voltages associated with GaN technology leads directly to theoretically high linear efficiency and high output impedance. Other advantages include high power density, high maximum frequency, excellent thermal conductivity as well as impressive theoretical linearity [29, 66, 67]. These properties have perhaps unsurprisingly led to continued and intensifying interest in the development of high-voltage, high-power, high efficiency and high impedance microwave transistors offering theoretically at least four times the theoretical maximum output power density of GaAs and six times that of LDMOS [65, 68].

For a given required output power, the optimum output impedance (R_{opt}) differs for each device technology, and is an important design consideration. In Doherty design, this especially true as R_{opt} has large implications when realising the very specific output matching networks that are required. Table 4 illustrates how the different device technologies considered in this chapter compare in terms of typical optimum output impedance for comparable maximum output powers. This simple analysis is useful as a comparison, yet is approximate as it is based on ideal devices with little or no output capacitance and that exhibit little or no RF-DC dispersion[15].

[15] RF-DC dispersion describes those differences that are observed between measured DC and RF device behaviour.

GaAs devices for instance operate at low supply voltages below 15 Volts, and the large periphery power devices tend to demand high currents and hence generally possess relatively low optimum output impedance. It is shown for instance that the devices used within 10W and 100W GaAs Doherty realisations will typically have optimum output impedances of 6Ω and 1Ω respectively. This is in contrast to similar power GaN Doherty realisations where the devices would possess optimum output impedances of 100Ω and 10Ω respectively.

	Device Used within Doherty								
	LDMOS			GaAs			GaN		
P_{max} (W)	1W	10W	100W	1W	10W	100W	1W	10W	100W
V_d (V)	28	28	28	10	10	10	40	40	40
V_{knee} (V)	5	5	5	2	2	2	10	10	10
I_{max} (A)	0.08	0.90	8.70	0.25	2.50	25.00	0.06	0.60	6.00
R_{opt} (Ω)	**575**	**51**	**5**	**64**	**6**	**1**	**1000**	**100**	**10**

Table 4 – Doherty and device technologies

Devices with very low optimum output impedance can prove highly problematical when designing Doherty output matching structures, especially when using distributed topologies, where λ/4 transformers with similarly low characteristic impedances typically equal to R_{opt} will are required.

This chapter examines a number of different device technologies and their suitability to the Doherty application, and focuses on the design, fabrication, testing and initial characterisation of medium power (<2 Watt) GaAs and GaN structures. Other devices that have been considered in less detail include a MGF0951P Mitsubishi GaAs FET, an early generation Motorola MRF281 LDMOS FET and a Celeritek InGaP HBT.

A number of different measurement techniques are employed in the design and characterisation of the Doherty structures discussed. The use of load-pull and waveform measurement systems to synthesise 'Doherty-like' dynamic impedance environments around single devices is particularly interesting and relevant however, and is discussed in detail. This 'emulation' approach allows for device characterisation and optimisation under expected, operational conditions, and importantly provides extensive insight into device interaction within the Doherty.

6.1 GaAs MESFET Doherty

The CF015-11 medium-power GaAs devices that were used for this design were kindly supplied by Celeritek, UK. The MESFET devices have a 1200μm gate width and 0.25 μm gate length and are capable of delivering a maximum output power of 26 dBm. They employ Silicon Nitride passivation and are fabricated on ion-implanted wafers, and for these experiments were mounted in low-profile, low-parasitic Kyocera LCC-8 10-lead surface mount leadless ceramic packages. More detail on both the device and the packages is supplied in appendix-E.

6.1.1 Bias considerations

Whilst the design of the initial passive Doherty structure is initially discussed in Chapter 3, it was important to understand something about the active devices themselves. From pulsed DC measurements, these devices were found to pinch off at V_g = -1.5 V, have a knee voltage (V_k) of approximately V_d = 1 V and a maximum saturated current in excess of 400 mA at V_g = 0.5V. Pulsed measurements were conducted using a *DIVA* 250 system [69, 70], using a drain voltage of 5.5V, gate pulse width of 1 μs and an interval of 5 ms. The results of this measurement are shown in Figure 7.

From the manufacturer supplied information in Appendix-E and measured s-parameter data, the devices were known to possess significant low frequency gain with measured s_{21} at least 16dB at 2GHz. As a result, the devices had a tendency to oscillate, with stability analysis indicating that it was necessary to include a 10 Ω series resistance in the DC and RF path close to the input of the device.

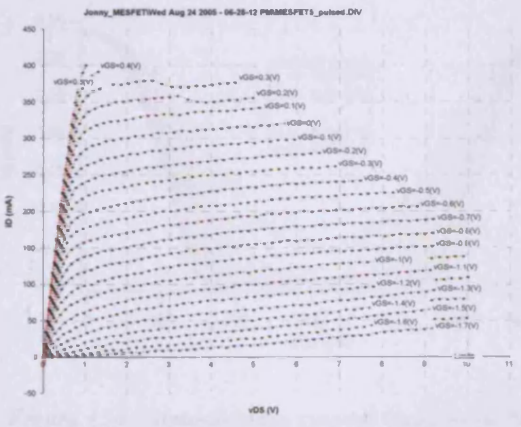


Figure 152 - CF015-11 MESFET – pulsed DC-IV characteristic (Vd=5.5V)

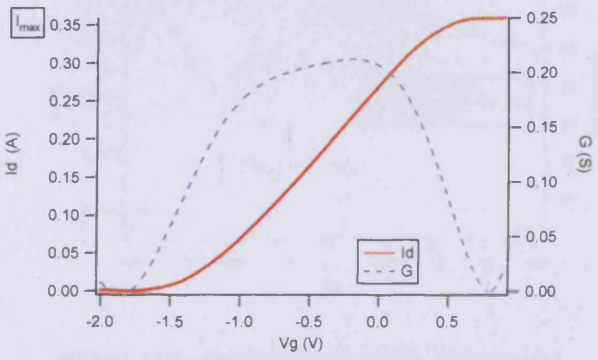


Figure 153 - CF015-11 MESFET transfer and trans-conductance characteristics at Vd=5.5V

Although this improved matters considerably, unpredictable behaviour, possibly due to the Gunn effect was still a problem at higher bias currents, which is evident from the small collapse observed in I_d at the top of the DC-IV curves show in Figure 7. This was found not to pose a problem under operational conditions however, when the devices were sited in the Doherty prototype structure. Conservative approximations of the V_g-I_d transfer characteristic and trans-conductance curves in Figure 153 were generated using a combination of measured DC data and imposed boundary conditions (for example, causing Imax to compress at 350mA). Curve-fitting functionality within the *IGOR* software environment [26] was then used to extract a 10 coefficient polynomial function, which was in turn used as the basis of a simple model in order to explore device linearity, efficiency and gain under varying bias and drive conditions.

The general aim of this initial simulation and analysis was to quickly gain an idea of how the devices would respond to excitation, and to decide upon appropriate bias conditions. The approach also allowed initial 'off-line' investigations to be conducted, whilst avoiding the risk of damage. This was particularly important due to the limited number of available devices, which had been specifically assembled for this project.

By linearly increasing the magnitude of the excitation applied to the model whilst decreasing the gate bias voltage, it was possible to generate output current waveforms with varying conduction-angle and constant maximum peak amplitude, as shown in Figure 154. This is similar to the ideal analysis presented by *Cripps* in [52] where an ideal '*strongly non-linear*' asymptotic transfer function is used in place of the actual measured device transfer function employed here.

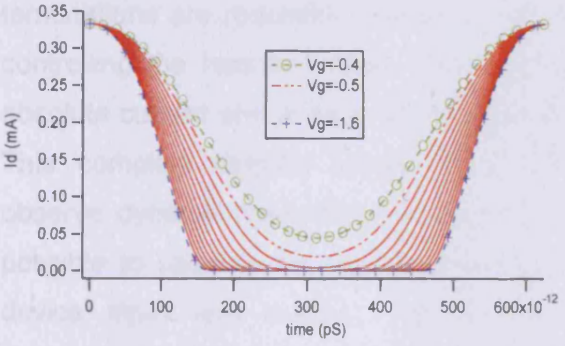


Figure 154 – time-domain current waveforms for Vg bias between -1.6V and -0.4V

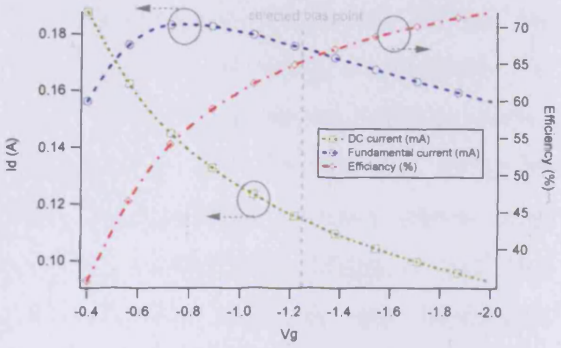


Figure 155 – fundamental and DC current and efficiency as a function of Vg

By analysing the current waveforms of Figure 154 in the frequency domain, it is possible to determine the expected harmonic behaviour of the device. Some useful results of this analysis are presented in Figure 155, Figure 156 and Figure 157 where it can be seen

that a gate voltage of Vg=-1.25V results in a class-B bias point that yields a current waveform giving a good compromise between unwanted harmonic generation, gain flatness, as well as reasonable maximum output power and efficiency.

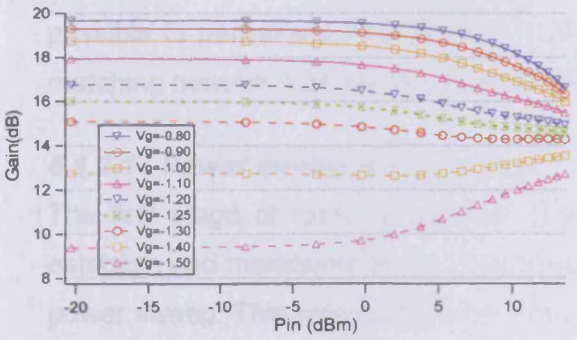


Figure 156 – gain flatness for different Vg as a function of P_{in}

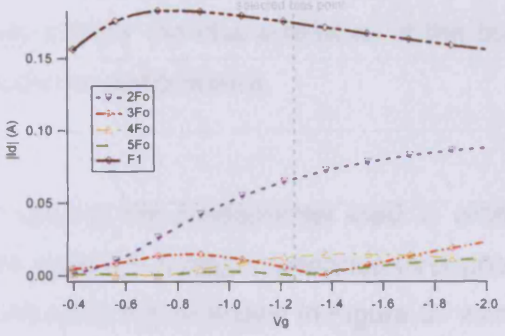


Figure 157 – harmonic current behaviour as a function of Vg

6.1.2 Using Load-pull and waveform measurement systems

Load-pull measurement systems are becoming increasingly popular tools in modern microwave PA design as they allow the optimisation and characterisation of device performance whilst operating into realistic harmonic load conditions. This is achieved through the synthesis of specific fundamental and harmonic termination impedances [46, 47, 71], with typical applications including measurements under constant load conditions such as power sweeps into optimum load impedance, measurements under varying load conditions such as those needed to generate contours of constant power, gain and efficiency, as well as measurements used to explore certain 'exotic' PA modes of operation such as class-E, class-F and inverted class-F, where very specific harmonic terminations are required in order to achieve the required device behaviour. As well as controlling the harmonic load, these systems crucially offer the ability to measure the absolute current and voltage waveforms that exist at the device or device package plane. This 'complete visibility' allows for '*waveform engineering*' [47, 71] and the ability to observe dynamic load-lines and dynamic transfer characteristics. In other words, it is possible to observe the various trajectories of the RF current and voltage at both the device input and output. The combination of harmonic load-pull and waveform measurement capabilities results in a powerful design approach that is particularly suited to Doherty design and optimisation.

It has been discussed in previous chapters how load-pull measurement systems can be employed to synthesise the drive dependent harmonic impedances and excitation conditions that exist within a specific Doherty structure, around either the '*main*' or single

'*auxiliary*' devices. Using this 'emulation' approach in combination with measured time-domain current and voltage waveforms, it is possible to optimise aspects of the Doherty design. More specifically, by understanding the ideal and realistic dynamic impedance environments that exist around both *main* and *auxiliary* devices within the Doherty, it is possible to perturbate, explore and to ultimately identify the characteristics of the output matching network that are required to deliver optimum performance.

6.1.2.1 Power sweep at R_{opt} (25 Ω)

The first stage of load-pull analysis involved varying the fundamental load in order to establish and maintain the previously calculated optimum output impedance throughout a power sweep. This was conducted using the calibrated fixture shown in Figure 37 with the device biased in the shallow class-B condition identified in Figure 155 and Figure 157. The resulting performance is shown in Figure 158 and Figure 159 and shows a reasonable agreement to the earlier analysis using the simple polynomial model. This simple power sweep into the assumed optimum load was necessary as a starting point, as well as to allow determination of the maximum drive conditions that would form the basis of a more detailed load-pull analysis involving automated measurements.

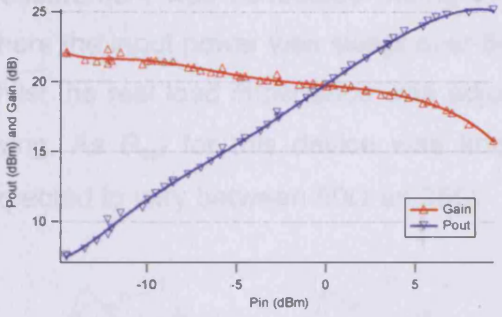


Figure 158 –P_{out} and Gain at optimum

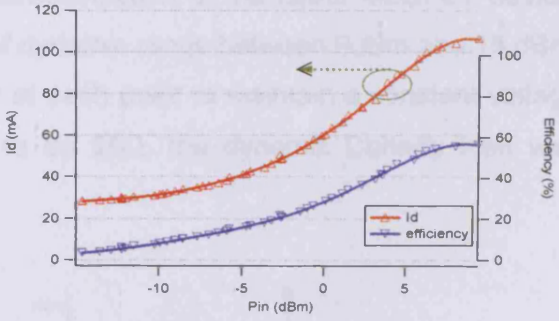


Figure 159 – efficiency and DC drain current at optimum

6.1.2.2 Synthesising Doherty conditions around a single 'main' device

As has been stated, one of the major advantages of using time-domain harmonic load-pull measurement systems for Doherty design is the access to measured voltage and current waveforms at the calibrated reference planes [72, 73]. Plotting the time-domain output voltage vs. output current waveforms allows the analysis of device behaviour through observation of dynamic load-lines. These are usually plotted relative to the devices boundary conditions or measured DC-IV behaviour, and are advantageous for a number of reasons: as has been seen, Doherty understanding is best developed through load-line

analysis, and specifically how the *main* and *auxiliary* device load-lines behave and influence each other.

In order to understand how to synthesise the impedance and excitation environments that exist within a Doherty structure, it is necessary to revisit and focus upon certain aspects of fundamental Doherty theory. In the Doherty's *low-power* region of operation where the *auxiliary* device is inactive, the *main* device load-line or output voltage swing expands normally with increasing drive towards the knee region. As the transition point is reached however and the high-power region is entered, the *main* device load-line is 'restrained' and prevented from entering the knee region, and instead, diverted upwards by the load-pulling action of the *auxiliary* device. In this region of operation and under ideal conditions, the *main* device expects to see a linearly decreasing load with increasing input drive voltage magnitude.

From this analysis, it follows that one way to synthesise the required dynamic impedance is to manually observe the *main* device dynamic load-line, and adjust the fundamental load such that the output voltage swing is maintained at a constant and pre-defined maximum, which approaches, but does not interact with the knee region. Such a measurement was conducted during the characterisation of the GaAs MESFET device, where the input power was swept over 6dB of dynamic range between 9dBm and 15 dBm, whilst the real load impedance was adjusted at each point to maintain a constant voltage swing. As R_{opt} for this device was known to be 25Ω, the dynamic Doherty load was expected to vary between 50Ω an 25Ω.

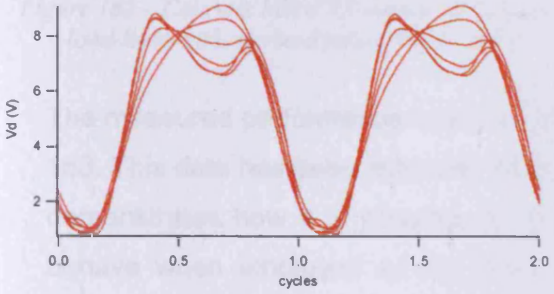


Figure 160 –drain voltage measured at each point in the power sweep between 9 and 15 dBm.

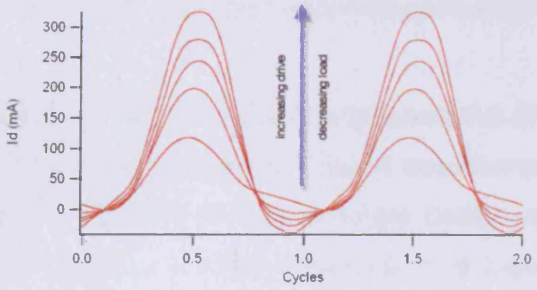


Figure 161 –drain current waveforms measured at each point in the power sweep between 9 and 15 dBm.

Interestingly however, although the optimum impedance was known to be 25Ω, the load required ranged between 75Ω and 20Ω, and is presented graphically as a function of input power in Figure 163, along with the resulting output power, gain and efficiency.

The measured voltage and current waveforms are shown in Figure 160 and Figure 161. Although the voltage waveforms are distorted due to non-optimal harmonic termination, it can be seen how the magnitude of the voltage waveform remains fairly constant whilst the class-B, 'half-wave' rectified current waveforms, although containing a significant displacement current contribution due to output capacitance, can be seen to increase in magnitude as prescribed by classical Doherty theory [21].

By plotting these waveforms as dynamic load-lines on the I-V plane along with the DC measurement data, it is possible to observe key performance related behaviour, including the proximity of the load-line to the knee-region boundary, as well as any evidence of RF-DC dispersion. This is illustrated in Figure 162 where it is clear for instance that the dynamic load-lines are where they are expected to be, in relation to the IV plane, and there is generally a good agreement between the boundary conditions revealed by the dynamic RF load-lines and those defined by the measured DC characteristics.

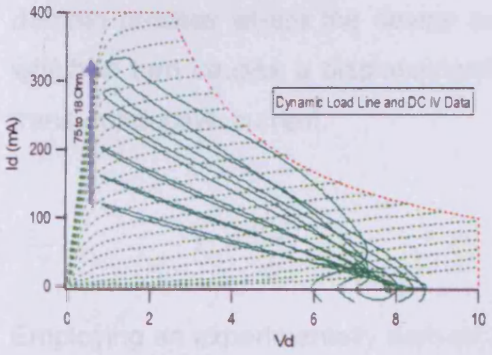


Figure 162 – Celiretik MESFET measured dynamic load-lines with overlaid pulsed DCIV data

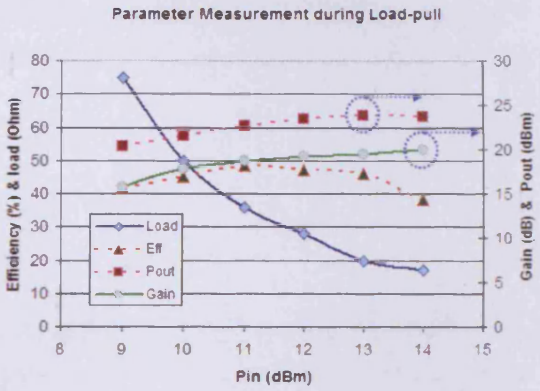


Figure 163 – measured performance parameters

The measured performance over 5dB of dynamic range at the input is presented in Figure 163. This data has been extracted from the measured voltage and current waveforms and demonstrates how it is possible to develop a good idea of how a single device would behave when employed as the *main* device within a Doherty structure. It is clear for instance that an efficiency plateau of between 40% and 50% is maintained over the entire dynamic range, whilst the output power exhibits the classical compression in the presence of non-compressive gain, which is another characteristic of Doherty *main*-device behaviour. It should be remembered that once embedded within the Doherty structure, this compressive power characteristic would combine with the expansive power characteristic of the *auxiliary* device, and theoretically result in overall linear behaviour.

One observation is that over an input dynamic range of 5dB, the load required to maintain a constant voltage swing ranges between 75Ω to 18Ω, which is far greater than the expected 2 R_{opt} to R_{opt} variation expected over 6dB. This is due to expansive gain of the device, and is an important design consideration that is discussed in more detail in chapter 3.

If the net parasitic capacitance and inductance associated with the package and bonding arrangement is small, and the calibrated reference planes can be defined physically close to the active device, as is the case with the packages used here, then it is possible, although not ideal to use the measured waveforms with no de-embedding, as is demonstrated in Figure 162.

In this case however, it is possible to recover the classical half-wave rectified current waveforms that are characteristic of ideal simulations, by accounting for the effects of displacement current due to device output capacitance. Equation (30) represents a time-domain process where the device output voltage (v_c) excites an output capacitance (C) which in turn causes a displacement current (I_c) to flow and distort the devices 'normal' trans-conductive current.

$$I_c = \frac{dQ}{dt} \qquad I_c = C \cdot \frac{dv_c(t)}{dt} \qquad (30)$$

Employing an experimentally derived output capacitance of 4pF, it was possible to remove this effect, returning the distorted current waveforms of Figure 161 to the familiar half wave rectified waveforms shown in Figure 165.

For these measurements, second and third harmonic impedances have been passively tuned to near to 50 Ω. This has resulted in harmonic voltages being developed that combine with the fundamental voltage resulting in a waveform that tends to mirror the current waveform. Conditions are different in the Doherty measurement prototype however with even order harmonics terminated into low impedances by the harmonic trap, while odd harmonic components are naturally suppressed through choice of bias point [52].

The load-pull measurement system used is capable of synthesising a wide range of harmonic impedances at a calibrated reference plane, so presenting very low second and third harmonic impedances in order to mimic the impedances presented by the Doherty output structure is the obvious approach. Achieving this with packaged devices presents a specific challenge however as the effective calibrated reference plane needs to be

extended from the package-lead plane, through the package to the device plane itself. In other words, the effects of package parasitics as well as any associated delay need to be considered and de-embedded from measurement results before harmonic impedances can be accurately presented at the device plane. This is especially true for the harmonic components as the parasitic effects have an increasing effect with frequency.

In the absence of detailed package information or the necessary time required to conduct a thorough de-embedding process, one way of gaining an approximate idea of the fundamental voltage behaviour is to consider only the measured fundamental voltage component.

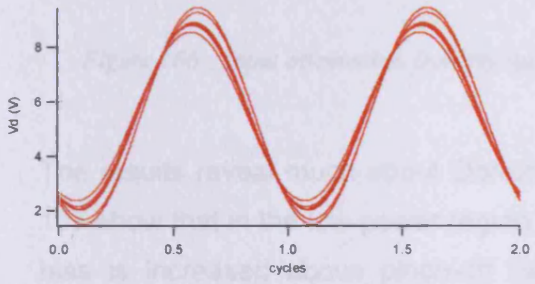


Figure 164 – Celeritek MESFET Vd (f1) (V)

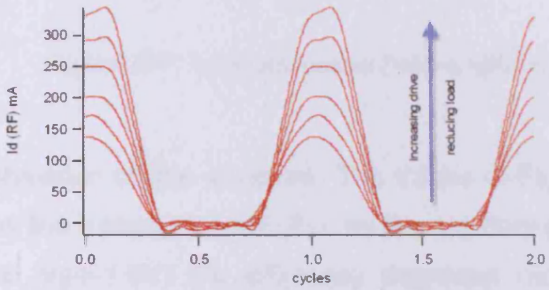


Figure 165 – Celeritek MESFET de-embedded Id(mA)

The measured fundamental voltage and output-capacitance corrected current waveforms are shown in Figure 164 and Figure 165. These align much more closely to ideal counterparts and give a good indication of what would actually happen at the device plane if the harmonic components were to be shorted. It is also assumed that shorting the harmonics will have little effect on the measured current waveforms due to spectral currents insensitivity to harmonic impedance.

6.1.3 Results

Detailed measurements of the GaAs MESFET Doherty structure discussed here are presented in chapter 4, where the structure is used as a vehicle to demonstrate the functionality of the single-tone Doherty measurement system. These measurements are extensive and include both input-attenuation and adaptive-bias Doherty realisations, as well as showing how it is possible to optimise the GaAs MESFET Doherty structure through dynamic adjustment of relative input phase and other parameters. The following measurement is not included in chapter 5 and is considered as an excellent way of demonstrating the presence of Doherty behaviour as well as highlighting some interesting design issues that exist. Specifically, this is the compromise between gain and efficiency in relation to the choice of *auxiliary* gate bias point for an IA-Doherty realisation.

Figure 166 and Figure 167 show the single-tone IA-Doherty gain and efficiency as a function of P_{in} and for different static values of *auxiliary* device gate bias, ranging between V_g=-2.2V and V_g=-1.25V.

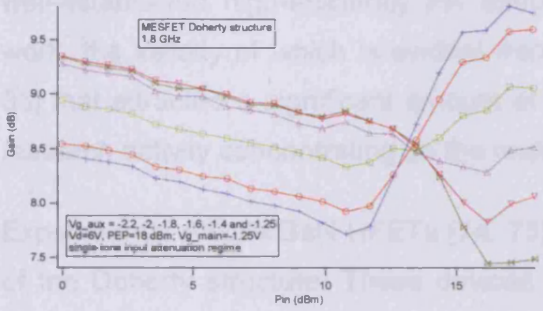


Figure 166 – input attenuation Doherty gain

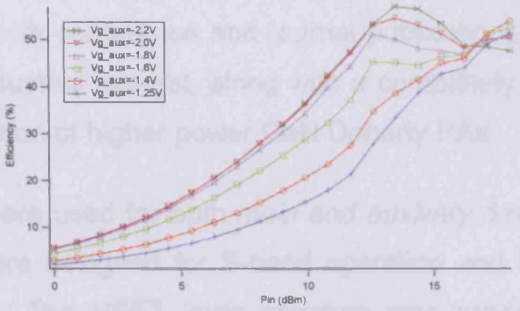


Figure 167 – input attenuation Doherty efficiency

The results reveal much about Doherty behaviour of this structure: The traces in Figure 167 show that in the low-power region below the transition point (P_T), as the *auxiliary* gate bias is increased above pinch-off (approx. Vg=-1.6V) the efficiency degrades rapidly loosing all signs of plateau behaviour, whilst the gain can be seen to increase uniformly. Turning attention to the high power region above the transition point, if the *auxiliary* device is biased too positively, significant overall gain expansion is observed alongside a poor efficiency profile. If the *auxiliary* bias is however too negative, a good efficiency plateau is observed, but this is in the presence of significant overall gain compression, indicating that the *main*-device load-line has expanded into the knee region. The real advantage of this measurement is that the optimum *auxiliary* bias condition is exposed. In this case it can be seen for instance that a choice of V_g=-1.8V results in a reasonably flat overall gain together with what is recognisable as an almost classical Doherty efficiency plateau.

6.2 GaN HFET Doherty

The realisation of a GaN Doherty PA structure was significant milestone as it involved the combination of a promising, potentially highly-efficient device technology with a relatively well-established high-efficiency PA structure. This represented an important phase of work, the validity of which is evident from both conference and journal publications [32, 33] that attracted a significant amount of industrial interest, along with a completely new research activity concentrating on the realisation of higher power GaN Doherty PAs.

Experimental AlGaN/GaN HFETs [74, 75] were used for both *main* and *auxiliary* devices of the Doherty structure. These devices were designed for S-band operation and have four 0.8µm long, 250µm wide NiAu gates. The HFET layer structure was grown by MOVPE and consisting of 30nm un-doped AlGaN (25%), a 1nm AlN layer to improve mobility and linearity [76] and silicon nitride passivation has been used to reduce the effects of current slump [28, 77] which is a documented problem with GaN transistor technology [29].

Two dies, each comprising five 1mm GaN devices were mounted into two Kyocera LCC-8 10-lead surface mount leadless packages. Two of the five devices within each package were bonded to the package leads in such a way as to allow either the connection of a single 1 mm device, or the parallel connection of two devices creating a larger 2mm device.

6.2.1 Design considerations

The GaN Doherty structure was designed using a similar approach to the proven GaAs MESFET experimental structure discussed earlier in this chapter, but with an impedance environment suited to devices with a R_{opt} of 50Ω. The strategy was to use an identical structure to implement two different power GaN Doherty realisations, using initially 1mm and then 2mm devices. As the impedance environment was fixed, the only way to achieve this whilst maintaining the optimum output impedance of 50Ω was to use two different drain bias voltage conditions of 17V to 34V for the 1mm and 2mm realisations respectively. This can be considered as a somewhat unorthodox approach, but is possible in the case of GaN technology devices due to the high breakdown voltages in comparison to other technologies. The maximum output power for the Doherty realisation using 2mm devices was expected to be more than four times that of the same structure using 1mm devices. This was based on the early assumption that the knee voltage would remain the same for both devices and both cases of drain bias. As will be seen, this was not to be the

case due to the now well documented GaN associated problems of knee-creep and current slump [28, 77].

The devices were mounted in the same chip carriers as used in the GaAs MESFET design and were soldered into the experimental Doherty structure, which is described in more detail in chapter 3.

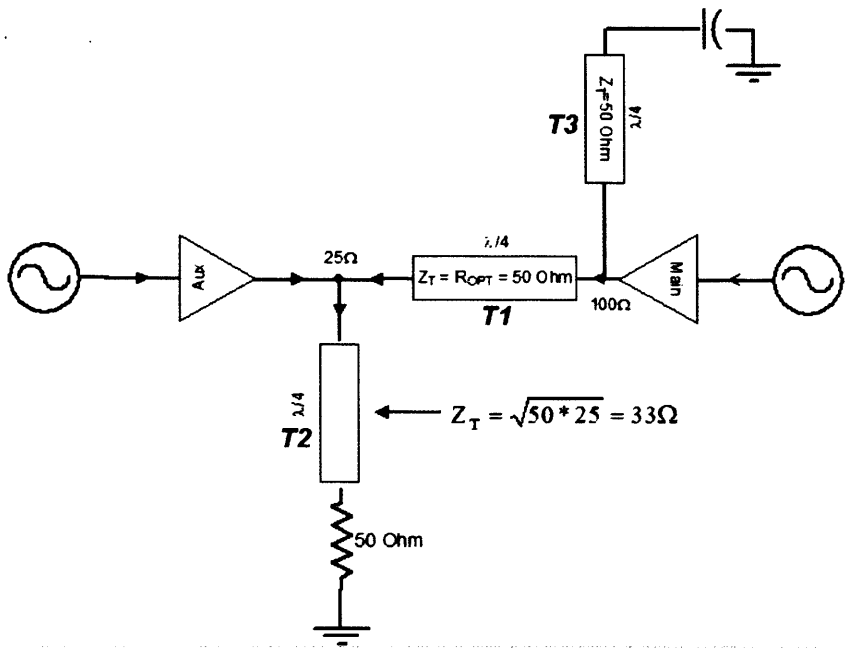


Figure 168 – Doherty structure and impedance environment

The experimental structure is represented in the Doherty schematic of Figure 168. The *main* and *auxiliary* devices are connected via the central λ/4 transformer (T1) possessing a characteristic impedance equal to R_{opt}, which in this case is 50Ω. According to classical Doherty theory, in the low-power region of operation an impedance of $R_{opt}/2$ or 25Ω must exist at the output of the *auxiliary* device, which will in turn be transformed to an impedance of $2R_{opt}$ at the output of the *main* device. In this case, the 25Ω is realised through the transformation of the 50Ω system load via a second λ/4 transformer (T2) possessing a characteristic impedance of 33.3Ω, as calculated using (31).

$$Zt = \sqrt{(Ropt/2)\cdot 50} \qquad (31)$$

6.2.1.1 DC measurements

Static and pulsed DC measurements were conducted on the 1mm GaN device using a *DIVA* 250 system [69, 70]. For the pulsed measurements, a gate pulse width of 1 μS and an interval of 5 ms were used, and the results are shown below in Figure 169 and Figure 170.

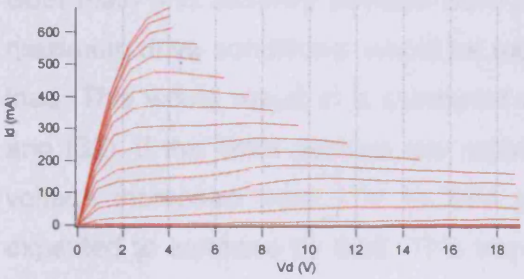


Figure 169 - 1mm GaN static DC-IV characteristic

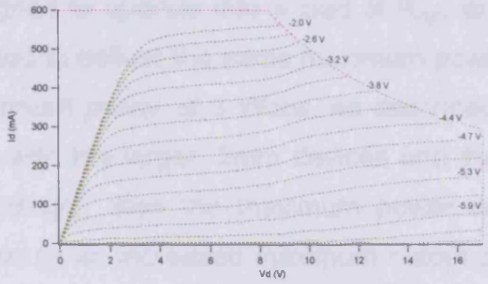


Figure 170 – 1mm GaN pulsed DC-IV characteristic

Both static and pulsed DC measurement results indicated a degree of non-ideal behaviour in the form reduced drain current 'kinks' for drain voltages below 10V, which are most likely attributable to charge related effects as no oscillations were observed. As was the case for the GaAs MESFET design, an initial model was extracted from the measured DC data by fitting a 10 coefficient polynomial function to an extracted Vg-Id transfer function. The polynomial coefficients were stored using the discrete MDIF file format [78], and made available as a model within in the ADS simulation environment using a Data Accesses Component (DAC) and a Symbolically Defined Devices (SDD) component [78].

The use of this relatively simple modelling approach was considered valid as it was assumed at this stage that device parasitics would be minimal. This is especially true in the case of GaN technology as the output capacitance is observed to be smaller than that observed for similar power GaAs MESFET devices. This assumption would be tested and later confirmed through load-pull measurements.

6.2.1.2 Initial design and simulation

From the measured DC-IV characteristics of a single 1mm device, pinch-off was observed to be at approximately Vg=-6V. A fundamental load-line was assumed for a drain voltage of 17V and maximum useful DC current (I_{max}) of 500 mA. This allowed a maximum fundamental power of $(V_{Pek} \cdot I_{Pek})/2$ where V_{peak} and I_{peak} are the peak fundamental RF voltage and current components respectively. For the initial design and in terms of DC conditions, it was assumed that $V_{pek} = (V_{dd} - V_k)$ and that $I_{pek} = (I_{max}/2)$. Assuming the DC measurement-

suggested knee voltage (V_k) of 5V, it could be deduced that the optimum impedance for the 1mm GaN devices for the given drain voltage was 50Ω, as described in (32).

$$Ropt = \left[\frac{(Vd - Vk)*2}{\text{Imax}}\right] = \left[\frac{(17-5)*2}{0.5}\right] = 48\Omega \approx 50\Omega \qquad (32)$$

Both *main* and *auxiliary* devices were designed to operate into a load of R_{opt}, and under maximum drive conditions, would be expected to deliver the same maximum power to the load. This would result in a combined maximum power of 3 Watts, as described in (15) and (33). If the 1mm devices are replaced with the larger, 2mm devices and the supply voltage increased from 17V to 34V accordingly, then the maximum power would be expected to increase by 6dB. This translates to an increased maximum output power of 12 Watts or 40.6 dBm.

$$P_{max} = 2 \cdot \left\{\left[\frac{(17-5)*(0.5)}{4}\right]\right\} = 3.0\ Watt\ (34.8\ \text{dBm}) \qquad (33)$$

It is important to note however that this initial design was based on DC measurements alone, and assumed no dispersion between DC and RF behaviour.

The design was aided by ADS simulations using a simple modelling approach and involved implementing an input attenuation Doherty approach employing two, identically sized and identically biased devices. Some of the simulation results are presented here.

One approach that was employed in bringing about Doherty behaviour within a simulation is to make use of the simulators optimisation capabilities to identify the required *auxiliary* device behaviour. More specifically, the optimiser is used to identify the *auxiliary* drive magnitude required to maintain a constant *main* device output voltage swing, such that the *main* device load-line is held close to, and prevented from interacting with the knee region. This optimisation was performed for both 1mm and 2mm designs over at least 6dB of dynamic range. Figure 171 and Figure 172 shows the identified, 'optimised' *auxiliary* device input voltages, *Vin (Aux),* that gives rise to almost constant *main* device output voltage magnitude, and can be seen to be an almost linear functions of the *main* input voltage *Vin (main).*

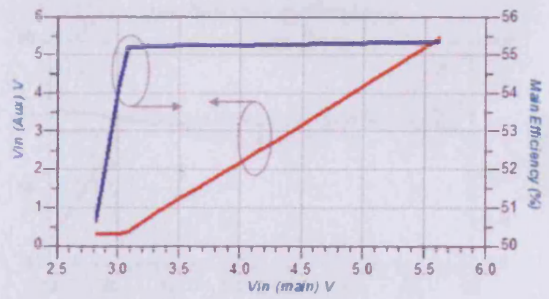


Figure 171 – 1mm main device Vd and auxiliary I/P drive

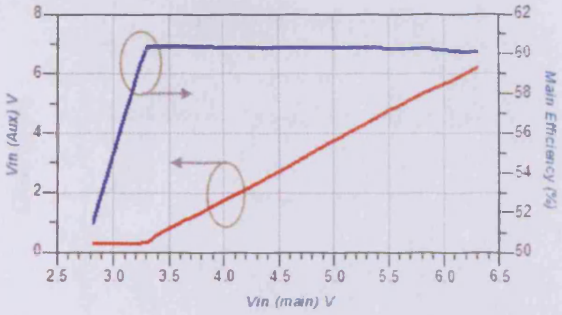


Figure 172 – 2mm main device Vd and Auxiliary I/P drive

This near ideal *main* device behaviour is as a result of the almost ideal *auxiliary* and *main* device load-line behaviour shown in Figure 173 through Figure 176.

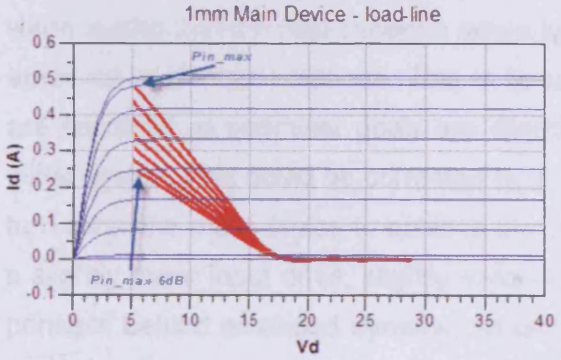


Figure 173 – 1mm device main load-line

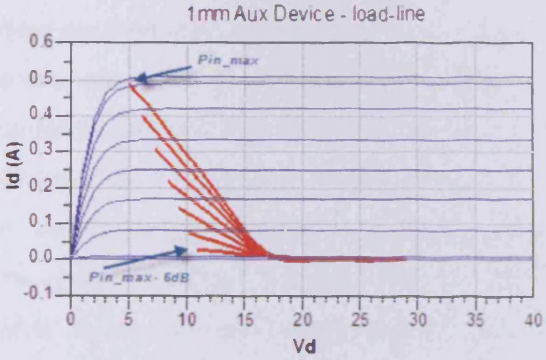


Figure 174 – 1mm device auxiliary load-line

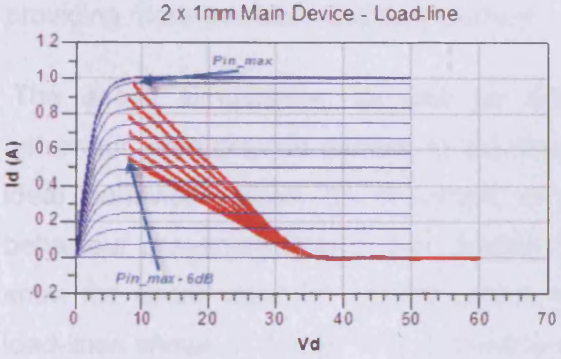


Figure 175 – 2mm device main load-line

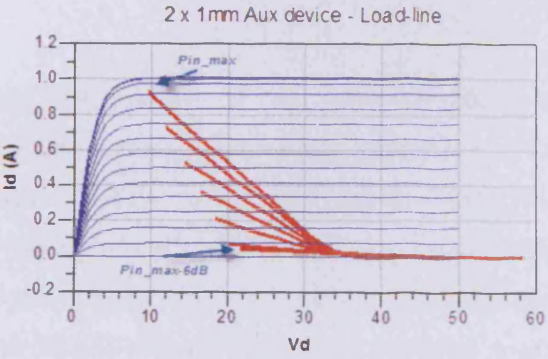


Figure 176 – 2mm device auxiliary load-line

The near ideal Doherty load-lines show how the *main* device voltage swing is being maintained close to, but not too close to the device's knee-region. This translates perhaps unsurprisingly into near ideal Doherty performance, which is evident from the efficiency plateau and nearly constant gain over the entire dynamic range shown in Figure 177 and Figure 178.

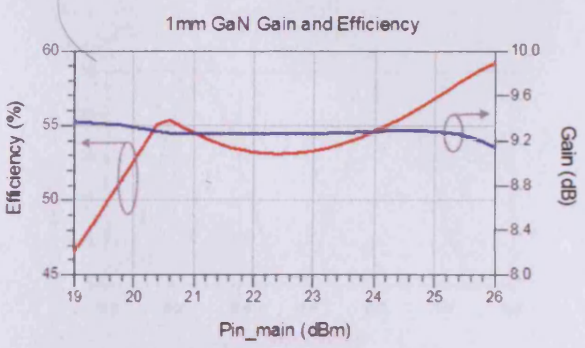


Figure 177 – 1mm device Gain and Efficiency

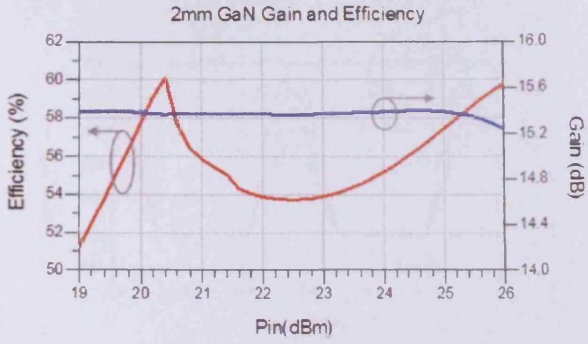


Figure 178 – 2mm device P_{in}-P_{out} characteristics

It is worth noting that the gain of the Doherty employing the larger, 2mm devices is 6dB more than the same structure employing the 1mm devices. This is as predicted and simply because the available device current and available voltage have doubled. It is also worth noting that the 6dB dynamic range specified by classical Doherty theory is not quite achieved in the optimisations. This is because the *main* device voltage magnitudes that are specified as optimiser goals are slightly conservative and less than that used in the initial design. This could be corrected by a small increase in the value of R_{opt} and would in turn allow the *main* device to achieve maximum voltage swing and maximum efficiency at a slightly lower input drive, slightly extending the dynamic range. This is in fact the basic principle behind extended dynamic range Doherty structures, as is described in detail in [9], where it is shown how the dynamic range can be easily extended from the classical 6dB by adjusting the characteristic impedance of the *main* inverting transformer and providing more available *auxiliary* current.

The above simulations, as well as allowing observation of the dynamic load-line behaviour, also provide access to the time domain current and voltage waveforms. The ideal behaviour gives an important reference against which the actual measured behaviour presented later in this chapter can be compared. Figure 179 and Figure 180 show the nearly ideal RF voltage and current waveforms that are used to construct the load-lines shown in Figure 173, and are another way of observing the near constant *main* voltage swing together with a linearly increasing current magnitude.

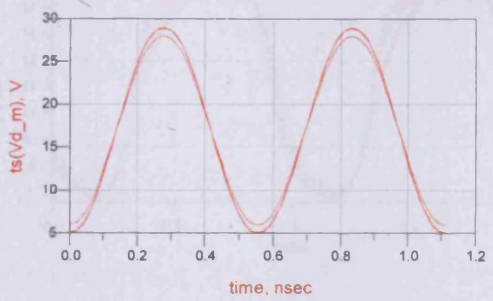


Figure 179 – simulated 1mm main-device O/P voltage waveforms over 6dB dynamic range

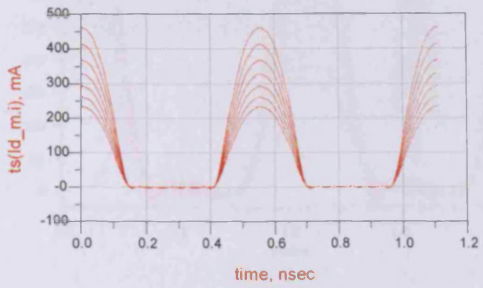


Figure 180 – simulated 1mm main-device O/P current waveforms over 6dB dynamic range

Figure 181 and Figure 182 show the resulting, simulated output power for both 1mm and 2mm Doherty realisations and confirm that the expected maximum output power is both linear, and agrees with the previously calculated values of 3 and 12 Watts.

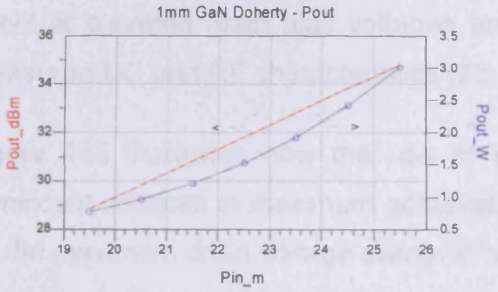


Figure 181 – 1mm device P_{in}-P_{out} characteristics

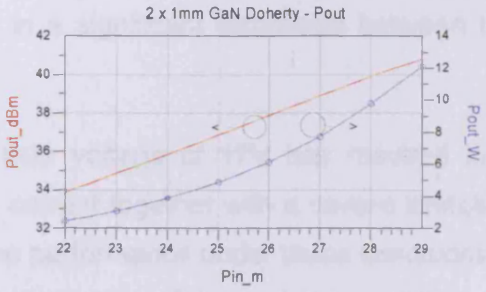


Figure 182 – 2mm device P_{in}-P_{out} characteristics

6.2.2 *Initial load-pull measurements at Vd = 17V*

As was the case for the GaAs MESFET, a time-domain load-pull measurement system was used to sweep a real, fundamental load presented to a single 1mm GaN HFET device biased in class-B (Vg=-6V), over at least 6dB of dynamic range. The required impedance was determined experimentally, such that a constant maximum output voltage swing was maintained close to the knee-region, in much the same way as the simulated optimisation approach discussed in the previous section. The resulting current and voltage waveforms are shown in Figure 183, which at first glance compare quite well to simulated results, and look similar in profile to those observed for the GaAs MESFET device.

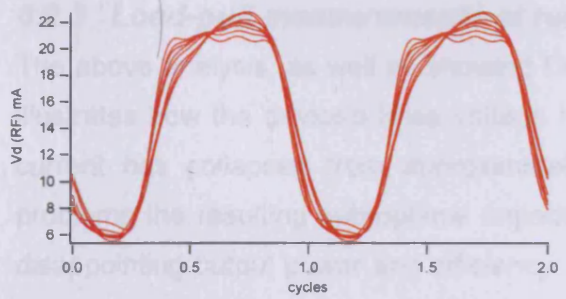


Figure 183 – 1mm Qinetiq GaN drain voltage at Vd=17V

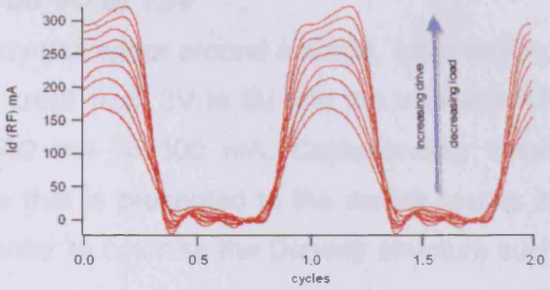


Figure 184 – 1mm Qinetiq GaN drain current at Vd=17V

Although the voltage magnitude remains relatively constant and the magnitude of the half-wave rectified current waveform increase as expected with increasing input drive, on closer inspection there is some current compression evident at higher drive levels, and the maximum magnitude of both voltage and current are lower than expected. This is more noticeable when the waveforms are viewed as dynamic load-lines, where the GaN related effects of *knee-creep* and *current-slump* become clear. These problems have a significant effect at elevated drain bias voltages and result in a significant dispersion between the measured DC and RF characteristics [28, 77].

Figure 185 illustrates how the use of a drain bias voltage of 17V has resulted in a significant collapse in maximum achievable drain current together with a severe limitation on the maximum drain voltage swing. When device performance under these conditions is considered, Figure 186 reveals a plateau of relatively low efficiency between 30% and 40% over 8 dB of dynamic range together with a maximum output power of 28 dBm, which is almost 3dB lower than simulations and initial designs suggested was possible.

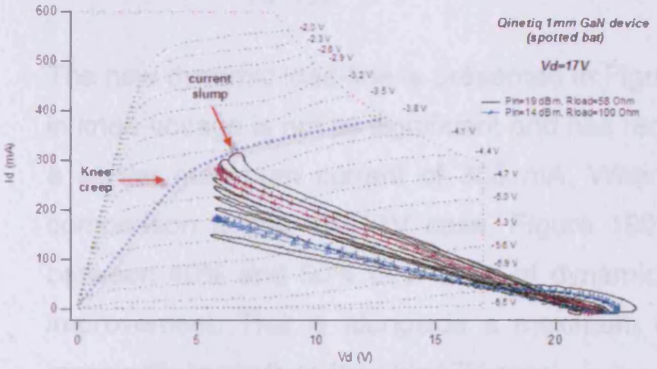


Figure 185 – GaN HFET measured dynamic load-lines for Vd=17V, with overlaid pulsed DCIV data

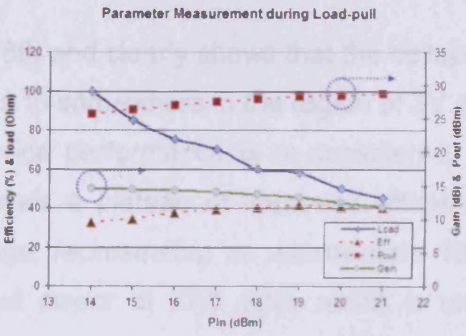


Figure 186 – Qinetiq GaN measured performance for Vd=17V

6.2.3 Load-pull measurements at reduced Vd of 12V

The above analysis, as well as showing Doherty behaviour around a single, *main* device, illustrates how the device's knee voltage has 'crept' from 3V to 6V and the available RF current has collapsed from approximately 500 mA to 300 mA. Compounding these problems the resulting sub-optimal impedance that is presented to the device results in disappointing output power and efficiency. In order to optimise the Doherty structure such that the effects of knee voltage 'walk-out' are reduced, further large-signal measurements were conducted and an optimum drain voltage of Vd=12V was identified that allowed for a maximum 'slumped' current of 350mA and the reduced knee voltage of 3V. Using this approach, the value of R_{opt} was conveniently maintained at 50Ω, allowing the same structure to be used.

The re-measured current and voltage waveforms are shown in Figure 187 and Figure 188, and show current waveform behaviour that relatively unchanged in comparison to the Vd=17V case, and a voltage swing that is somewhat reduced .

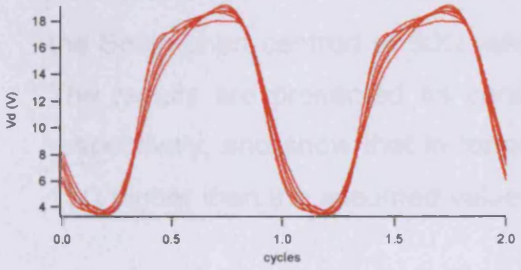


Figure 187 – 1mm Qinetiq GaN drain voltage at Vd=12V

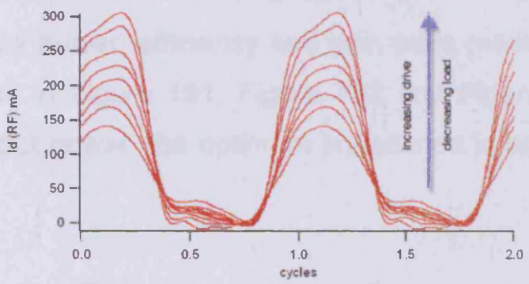


Figure 188 – 1mm Qinetiq GaN drain current at Vd=12V

The new dynamic load-line is presented in Figure 189, and clearly shows that the collapse in knee-voltage is not as significant and has receded to somewhere in the region of 3V, for a similar maximum current of 300 mA. When device performance is re-considered, In comparison to the Vd=17V case, Figure 190 reveals a plateau of improved efficiency between 40% and 50% over 8 dB of dynamic range, representing an approximate 10% improvement. This is alongside a maximum output power of 27.5 dBm, which is only marginally lower than the Vd=17V case.

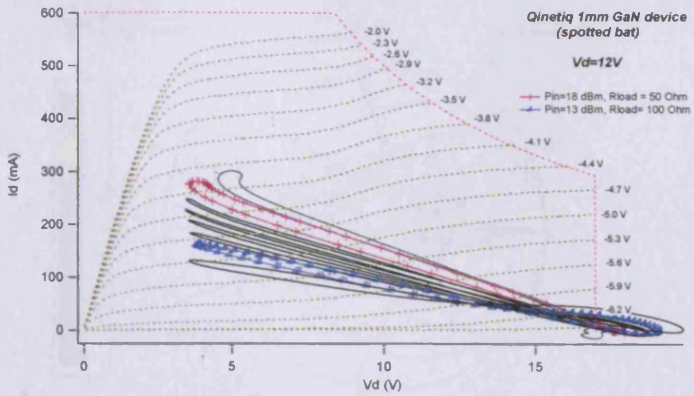


Figure 189 – GaN HFET measured dynamic load-lines for Vd=12V, with overlaid pulsed DCIV data

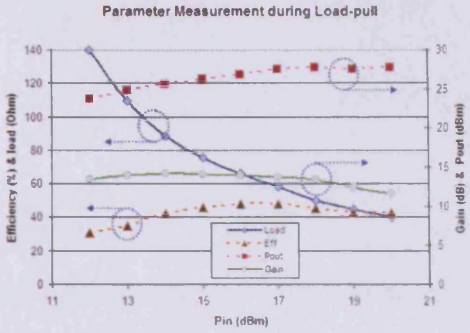


Figure 190 – Qinetiq GaN measured performance for Vd=12V

6.2.3.1 Contour Plots

In order to test the assumptions made regarding the optimum device impedance, output power, etc, a measurement was conducted where the device was biased in class-B, the drain voltage set at 12V, and the available input power fixed at a point that caused 1dB compression into a load of 50Ω. The fundamental load was then varied over a region of the Smith chart centred at 50Ω, whilst output power, efficiency and gain were measured. The results are presented as contour plots in Figure 191, Figure 192 and Figure 193 respectively, and show that in terms of output power, the optimum impedance is actually 15Ω higher than the assumed value at 65Ω.

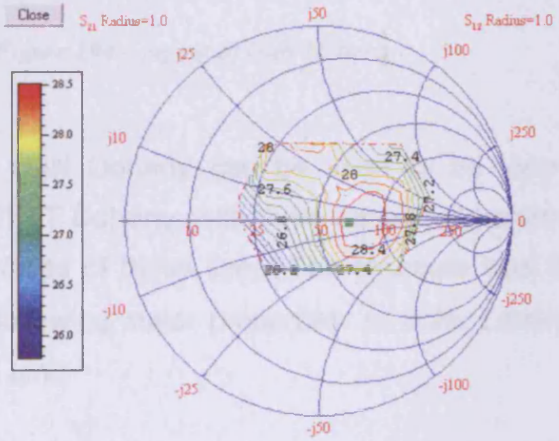


Figure 191 –GaN HFET P_{out} contours at 1dB compression point (Vg:-6.00V, Vd:12V)
Load=(-0.16,-0.01), P_{out}=28.5 dBm, Efficiency=52.1%

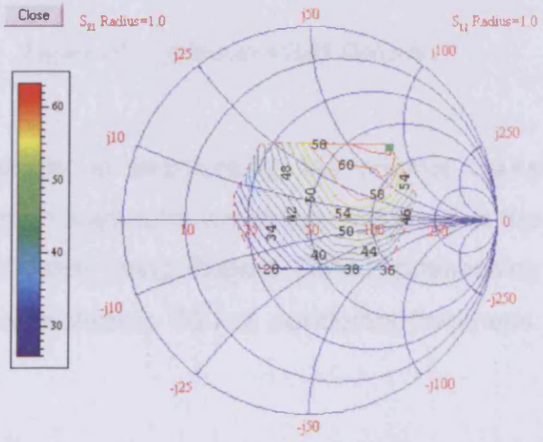


Figure 192 – MESFET Efficiency contours at 1dB compression point (Vg:-6.00V, Vd:12V)
Load=(0.42,0.38), P_{out}=27.1 dBm, Efficiency=63.2%

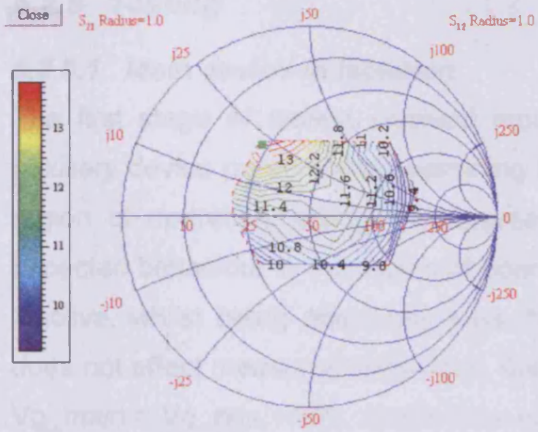


Figure 193 –MESFET Gain contours at 1dB compression point (Vg:-6.00V, Vd:12V)
Load=(-0.25,0.37), P_{out}=28 dBm, Efficiency=42.7%

6.2.4 Fabrication

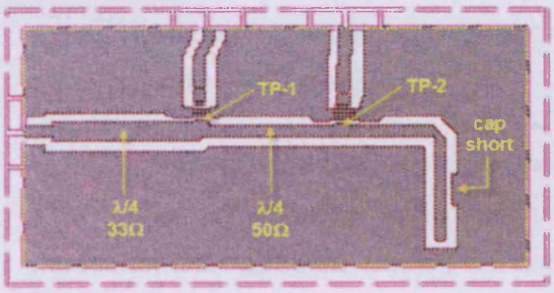


Figure 194 – layout of GaN Doherty

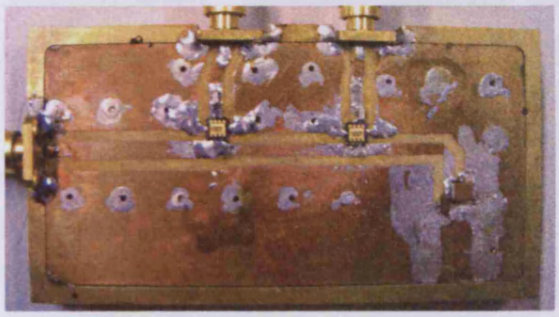


Figure 195 – fabricated GaN Doherty

The GaN Doherty can be seen to be very similar in structure to the original GaAs MESFET Doherty, with three series λ/4 transmission lines and two devices situated at the interfaces of these lines. The structure was fabricated using Rogers TMM3, possessing the following major properties: ε_r: 3.25, Laminate thickness: 30 mil, conductor thickness: 17.5 μm,

As the GaN devices were in very short supply, the intention was to conduct as much of the initial testing and tuning as possible passively and in advance of mounting the devices themselves. This involved tuning, and the inclusion of low frequency decoupling capacitors that would be necessary for planned modulated measurements. This approach is in contrast to the GaAs Doherty design where it was found convenient to perform most of the tuning with the devices in place. Tuning is discussed in detail in Chapter 3.

6.2.5 Testing

6.2.5.1 Main device in isolation

The first stage of testing involved mounting the *main*-device in isolation, i.e. with no *auxiliary* device present and examining the Doherty structure behaviour in the low-power region of operation. Using this approach, it was possible to compare measured and expected behaviour in the region of operation, where the *auxiliary* device is intended to be inactive, whilst being absolutely sure that the physical presence of the *auxiliary* device does not affect measured behaviour. Biasing the device at a drain voltage of 17V and with Vg_*main* = Vg_aux = -6V, single-tone excitation was then applied to the *main* device and the input power swept over a dynamic range between 0dBm and 25dBm. The first observation from the measured results was that there was an obvious and gradual collapse in gain, well before the point of compression predicted by DC characterisation. It was also observed that although the gain profile could be modified by adjusting the gate bias, the premature compression could not be avoided. Under such conditions, it was difficult to select an optimum gate bias condition. However, following some experimentation, Vg=-6.5V was chosen as the bias point to offer the optimum in terms of efficiency and gain flatness.

6.2.5.2 Main device with auxiliary device present and biased-off

The *auxiliary* device was then inserted into the structure, biased off at Vg=-9V, and the measurements repeated, in order to confirm the physical presence of the inactive *auxiliary* device had no significant effect on the previously measure results.

It is worth stressing the importance of this stage of testing as it was known that any significant device output capacitance could have a profound effect on the device's off-state output impedance, and for this Doherty structure with its devices mounted directly on the combining transformer, this would have a disastrous effect on the overall performance. This problem stems from the inability to effectively 'disable' devices such that they present high RF impedance in their non-conductive state. When designing Doherty's using devices with high output capacitance, specific measures must be taken such that low off-state output impedances at the output of the *auxiliary* device are transformed to much high impedances using techniques such as those proposed in [42, 60, 79].

Figure 196 and Figure 197 show the behaviour of the *main* device whilst the *auxiliary* device is biased hard-off at -9V, and the *main* device gate bias is swept between -6V and -6.8V, whilst the drain voltage was maintained at 17V.

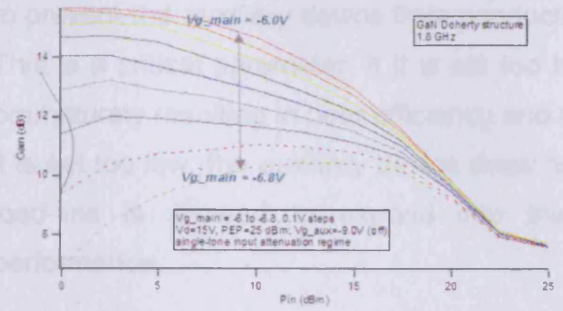


Figure 196 – main device in isolation (gain)

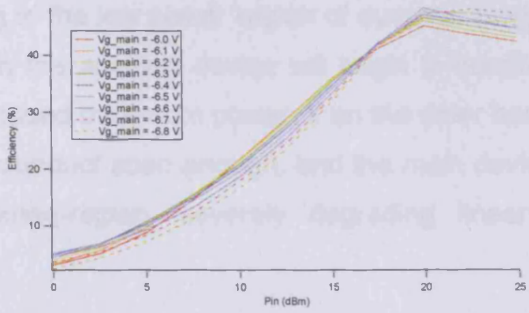


Figure 197 – main device in isolation (Efficiency)

The graphs show that although variations in gate bias have a significant effect on gain, especially at lower drive levels, the impact on efficiency is relatively small. What is also worth noting is the low maximum drain efficiency achieved for a device technology that promises high linear efficiency.

6.2.5.3 Improving performance by reducing the drain voltage

Although somewhat disappointing, some performance degradation was anticipated due to the known effects of the current-slump and knee voltage walk-out problems associated with these devices, as discussed in 6.2.2. In an attempt to reduce these effects and improve performance, the same measurement was conducted using a lower drain voltage of 10V, the results of which are shown in Figure 198 and Figure 199, where it can be seen that the efficiency has improved.

From these improved results, it was possible to select the maximum Doherty drive power (P_{PEP}) and the transition point drive power (P_T) corresponding to 23 dBm and 17 dBm respectively.

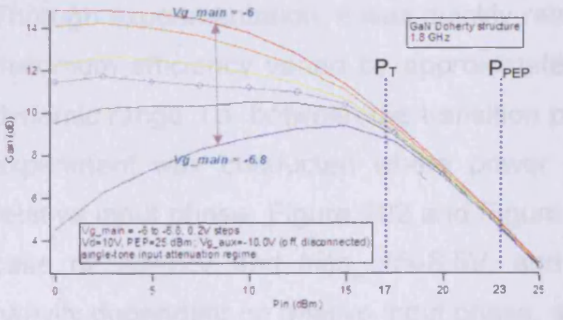


Figure 198 – main device in isolation (gain)

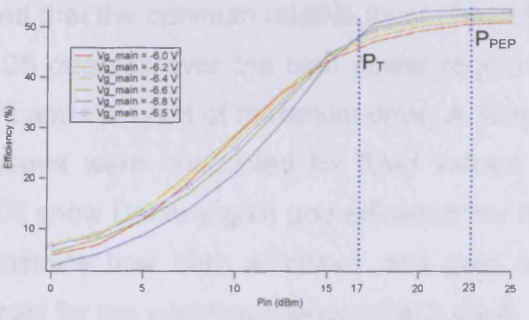


Figure 199 – main device in isolation (Efficiency)

6.2.5.4 Testing for Doherty behaviour using the adaptive-bias approach

An adaptive-bias Doherty approach was used to test the structure. Figure 200 and Figure 201 show the GaN Doherty gain and efficiency for power sweeps where *bias_off* is varied between -8V and -9.5V. The parameter '*bias_off*' is the fixed gate-bias voltage that is used

to prevent the *auxiliary* device from conducting in the low power region of dynamic range. This is a critical parameter: if it is set too high the *auxiliary* device will begin to conduct prematurely resulting in poor efficiency and reduced maximum power. If on the other hand it is set too low, the *auxiliary* device does not conduct soon enough, and the *main* device load-line is allowed to expand into the knee-region, severely degrading linearity performance.

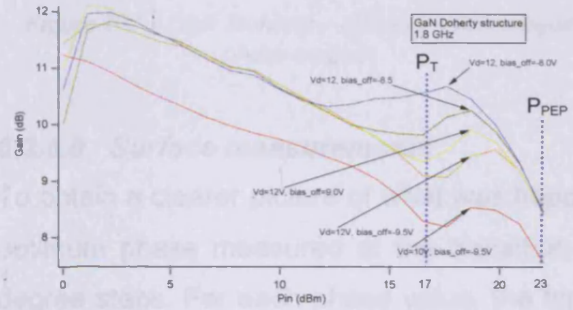


Figure 200 – GaN Doherty – effect of value of bias-off on gain

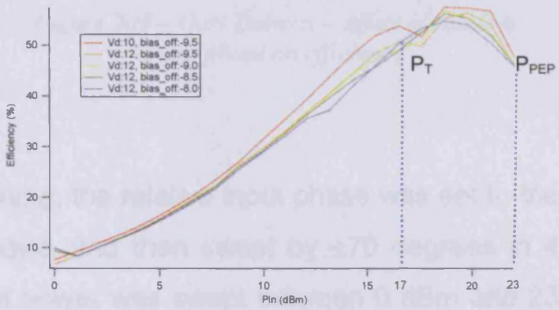


Figure 201 – GaN Doherty – effect of value of bias-off on efficiency

A good compromise between *main* device compression and *auxiliary* turn-on can be achieved by setting *bias_off* to -8.5V. It must be noted however that the rapid decrease in both gain and efficiency at the high-power end of the sweep is not completely due to normal device compression, but instead a consequence of bias dependent gain-phase, which, as was the case for the GaAs devices in the previous section, is significant. This effect can be appreciated when viewing the efficiency as a function of both P_{in} and relative input phase, as shown in the following section and presented as a surface in Figure 204.

6.2.5.5 *Effect of bias dependent gain-phase*

Through experimentation, it was quickly realised that the optimum relative input phase for maximum efficiency varied by approximately 25 degrees over the high power region of dynamic range, i.e. between the transition point and the point of maximum drive. A simple experiment was conducted where power sweeps were conducted for fixed values of relative input phase. Figure 202 and Figure 203 show Doherty gain and efficiency for the case of Vd=12V and *bias_off*=-8.5V, and illustrate how both efficiency and gain are heavily dependent on relative input phase, at least for the adaptive-bias approach used.

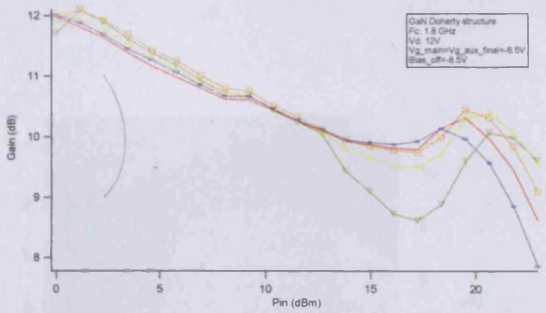


Figure 202 – GaN Doherty – effect of relative input phase on gain

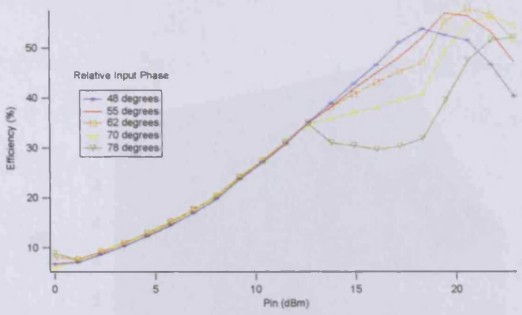


Figure 203 – GaN Doherty – effect of relative input phase on efficiency

6.2.5.6 Surface measurements

To obtain a clearer picture of what was happening, the relative input phase was set to the optimum phase measured at the transition point, and then swept by ±70 degrees in 4 degree steps. For each phase value, the input power was swept between 0 dBm and 23 dBm. The *main* device gate bias was set to equal the final value of the *auxiliary* device gate bias at -6.5V, whilst the drain voltage was set to 10V. Using a carrier frequency of 1.8GHz and a value of *bias_off* = -8.5V, the adaptive-bias gain and efficiency were measured and are shown in Figure 204 to Figure 207.

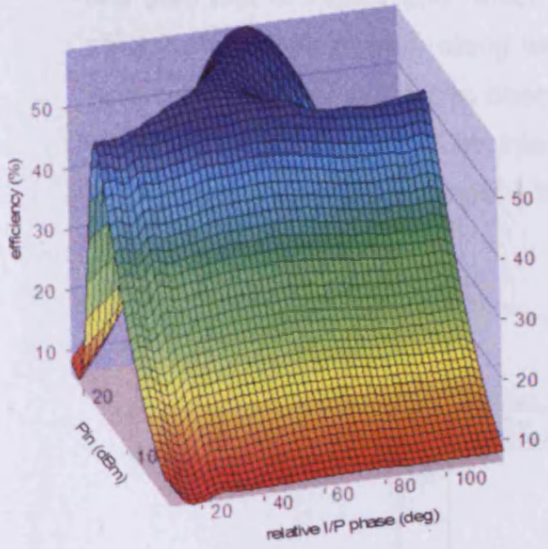


Figure 204 – efficiency from above

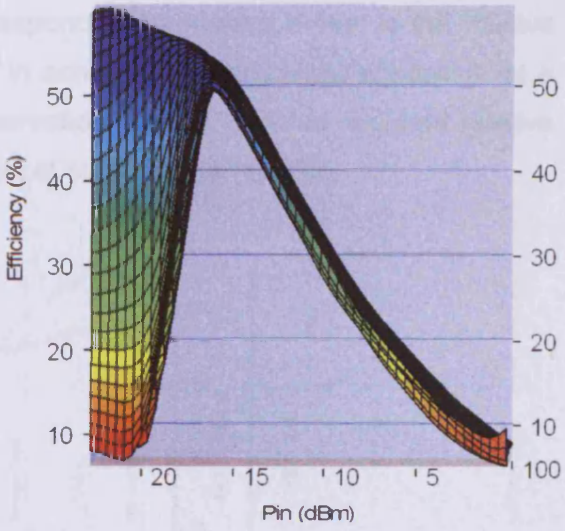


Figure 205 – efficiency from side

The first two plots show the measured drain efficiency viewed from two different perspectives. Whereas Figure 204 clearly shows the bias dependent gain-phase behaviour, Figure 205 clearly shows the existence of the efficiency plateau.

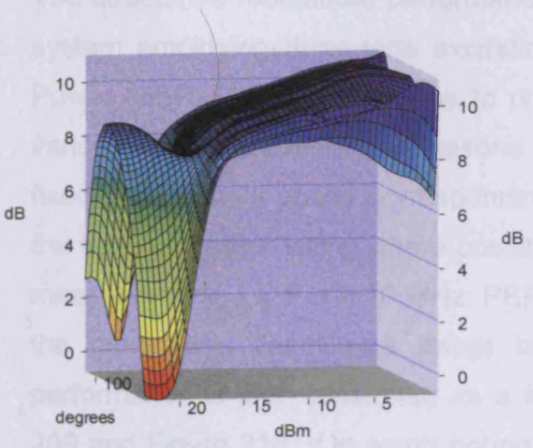


Figure 206 – gain surface from side

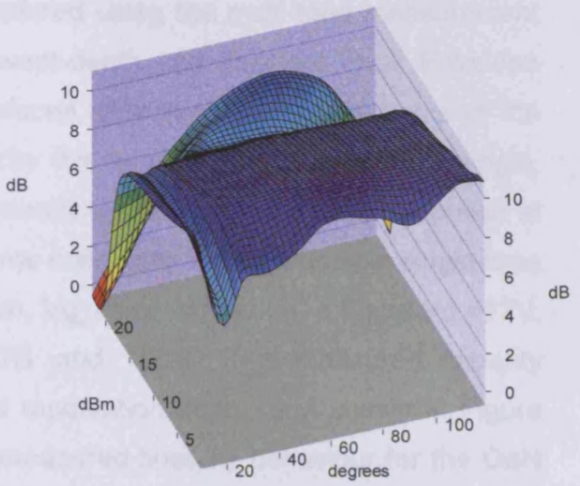


Figure 207 – gain surface from above

Of course, when interpreting Doherty results, it is important to consider gain as well as efficiency. Figure 206 and Figure 207 present the corresponding gain surfaces, which although non-optimal due to the devices used, show that the efficiency plateau exists in the presence of non-compressive gain. These results are summarised in the efficiency and gain plot of Figure 208, which identifies the maximum measured efficiency at each point in the power sweep, along with the corresponding gain. Also shown is the relative input phase profile, which has been employed in achieving the optimised efficiency, as a function of output power. The interesting observation here is that the required relative input phase in degrees is almost a linear function of output power in dBm.

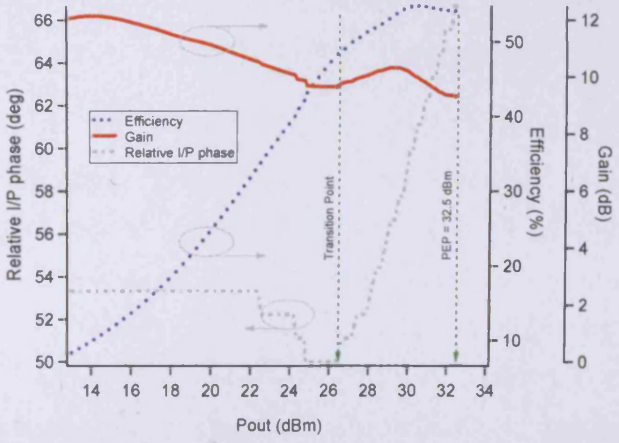


Figure 208 – single-tone gain and efficiency and relative input phase

6.2.5.7 *Modulated behaviour*

The structure's modulated performance was explored using the multi-tone measurement system employing three-tone excitation with swept-depth and constant Peak Envelope Power (PEP). Although possible to present surfaces describing linearity in terms of the various mixing products, for reasons of simplicity this is achieved here using a single, fixed relative input phase corresponding to the measured optimum relative input phase at the transition point. Using where possible the same conditions to those used in single-tone measurements, i.e. Fm = 10 MHz, PEP = 23 dBm, Vg_*main*=Vg_aux = -6.5 and Vd =12V, the modulation depth was swept between 0% and 100%. The measured linearity performance is then presented as a function of modulation depth, and shown in Figure 209 and Figure 210. It is worth noting that the measured linearity behaviour for the GaN Doherty structure is very similar to that of the GaAs Doherty structure, and both agree well with the simulated predictions presented in chapter 5.

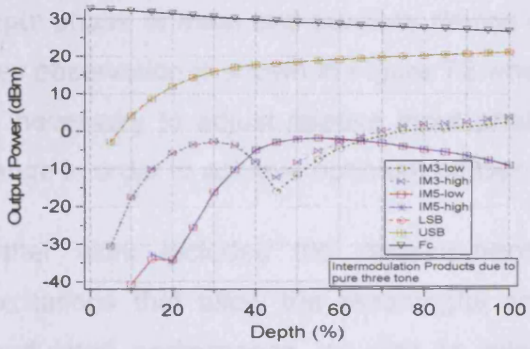


Figure 209 – 3-tone linearity performance (I-P atten)

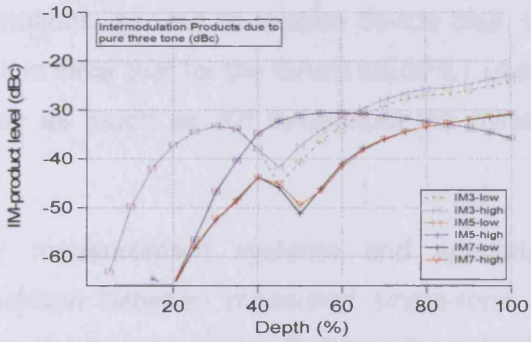


Figure 210 – 3-tone linearity (dBc) performance (I-P atten)

Chapter 7 Conclusions

Although the Doherty is renowned for its elegant simplicity, its realisation using modern microwave devices is problematical, far from simple and reveals many hidden complexities which are brought about by the complex harmonic interaction between two active devices, and conspire to cause a variety of performance related problems.

This thesis considers both fundamental and harmonic behaviour of the Doherty PA and concentrates initially on identifying the various design trade-offs that exist between linearity and efficiency. Using extensive single-tone and modulated analysis, a novel measurement approach has been developed that involves replacing the classical Doherty's symmetrical input power division arrangement with independent, phase-coherent excitation. Using this approach, a number of optimisation approaches have been identified that involve the dynamic adjustment of relative input magnitude and relative input phase of main and auxiliary device excitations, as well as relative device bias. One key observation is shown in Figure 72 where it is clear that for the GAaS MESFET used, it is necessary to adjust relative input phase by as much as 30° throughout the dynamic range in order to achieve optimum efficiency.

Other work includes the development of measurement systems and specialised excitations that allow the meaningful comparison between measured single-tone and modulated performance, as well as allowing investigations into Doherty linearity. The extensive use of harmonic load-pull measurement systems and the direct synthesis of the impedance environments that exist within the Doherty have allowed a number of device technologies to be considered. This has resulted in the realisation of GaAs and GaN Doherty prototypes which have been extensively characterised and form the basis of a number of significant publications.

Following an introduction which places the research activity into context, ***Chapter 2*** introduces some essential theory of the Doherty PA, as well as additional detail that is relevant to this thesis and not general available in published literature. It is considered constructive for instance to evaluate Doherty operation, not only in terms of transformed impedances, but also in terms of terminal voltages and currents that are present at the Doherty's *main* and *auxiliary* device outputs, and specifically how these map onto the I-V plane of a device. This discussion is extended to characterising device behaviour whilst exposed to Doherty impedance environment. This novel emulation approach involves employing fundamental load manipulation to maintain a constant device output voltage,

over a wide dynamic range. Even when working with relatively ideal device models, this analysis leads to key observations including the drive related non-constant device gain seen in Figure 20, and behaviour that has significant consequences in terms of Doherty design. It is clear from Figure 19 for example that even using a device with small parasitic properties and low output capacitance, the dynamic range of the Doherty will be limited to due to the constant output voltage leading to significant displacement current relative to the fundamental output current. This analysis was valuable and formed the basis of the harmonic load-pull measurements conducted towards the end of the research and described in Chapter 6, where real devices from different device technology families are characterised within synthesised Doherty environments. Classical, input-attenuation and adaptive-bias Doherty implementations are discussed in some detail, together with the importance of harmonic generation and termination within the Doherty PA

The Doherty PA is without doubt an elegant and simple structure; however, its successful realisation using modern microwave devices tends to be problematical. ***Chapter 3*** considers this problem, which is in essence due to a number of subtle complexities that exist at both fundamental and harmonic levels, and that are in general brought about by the complex interaction between the two active devices, and their passive environments. Whereas observing device behaviour within static, well-behaved impedance environments is relatively straight forward, achieving the same visibility within the highly complex and dynamic impedance environments within the Doherty structure is, in comparison extremely difficult. This problem is further aggravated by the fact that that in some Doherty realisations considered, both the bias and excitation delivered to the *main* and *auxiliary* devices will be dynamic functions of the applied drive magnitude [31, 42, 43].

Two Doherty characterisation approaches have been considered. The *harmonic* approach involves using harmonic load-pull measurement systems to develop understanding of Doherty behaviour through the synthesis and presentation of 'Doherty' harmonic impedance environments to a single device. Although considered to be the 'ideal' approach, it was also deemed high risk and was at the time, considered not to be the best or most appropriate option.

The alternative *fundamental* characterisation approach that was ultimately adopted involved developing specific Doherty measurement structures and biasing arrangements that were effective in suppressing harmonic generation, thus allowing research to focus upon fundamental Doherty behaviour and optimisation without the added complexity of harmonic interaction. Two Doherty measurement structures are discussed that have been designed for devices with optimum impedances of 25Ω and 50Ω, for GaAs and GaN

Doherty realisations respectively. These structures contain all of the necessary elements to support Doherty behaviour, such as output impedance transformation networks, harmonic suppression mechanisms, stabilisation mechanisms, bias circuits, etc, and are in effect complete, functional Doherty amplifiers. The tuning of these structures ensures that even order harmonics are suppressed, which is critical to the success of this approach.

Chapter 4 considers the evolution of the measurement systems developed for Doherty characterisation. This includes the synthesis of *main* and *auxiliary* excitation signals, provision of the required bias environment, the measurement of the resulting power spectrum and the implementation of a suitable software environment to support calibration, measurement control and data presentation. Through the use of independent, phase-coherent microwave signal generators, a measurement system was developed that allowed the automated, systematic perturbation of relative input phase, relative input magnitude and relative bias profile, together with the ability to measure the effects of these perturbations in terms of key performance parameters. Although measured single-tone results are conclusive in demonstrating the presence of Doherty behaviour in the realisations that have been considered, they are also indicative of the hidden complexities that exist within the simple Doherty structure. Investigation into these complexities has led to a number of optimisation possibilities involving the dynamic variation of relative input phase, relative input magnitude and bias profile. From early analysis and Figure 81 through to Figure 98, it is clear however that improving one parameter generally leads to degradation of others.

The most effective way of presenting the resulting large amounts of measurement data was found to be graphically, through the use of 3-dimensional surface plots, through which it was clear for example that gain and efficiency of the GaAs MESFET structure were very much functions of relative input phase. In summary, the simple Doherty structure is far more complex than simple theory suggests is the case.

One key assumption made during single tone analysis was that optimising the Doherty structure for constant gain and constant gain-phase would lead to improvements in overall linearity. This theory was untested however and it was essential to be able to measure Doherty performance under modulated excitation. In ***Chapter 5***, it is discussed how the conventional linearity measurement approaches were found to be problematical when applied to the Doherty measurement prototypes, and how a new three-tone characterisation approach was developed that allowed excitation of specific areas of the

Doherty's output characteristic, and produced results that were comparable to single-tone equivalents.

The need to perform modulated measurements on the Doherty structure introduced significant measurement hardware and software related problems however. The most significant of these was the synthesis of independent, modulated *main* and *auxiliary* RF input excitations, the control of their relative phase and magnitudes, along with *main* and *auxiliary* bias voltages. A base-band modulation approach was eventually adopted that involved direct manipulation of I and Q modulation component signals, and provided the required dynamic adjustments in both relative magnitude and phase of the input stimuli. Additional functionality was added in the form of an IF load-pull and measurement capability that was effective in allowing the presentation of specific impedances to the significant IF component. This functionality would be needed to allow investigations into the assertion that the Doherty structure was especially sensitive to variations in base-band impedance.

The overall aim of this phase of work was to establish a foundation on which a detailed analysis and characterisation of measured Doherty linearity could be based. Some theoretical and model-based analysis work has been conducted however and is presented, together with some modulated measurements, in order to validate both the functionality of the measurement system and the analysis approach taken.

It was important to consider the suitability of different device technologies for use within Doherty PA structures for base-station applications. ***Chapter 6*** addresses this issue and concludes that although LDMOS is currently the device technology of choice, there is some serious debate over how long this will continue to be the case, and raises a pointed question: can LDMOS, as an incremental technology can continue to evolve rapidly enough to continue to meet the frequency, power, linearity and efficiency needs of modern mobile communication systems, in the presence of increasingly competitive alternative technologies and more challenging applications?

GaAs and GaN are two such alternative, evolving device technologies that are considered through their use as the active devices technologies within two, specially designed Doherty measurement prototypes. These structures, in combination with specific biasing arrangements are effective in suppressing harmonic generation and allowing fundamental Doherty behaviour to be explored and characterised.

Harmonic load-pull and waveform measurement techniques have been extensively employed, and are introduced as a valuable and novel means of characterising devices

whilst operating in realistic, operational conditions, achieved through the 'emulation' of dynamic excitation and impedance environments that are known to exist with Doherty architectures. This approach, when applied to the design of the GaN Doherty revealed some significant problems associated with the GaN device technology related problems of current-slump and knee-creep. The use of waveform measurement in the design also presented a solution to this problem allowing performance to be quickly re-evaluated at reduced drain voltage.

Chapter 8 Future Work

8.1 General

At the start of the research activity, two possible Doherty characterisation approaches were identified that involved considering behaviour from both *fundamental* and *harmonic* perspectives. This thesis has dealt primarily with the fundamental analysis of Doherty, identifying a number of issues and problems that needed to be addressed, along with a number of optimisation approaches that now need to be developed further. Modulated Doherty behaviour has been considered and measured, and has resulted in the realisation of a modulated measurement system and an approach that puts in place the foundations that are necessary for a more complete, measurement-based linearity characterisation to be undertaken. This needs to include investigation of the possibility that the Doherty is more sensitive to base-band impedance than other, conventional PAs, which is made possible by the inclusion of an IF load-pull capability in the measurement system's capabilities.

Whereas the fundamental Doherty characterisation approach has been concerned primarily with observing different device technology behaviour whilst embedded within various measurement prototypes, the harmonic approach is more concerned with the observation of waveforms and the emulation of impedance environments that surround a device whilst it is operating in a Doherty structure. Although this approach has been developed from a fundamental perspective, and has proved extremely useful in the design of the GaN Doherty for example, it needs to be taken further. Specifically, the harmonic environments that surround both *main* and *auxiliary* devices within the Doherty need to be considered, synthesised and perturbated in order to understand the sensitivities that exist.

In addition to the above, the activities looking at GaN and other device technology based Doherty measurement structures needs to continue, such as new generation LDMOS, with an aim of utilising improved performance devices, operating at higher drain voltage and power levels.

Other areas that are worth pursuing are detailed in the following sections.

8.1.1 Measurement-based Modelling

As part of the harmonic characterisation approach, it was anticipated that focused measurement data could be collected and used 'off-line' within a CAD environment, allowing accurate, detailed investigation and optimisation exercises based on actual measured data.

The *off-line* measurement-based behavioural model approach is particularly interesting as it allows complex, active devices to be represented using actual, focused measured data, whilst other passive circuit elements such as transmission lines can be represented using reliable and well established CAD-based components. In using the 'off-line' model approach, the importance of anticipating the drive, bias and impedance environments within the Doherty cannot be overstated, as this allows the measurement scope for such a model to be limited to a manageable subset of bias, drive and impedance conditions, thus allowing the measurement time to conduct the necessary measurements to remain reasonable. As an example, consider a FET measurement based model that responds to input voltage, gate bias, drain bias and output reflection coefficient. If the eventual environments for the model are unknown, then measurements for all combinations of these independent variables will be required, making this an unrealistic option. If the application is known to be the Doherty PA however, a good idea of these operational conditions can generally be developed, and the number of necessary measurements dramatically reduced. Using this ideal approach, it is clear that a large degree of characterisation and optimisation could be achieved within the simulation environment. The additional advantage of employing the measurement based 'off-line' behavioural models is that the process is device independent, so could be applied equally effectively for example to Doherty structures employing GaAs pHEMT, LDMOS or GaN device technologies.

Both the ability to develop measurement based non-linear models and the ability to conduct the required, focused measurements needs to be further developed. The models themselves need to respond to a number of stimuli, specifically and most importantly input voltage, and load.

8.1.2 Consideration of Harmonic termination in the Doherty

In the existing, *fundamental* characterisation approach, special measurement structures are employed that terminate odd-order harmonics into short circuits and prevent the generation of corresponding voltage spectra. A natural progression of this approach is to replace the harmonic short with an additional port through which harmonic load-pull signals can be injected. Once calibrated, this port could be used as an extension of the harmonic load-pull measurement system, through which any harmonic impedance could be presented to the output of the *main* device.

Such a structure has already been realised and is shown in Figure 211. As well as the load-pull port, this structure has a coupled line that has been matched to 50Ω, and that can be used as a directional coupler. The idea here is that the structure could be effective

in measuring the harmonic impedance at both *main* and *auxiliary* device outputs during normal Doherty operation.

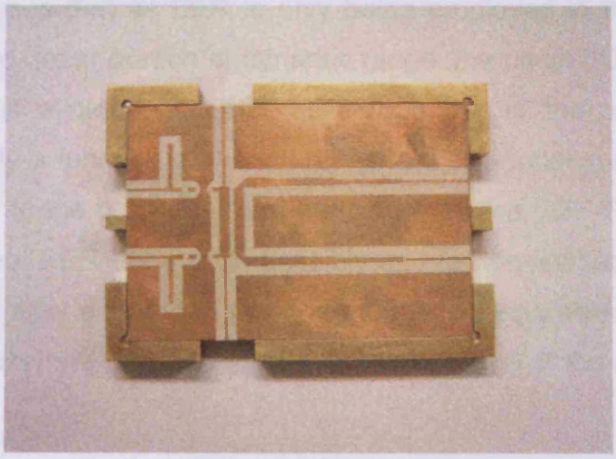


Figure 211 – Doherty structure with coupled line and load-pull port

To improve directivity of such an approach, another idea is to use two couplers, one either side of the combining line. If the devices were located at either end of the line, this approach would, using a calibration technique that would require some thought, allow calibration of reference planes at the devise insertion points. This idea needs to be further developed.

8.1.3 A Doherty employing EER

Envelope Elimination and Restoration (EER) and Doherty techniques are both very effective in enhancing PA efficiency over dynamic range. Both have limitations however, and one interesting idea is to develop a structure that combines these two approaches, benefiting from the advantages of each.

One possibility is to employ EER on the auxiliary device whilst maintaining the main device in a class-B or even class-AB state. The benefit of this approach becomes apparent when considering extended or so called asymmetrical Doherty structures that operate over wide or extended dynamic range. Usually, such Doherty structures suffer from an efficiency 'dip' between the transition point and PEP, which deepens with increasing dynamic range to the point where the overall value becomes limited. This deleterious 'dip' is due combined device efficiency and in an ideal structure is completely attributable to the relatively poor efficiency of the auxiliary device. If EER is applied to the

auxiliary device however, simulations show that it is possible to completely remove this 'dip', and establish a high efficiency plateau over the entire dynamic range.

One important advantage is that as EER is only being employed in the auxiliary device which is active only in the upper portion of dynamic range, the usual EER disadvantage of limited dynamic range is avoided. Another advantage lies in the realisation that the Doherty linearity is mostly a function of the main device trans-conductance characteristic, and is largely insensitive to the behaviour of the auxiliary device [22]. This may mean that large degrees of non-ideal EER behaviour, possibly due to non-linearity of the modulator used can be tolerated. It may also mean that the modulator requirements can be relaxed from the usual EER case where it is responsible for imparting all of the amplitude variation on the carrier.

8.1.4 A Base-band in – RF out Doherty PA

Within this thesis, there are a number of indications that suggest it may not be possible to achieve ideal Doherty behaviour using a simple, passive power division such as is used in the classical approach, the optimisation of such a structure being difficult if not impossible due to the closed nature of the structure and the internal device interaction. By employing a Doherty structure with independent inputs, it has been shown that the dynamic adjustment of the relative input phase and magnitude, along with the *auxiliary* bias profile can be used to optimise the Doherty for efficiency and linearity. This can be achieved in a number of different ways, one of which is through the use of hardware such as IQ modulators that are controlled by base-band signals that are functions derived from the instantaneous magnitude of the input signal.

When considering continuous, rapidly changing modulated excitation such as WCDMA, derivation of these signals using envelope detection becomes problematical due to the inherent delays associated with simple detectors and the processing involved.

One way to overcome this problem is to consider the Doherty as a transmitter and not a PA architecture. Viewed from this perspective, it is possible to envisage a Doherty structure that accepts base-band I and Q modulation, and produces modulated RF. The advantage is that the necessary base-band signals are available and can be used to generate the necessary base-band control signals 'up-front' before modulation and amplification occur, thus overcoming any delay issues. In fact, such a structure would tolerate significant base-band processing delays as the problem becomes one of aligning the base-band signals, such that they are applied to the modulating structure in a phase-coherent manner.

8.1.5 Optimisation of output matching networks

In the ideal passive Doherty impedance environment, all odd harmonic impedances are the same (shorts) and all even harmonic impedances are the same ($2R_{opt}$). In reality however, line behaviour, and the usually unavoidable delay associated with the transmission path between both *main* and *auxiliary* devices, and the central $\lambda/4$ transformer cause non ideal behaviour in the output structure. This is evident in Figure 212 and Figure 213 where an ideal Doherty output structure and a realistic structure are compared.

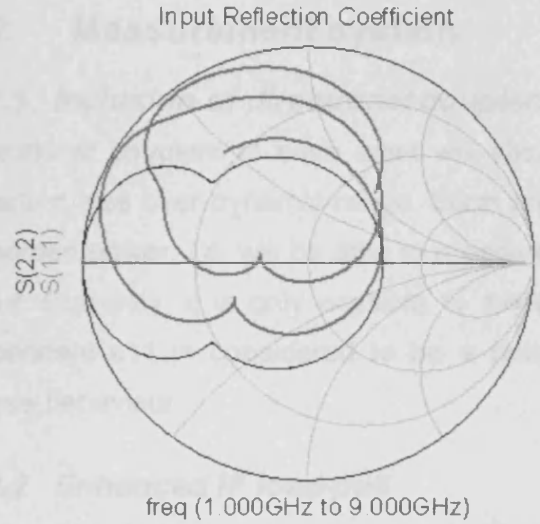


Figure 212 – ideal and realistic O/P matching network behaviour - Smith Chart

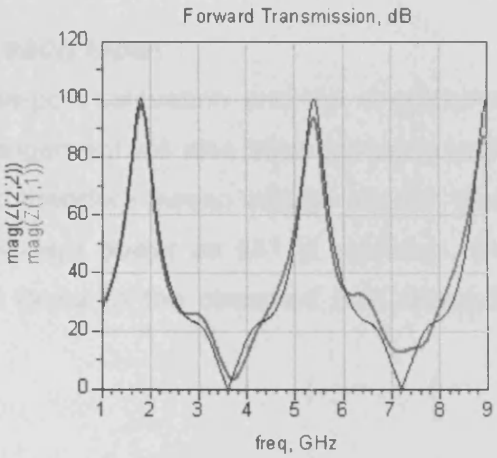


Figure 213 – ideal and realistic O/P matching network behaviour – magnitude

The additional offset between the package plane and device plane has significant consequences – Firstly, the shorted stub must be tuned to accommodate this additional length and to ensure the correct impedances are presented to the *main* device at different frequencies. In the case of the simulation, the line length has been reduced to 0.22λ. Even following tuning, the offset length causes the quality of the shorts presented to even-order harmonics gets progressively worse with frequency. For example, whereas the short presented at 3.6 GHz is good (3Ω), the short presented to the fourth harmonic has degraded to 15Ω.

What is clear, from the simple simulations shown is that even small additional lengths introduced by offsetting the device plane from the combining line interface cause significant problems. One way to address this is through the introduction of offset lines, that when combined with the existing delays, cause the correct phase properties to exist at both *main* and *auxiliary* device planes. The disadvantage of this approach is of course

that these will be physically large and will introduce additional loss. For this reason, it is considered a much better idea to locate devices very close to line in the first place, and maybe dispense with the package all together, adopting a hybrid style approach.

It has been shown how the normal behaviour of this transformer limits the bandwidth of the Doherty, and another activity that could form part of this work is the consideration of alternative output matching architectures that allow the necessary impedance inversion to take place, but offer constant group-delay over a specified bandwidth. It is considered that this approach, if possible could significantly improve the linearity of the Doherty.

8.2 Measurement system

8.2.1 Inclusion of directional couplers at each input

Directional couplers at each input will allow one-port calibration and the measurement insertion loss over dynamic range. Such an arrangement will also allow measurement of absorbed power, i.e. will be able to measure and therefore sweep voltage at each device input. Currently, it is only possible to sweep incident power as s11 is unknown. Drive dependent s11 is considered to be a potential factor in the observed bias dependent phase behaviour.

8.2.2 Enhanced IF load-pull

The multi-tone measurement system's IF load-pull capability can currently only cater for the most significant IF component. When using even simple modulated excitations with the Doherty, there are a number of IF components generated, and it is necessary to load-pull each of these. Ideally, a non-sinusoidal load-pull approach needs to be developed.

8.2.3 Alternative phase alignment approaches

The Microwave Transition Analyser is clearly under-utilised when used only for the task of simple phase alignment in the Doherty measurement systems. One other approach identified was to use a commercially available integrated circuit: Analog Devices' AD8302. This is a fully integrated RF IC for measuring amplitude and the phase between two independent input signals. The device can be used from low frequencies up to 2.7GHz and generates two voltages that are linear functions of the relative phase and magnitude of the two input channels. Originally designed for RF/IF PA Linearization and precise RF power control applications, this device could be used here to mimic the role of the MTA in monitoring the relative input phase and magnitude of the stimulus applied to the Doherty. This circuit has already been fabricated, but has not yet been implemented and integrated into the measurement system capability.

8.3 Doherty Optimisation Approaches

8.3.1 Linearisation through dynamic adjustment of Relative Input Phase and Magnitude

Although exhibiting high efficiency, measurements have shown how Doherty measurement structures can exhibit significant gain and gain-phase variation in the high power region of operation. As has been demonstrated, by varying the relative phase of the RF stimulus applied to *main* and *auxiliary* devices of the Doherty structure, it is possible to generate three dimensional gain and gain-phase surfaces that clearly illustrate the dynamic phase conditions that can lead to flat gain and constant gain phase. By introducing additional measurement variables in the form of relative input magnitude or *auxiliary* device bias profile, it is possible to generate collections of 'stacked' surfaces, and therefore multiple, constant gain and gain-phase contours that effectively 'expand' the optimisation space. When considered over active dynamic range as shown in Figure 214, Figure 215 and Figure 216, it is possible to understand how choosing specific, relative input phase and relative input magnitude combinations for each value of P_{in} can lead to 'best choice' or optimum linearity and efficiency.

Figure 217 illustrates cross sections through the collections of gain-phase and gain surfaces of Figure 216 and Figure 214 respectively at a value of input power corresponding to approximately PEP-3dB. The markers show the constant gain-phase and constant gain contours, for all surfaces, and effectively represent the choices an optimiser would have if trying to reach the best gain/gain phase compromise.

This is considered a very interesting and promising optimisation approach that has fallen outside the *main* scope of the research, and that could be pursued using single-tone analysis and corroborated using modulated analysis.

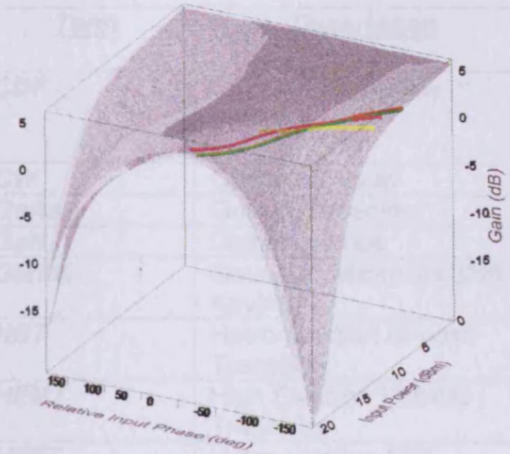


Figure 214 – I/P power vs. gain vs. relative input phase

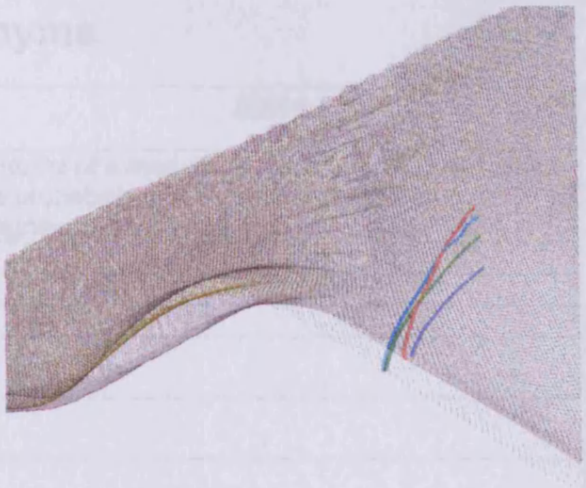


Figure 215 - I/P power vs. gain vs. relative input phase (zoomed). Each surface represents one case of relative input magnitude offset

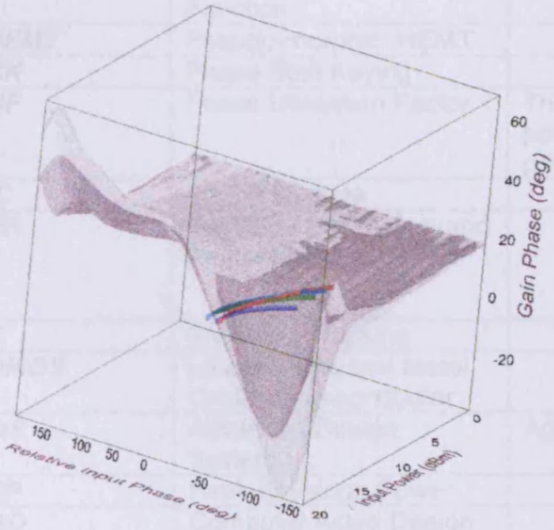


Figure 216 - I/P power vs. gain-phase vs. relative input phase

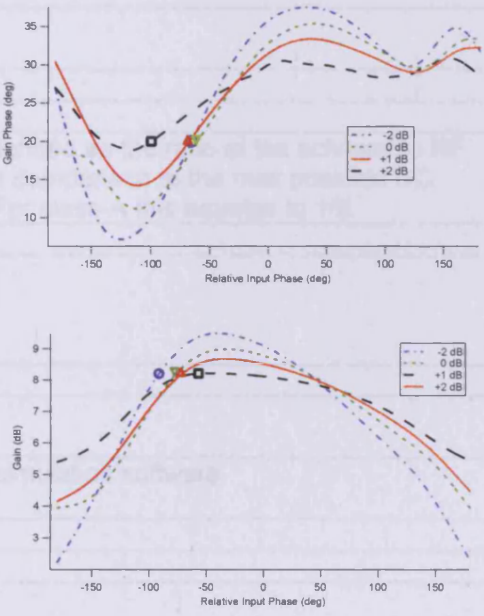


Figure 217 gain-phase vs relative input phase for various Auxiliary device P_{in} offset

Glossary of Terms and Acronyms

Term	***Description***	***Notes***
CDF	Cumulative Density Function	In terms of a modulation envelope, CDF describes the probability that a particular envelope magnitude will be reached.
CW	Constant Wave	
GaAs	Gallium Arsenide	
GaN	Gallium Nitride	
GMSK	Gaussian Minimum Shift Keying	
HBT	Hetro-junction Bi-polar Transistor	
HEMT	High Electron Mobility Transistor	
HFET	Hetro-junction FET	
InGaP	Indium Gallium Phosphide	
InP	Indium Phosphide	
LF	Low Frequency	
MESFET		
MF	Medium Frequency	
PAR	Peak to Average power Ratio	
PDA	Personal Digital Assistant	
PDF	Probability Density Function	
pHEMT	Pseudo-morphic HEMT	
PSK	Phase Shift Keying	
PUF	Power Utilisation Factor	This is defined as the ratio of the achievable RF power in comparison to the max possible DC power. For class-A this equates to 1/8.
SiC	Silicon Carbide	
EER	Envelope Elimination and Restoration	
ET	Envelope Tracking	
LDMOS	Laterally Diffused Metal Oxide Semi-conductor	
ADS	Advanced Design System	Agilent simulation software
PEP	Peak Envelope Power	
CAD	Computer Aided Design	
ACPR	Adjacent Channel Power Ratio	
EVM	Error Vector Magnitude	
TRL	Through-Reflect-Line	Calibration technique
AM-PM	Amplitude Modulation to Phase Modulation conversion	
ESG	E-series Signal Generator	
GPIB	General Purpose Instrumentation Bus	
SD	Standard Deviation	
GSM	Global System for	

	Mobile communication	
W-CDMA	Wide-band Code Division Multiple Access	
PDF	Probability Density Function	
SLOT	Short-Load-Open-Through	Calibration technique

References

[1] W. J. Bryon, "Arcs and sparcs, Part-1," *Communications quarterly*, vol. 4, pp. 27-43, spring 1994.

[2] W. J. Bryon, "The arc method of producing continuous waves," *Communications quarterly*, vol. 8, pp. 47-65, Summer 1998.

[3] K. M. MacIlvain and W. H. Freedman, *Radio Transmitters and Carrier Currents*, vol. 3: Scranton PA: International Textbook Company, 1994.

[4] E. H. Armstrong, "A METHOD OF REDUCING DISTURBANCES IN RADIO SIGNALING BY A SYSTEM OF FREQUENCY MODULATION," *Proceedings of the Instute of Radio Engineers*, vol. 24, 1936.

[5] F. Raab, P. Asbeck, S. Cripps, P. Kenington, Z. Popovic, N. Pothecary, J. Sevic, and N. Sokal, "RF and Microwave Power Amplifier and Transmitter Technologies - Part 1," in *High Frequency Design*, 2003, pp. 22–36.

[6] R. v. Nee and R. Prasad, *OFDM for Wireless Multimedia Communications*: MA: Artech House, 2000.

[7] CEPT, "ADJACENT BAND COMPATIBILITY BETWEEN UMTS AND OTHER SERVICES IN THE 2 GHz BAND," European Conference of Postal and Telecommunications Administrations ERC REPORT 65, 2000.

[8] W. J. Kim, P. Stapleton, K. J. Cho, and J. H. Kim, "Digital Presistortion of a Doherty Amplifier with a Weak Memory within a Connected Solution," presented at IEEE MTT-S Int Microwave Symposium Digest, 2004.

[9] M. Iwamoto, W. Aracely, P. F. Chen, A. G. Metzger, L. E. Larson, and P. M. Asbeck, "An Extended Doherty Amplifier with High Efficiency over a Wide Dynamic Range," presented at IEEE Transactions on Microwave Theory and Techniques, 2001.

[10] P. Kenington, S. R. Ring, A. Bateman, and A. S. Tavener, "Meeting the Challenges of High Efficiency Power Amplifiers," presented at Microwave and RF Conference, Wembley, London, UK., 1999.

[11] F. Raab, P. Asbeck, S. Cripps, P. Kenington, Z. Popovic, N. Pothecary, J. Sevic, and N. Sokal, "RF and Microwave Power Amplifier and Transmitter Technologies - Part 4," in *High Frequency Design*, 2003, pp. 38–49.

[12] J. Sevic, "Efficient parallel stage amplifier (US Patent)," in *Patent*, vol. 5,872,481, U. P. Office, Ed. U.S.A, 1999.

[13] S. Brozovich, "High effiiciency multiple power level amplifier circuit (US Patent)." U.S.A, 1999.

[14] F. H. Raab and D. J. Rupp, "Highe Efficiency Single-Sideband HF/VHF transmitter based upon envelope elimination and restoration," presented at HF Radio Systems and Techniques (HF '94), York, UK, 1994.

[15] J. Staudinger and e. al., "High Efficiency CDMARF Amplifier using Dynamic Envelope Tracking Technique," presented at Int. Microwave Symp. Digest, Boston, MA, 2000.

[16] G. Hanington, P. F. Chen, P. M. Asbeck, and L. E. Larson, "High-efficiency power amplifier using dynamic power-supply voltage for CDMA applications," *IEEE Transactions on microwave theory tech.*, vol. 47, pp. 1471-1476, 1999.

[17] G. Hanington, A. Metzger, P. M. Asbeck, and H. Finlay, "Integrated DC-DC converter using GaAs HBT technology," *Electronics Letters*, vol. 35, pp. 2110-2112, 1999.

[18] D. R. Anderson and W. H. Cantrell, "High efficiency inductor-coupled high level modulator," presented at International Microwave Symposium, Phoenix, AZ, 2001.

[19] F. H. raab, "Efficiency of outphasing power-amplifier systems," *IEEE Trans. Commun.*, vol. COM-33, pp. 1094-1099, 1985.

[20] R. Langridge, T. Thornton, P. M. Asbeck, and L. E. Larson, "A power re-use technique for improving efficiency of outphasing microwave power amplifiers," *IEEE Trans. Microwave Theory Tech.*, vol. 47, pp. 1467-1470, 1999.

[21] S. C. Cripps, *RF Power Amplifiers for Wireless Communications*: Artech House, 1999.

[22] S. C. Cripps, *Advanced Techniques in Power Amplifier Design*: Artech House, 2002.

[23] W. H. Doherty, "A new high efficiency power amplifier for modulated waves," presented at IRE, 1936.

[24] F. Raab, "Efficiency of Doherty RF Power amplifier Systems," *IEE Transactions on Broadcasting*, vol. BC-33, 1987.

[25] D. M. Pozar, *Microwave Engineering*, 2nd ed. New York: Wiley, 1998.

[26] I. WaveMetrics, "Igor Pro 5.0," 5.03 ed, 11/2004, pp. User Manual.

[27] P. McGovern, J. Benedikt, P. J. Tasker, J. Powell, K. P. Hilton, J. L. Glasper, R. S. Balmer, T. Martin, and M. J. Uren, "Analysis of DC-RF Dispersion in AlGaN/GaN HFET's Using Pulsed I-V and Time-Domain Waveform Measurements," presented at IEEE MTT-S, Long Beach, CA, USA, 2005.

[28] P. McGovern, P. J. Tasker, J. Powell, K. P. Hilton, J. L. Glasper, R. S. Balmer, T. Martin, and M. J. Uren, "Experimental Investigation of DC-RF Dispersion in AlGaN/GaN HFET's Using Pulsed I-V and Time-Domain Waveform Measurements," presented at The International Conference on Compound Semiconductor Manufacturing Technology, New Orleans, USA., 2005.

[29] P. McGovern, D. J. Williams, P. J. Tasker, J. Benedikt, J. Powell, K. P. Hilton, R. S. Balmer, T. Martin, and M. J. Uren, "Single-tone and two-tone time-domain large signal characterization of GaN HFETs operated in class A," 2004.

[30] Y. Zhao, M. Iwamoto, L. E. Larson, and P. M. Asbeck, "Doherty Amplifier with DSP Control to Improve Performance in CDMA Operation," presented at IEEE MTT-S Int Microwave Symposium Digest, 2004.

[31] J. Lees, J. Benedikt, M. Goss, and P. J. Tasker, "Measurement Based Optimisation of an Adaptive Bias Doherty Structure," presented at IEEE MTT-S International Microwave Symposium, 2003.

[32] J. Lees, J. Benedikt, K. P. Hilton, J. Powell, R. S. Balmer, M. J. Uren, T. Martin, and P. J. Tasker, "Characterisation of an Experimental Gallium Nitride Microwave Doherty Amplifier," presented at EUMC, Paris, 2005.

[33] J. Lees, J. Benedikt, K. P. Hilton, J. Powell, R. S. Balmer, M. J. Uren, T. Martin, and P. J. Tasker, "An Experimental Gallium Nitride Microwave Doherty Amplifier," *IEE ELECTRONICS LETTERS*, vol. 41, pp. 1284-1285, 2005.

[34] J. R. Gajadharsing, O. Bosma, and P. Westen, "Analysis and Design of a 200W LDMOS Based Doherty Amplifier for 3G Base Stations," presented at IEEE MTT-S Int Microwave Symposium Digest, 2004.

[35] H. T. Jeong, M. H. Yeon, S. W. Kim, and I. S. Chang, "Design of the Doherty Amplifier with Push-Pull Structure Using Balun Transformer," presented at IEEE MTT-S Int Microwave Symposium Digest, 2004.

[36] C. Jeonghyeon, K. Jangheon, K. Bumman, L. Jong Sung, and K. Sang Hoon, "Highly efficient power amplifier for CDMA base stations using Doherty configuration," presented at IEEE MTT-S International, 2004.

[37] B. Shin, J. Cha, J. Kim, Y. Woo, J. Yi, and B. Kim, "Linear Power Amplifier based on a 3-Way Doherty Amplifier with Pre-distorter," presented at IEEE MTT-S Int Microwave Symposium Digest, 2004.

[38] H. Takenaka, K. Takahashi, K. Ishikura, K. Hasegawa, K. Asano, and M. Kanamori, "A 240W Doherty GaAs Power FET Amplifier with High Efficiency and Low Distortion fow W-CDMA Base Stations," presented at IEEE MTT-S Int Microwave Symposium Digest, 2004.

[39] S. Goto, T. Kunii, A. Inoue, K. Izawa, T. Ishikawa, and Y. Matsuda, "Efficiency Enhancement of a Doherty Amplifier with Combination of Class-F and Inverse Class-F Schemes for S-Band Base Station Applications," presented at IEEE MTT-S Int Microwave Symposium Digest, 2004.

[40] J. Olah and S. Gupta, "Power Amplifier Design using Measured Load Pull Data," in *Microwave Engineering Europe*, 2003.

[41] J. Wood and D. Root, *Fundamentals of Nonlinear Behavioral Modelling for RF and Microwave Circuits*: Artech House, 2005.

[42] Y. Yang, J. Cha, B. Shin, and B. Kim, "A Microwave Doherty Amplifier Employing Envelope Tracking Technique For High Efficiency and Linearity," presented at IEEE Microwave and Wireless Components Letters, 2003.

[43] J. Cha, Y. Yang, B. Shin, and B. Kim, "An Adaptive Bias Controlled Power Amplifier with a Load-Modulated Combining Scheme for High Efficiency and Linearity," presented at IEEE MTT-S Int Microwave Symposium, 2003.

[44] R. J. McMorrow, D. M. Upton, and P. R. Maloney, "The Microwave Doherty Amplifier," presented at IEEE MTT-S International Microwave Symposium Digest, 1994.

[45] J. Lees, A. Haczewski, J. Benedikt, and P. J. Tasker, "An Automated Multiple-Stimulus Measurement System for Characterising Multiple-Device Amplifiers," presented at 34th EuMC, 2004.

[46] J. Benedikt and P. J. Tasker, "High Power Time-Domain Measurement Bench for Power Amplifier Development," presented at 60th ARFTG Conference Digest, 2002.

[47] J. Benedikt, R. Gaddi, P. J. Tasker, M. Goss, and M. Zadeh, "High power time domain measurement system with active harmonic load-pull for high efficiency base station amplifier design," *IEEE Trans. Microwave Theory Tech.*, vol. 48, pp. 2617 –2624, 2000.

[48] J. Lees, A. Sheikh, J. Benedikt, and P. J. Tasker, "The design of a GaN Dohery amplifier using waveform measurements and active harmonic load-pull," presented at INMMiC, Aveiro, Portugal, 2006.

[49] J. Fleury and O. Bernard, "Designing and Characterizing TRL Fixture Calibration Standards for Device Modeling," *Applied Microwave and Wireless*, pp. 26-42.

[50] V. Y. C. Leong, "Microstrip-Based Implementation of the 'Thru-Reflect-Line' Calibration Technique for Vector Network Analyzers," *Journal of the Institution of Engineers*, vol. 33, 1993.

[51] D. Metzger, " Improving TRL* Calibrations of Vector Network Analyzers," *Microwave Journal*, 1995.

[52] S. C. Cripps, "Reduced Conduction Angle-waveform Analysis," in *RF Power Amplifiers for Wireless Communications*: Artech House, 1999, pp. 46-50.

[53] "The Microwave Transition Analyser: Measure 25ps Transitions in Switched and Pulsed Microwave Components," in *Product Note: 70820-2*: Hewlett Packard, 1991.

[54] P. Kennington, *High Linearity RF Amplifier Design*: Artech House, 2000.

[55] N. Pothecary, *Feedforward Linear Power Amplifiers*. Boston/London: Artech House, 1999.

[56] D. J. Williams, J. Leckey, and P. J. Tasker, "A study of the effect of envelope impedance on inter-modulation asymmetry using a two-tone time domain measurement system," presented at MTT-S, 2002.

[57] J. H. K. Voulevi, T. Rahkonen, and P. A. Manninen, "Measurement Technique for Characterising Memory Effects in RF Power Amplifiers," *IEEE Trans. on Microwave Theory and Techniques*, vol. 49, pp. 1383 - 1389, 2001.

[58] p. u. d. Agilent, *ESG-D series signal generator - User Manual*.

[59] Y. Suzuki, S. Mizuta, T. Hirota, and Y. Yamao, "Linearised Doherty Amplifier using a New Digital Predistorter Compensating Frequency Dependent Intermodulation Distortion for Mobile Radio," presented at 10th Asia-Pacific Conference on Communications, 2004.

[60] Y. Yang, J. Yi, Y. Woo, and B. Kim, "Experimental Investigation on Efficiency and Linearity of Microwave Doherty Amplifier," presented at IEEE MTT-S International, 2001.

[61] J. R. Gajadharsing, O. Bosma, and P. van Westen, "Analysis and design of a 200 W LDMOS based Doherty amplifier for 3 G base stations," 2004.

[62] I. Takenaka, H. Takahashi, K. Ishikura, K. Hasegawa, K. Asano, and M. Kanamori, "A 240 W Doherty GaAs power FET amplifier with high efficiency and low distortion for W-CDMA base stations," 2004.

[63] A. Bindra, "More Options For RF Power-Amplifier Designers," in *Electronic Design*, 2002.

[64] F. O'Keefe, J. S. Atherton, W. Boshe, P. Burgess, N. I. Cameron, and C. M. Snowden, "GaAs pHEMT-Based Technology for Microwave Applications in a Volume MMIC Production Environment on 150 mm Wafers," *IEEE Transactions on Semi-conductor Manufacturing*, vol. 16, pp. 376-383, 2003.

[65] R. J. Trew, "Wide Bandgap Semiconductors for Microwave Power Amplifiers," in *microwave*, 2000, pp. 47-54.

[66] L. Jong-Wook, L. F. Eastman, and K. J. Webb, "A gallium-nitride push-pull microwave power amplifier," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 51, pp. 2243, 2003.

[67] M. Werquin, C. Gaquiere, Y. Guhel, N. Vellas, D. Theron, B. Boudart, V. Hoel, M. Germain, J. C. De Jaeger, and S. Delage, "High power and linearity performances of gallium nitride HEMT devices on sapphire substrate," *Electronics Letters*, vol. 41, pp. 46, 2005.

[68] H. Ohashi, "Power electronics innovation with next generation advanced power devices," 2003.

[69] *Accent DIVA Models D210, D225, D225HBT, D265 Dynamic I-V Analyzer, User Manual*, vol. 1.0: Accent Optical Technologies, 2001.

[70] L. Dunleavy, W. Clausen, and T. Weller, "Pulsed I-V for Nonlinear Modeling," *Microwave Journal*, 2003.

[71] J. Benedikt, "Novel High Frequency Power Amplifier Design System," in *Division of Electronics*, vol. PhD. Cardiff: Cardiff University, 2002.

[72] P. J. Tasker, "Non-Linear Vector Network Analyser – Simply what is it and what can it do," presented at Non-linear Measurement Workshop, ARFTG, 2001.

[73] P. J. Tasker, "Non-Linear Vector Network Analyser – Realisation and Application," presented at Non-linear Measurement Workshop, 30th EuMC, 2000.

[74] D. Pavlidis, "Recent Advances in III-V Nitride Electronic Devices," presented at IEEE Electron Device meeting digest, 2004.

[75] M. J. Uren, A. R. Barnes, T. Martin, R. S. Balmer, K. P. Hilton, D. G. Hayes, and M. Kuball, "GaN devices for microwave applications," presented at 10th IEEE Int. Symp. on Electron Devices for Microwave and Optoelectronic Applications (EDMO'2002), Manchester, UK, 2002.

[76] R. S. Balmer, K. P. Hilton, K. J. Nash, M. J. Uren, D. J. Wallis, D. Lee, T. Martin, A. Wells, and M. Missous, "Analysis of thin AlN carrier exclusion layers in AlGaN/GaN microwave heterojunction field effect transistors," *Semicond. Sci. Tech*, vol. 19, pp. L65-67, 2004.

[77] M. Wolter, P. Javorka, A. Fox, M. Marso, and E. al, "Photo-ionization spectroscopy of traps in AlGaN/GaN high-electron mobility transistors," *Journal of Electronic Materials*, 2002.

[78] Agilent-Technologies, "ADS2004 User Manual," 2004.

[79] Y. Yang, J. Cha, B. Shin, and B. Kim, "A Fully Matched N-Way Dohetrty Amplifier with Optimized Linearity," *IEEE Trans. Microwave Theory Tech.*, vol. 51, 2003.

Appendix 1. IF Load-Pull and Calibration

Consider the signal flow graph for the simplified IF load-pull system consisting of RF and IF bias networks along with the directional coupler, as shown in Figure 99.

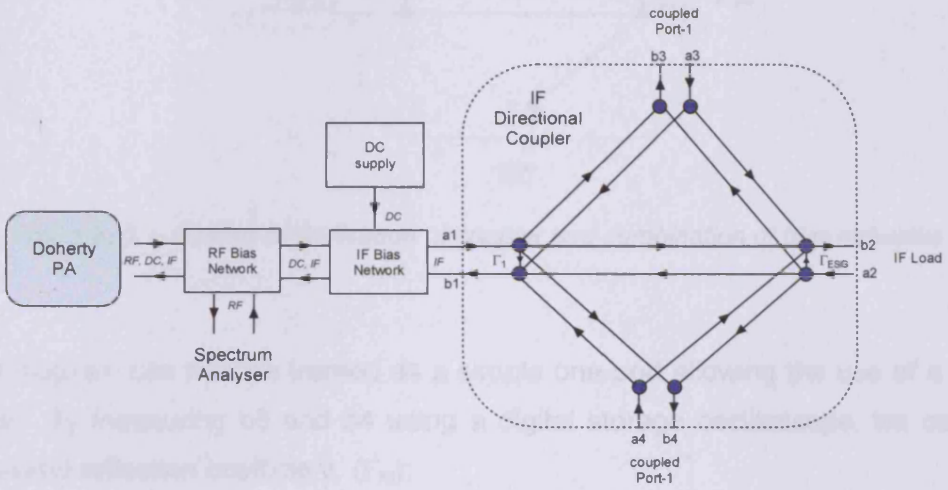


Figure 218 – Signal flow representation of directional coupler along with other components that comprise the IF load-pull capability.

If we assume that the directional coupler is ideal and perfectly matched, the flow diagram can be simplified such that that energy only flows out of the coupled ports and is completely absorbed in ideal terminations at its outputs, as shown in Figure 219.

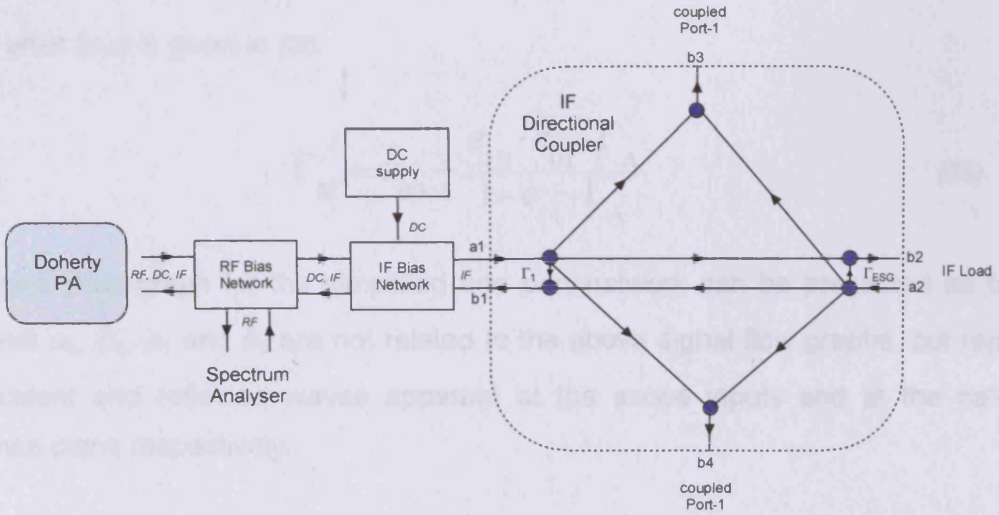


Figure 219 – simplified Signal flow representation assuming ideal coupler.

This can be further simplified by assuming ideal coupler directivity, and that other components in the IF signal path can be considered as a single, combined network.

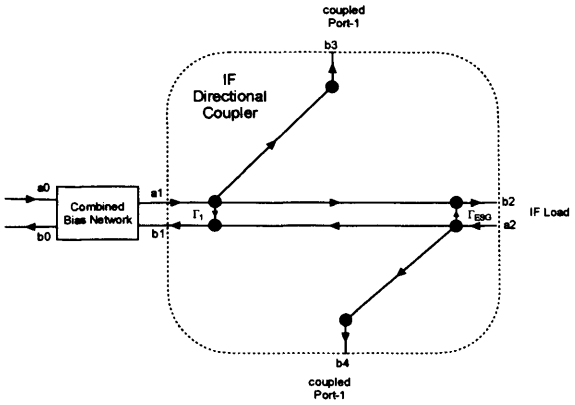


Figure 220 – Further simplification of coupler and combination of bias networks

The flow diagram can now be treated as a simple one-port allowing the use of a one port calibration. By measuring b3 and b4 using a digital storage oscilloscope, we can obtain the measured reflection coefficient, (Γ_M):

$$\Gamma_m = \frac{b3}{b4} \tag{34}$$

The one-port error formula that relates the actual reflection coefficient apparent at the reference plane (Γ_A) to the measured reflection coefficient at the oscilloscope (Γ_M), using the four error terms: directivity error (e_{00}), reflection tracking errors (e_{10} & e_{01}) and source match error (e_{11}) is given in *(35.*

$$\Gamma_M = e_{00} + \frac{e_{10} \cdot e_{01} \cdot \Gamma_A}{1 - e_{11} \cdot \Gamma_A} \tag{35}$$

The signal flow graph for the simplified one port network can be presented as follows. Note that a_0, b_0, a_1 and b_1 are not related to the above signal flow graphs, but represent the incident and reflected waves apparent at the scope inputs and at the calibrated reference plane respectively.

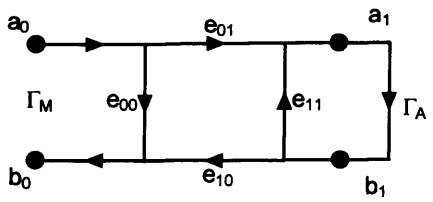


Figure 221 – Signal flow graph representation of simplified IF arrangement

Note that Γ_A represents the reflection coefficient at the calibrated reference plane, and for the one-port SOL calibration process will take on ideal values of the calibration standards. Note that imperfections and delays associated with the calibration standards used are ignored due to the low calibration frequencies used.

$$\begin{aligned}\Gamma_{Load} &= (0,0)\\ \Gamma_{Open} &= (1,0)\\ \Gamma_{Short} &= (-1,0)\end{aligned} \qquad (36)$$

Substituting each of these, in turn, into (35) yields three equations with three unknowns, where Γ_M^L is the measured reflection coefficient Γ_M with a load standard attached to the reference plane, Γ_M^o is the measured reflection coefficient Γ_M with an open standard attached to the reference plane, and so on.

Load
$$\Gamma_M^L = e_{00} \qquad (37)$$

Open
$$\Gamma_M^o = e_{00} + \frac{e_{10} \cdot e_{01} \cdot \Gamma_{Open}}{1 - e_{11} \cdot \Gamma_{Open}} \qquad (38)$$

Short
$$\Gamma_M^s = e_{00} + \frac{e_{10} \cdot e_{01} \cdot \Gamma_{Short}}{1 - e_{11} \cdot \Gamma_{Short}} \qquad (39)$$

Substituting (37) into (38) yields

$$\Gamma_M^o = \Gamma_M^L + \frac{e_{10} \cdot e_{01} \cdot \Gamma_{Open}}{1 - e_{11} \cdot \Gamma_{Open}} \qquad (40)$$

and

$$e_{10}e_{01} = \frac{\left(\Gamma_M^o - \Gamma_M^L\right)\left(1 - e_{11} \cdot \Gamma_{Open}\right)}{\Gamma_{Open}} \qquad (41)$$

Subtracting (39) from into (38) gives

$$\Gamma_M^s - \Gamma_M^o = \left[\frac{\left(e_{10}e_{01} \cdot \Gamma_{Short}\right)}{1 - e_{11} \cdot \Gamma_{Short}}\right] - \left[\frac{\left(e_{10}e_{01} \cdot \Gamma_{Open}\right)}{1 - e_{11} \cdot \Gamma_{Open}}\right] \qquad (42)$$

And

$$\Gamma_M^s - \Gamma_M^o = e_{10}e_{01}\left[\frac{\left(\Gamma_{\text{Short}}\right)}{1-e_{11}\cdot\Gamma_{\text{Short}}} - \frac{\left(\Gamma_{\text{Open}}\right)}{1-e_{11}\cdot\Gamma_{\text{Open}}}\right] \qquad (43)$$

Substituting (41) into (43) yields

$$\Gamma_M^s - \Gamma_M^o = \frac{\left(\Gamma_M^o - \Gamma_M^L\right)\left(1-e_{11}\cdot\Gamma_{\text{Open}}\right)}{\Gamma_{\text{Open}}}\cdot\left[\frac{\left(\Gamma_{\text{Short}}\right)}{1-e_{11}\cdot\Gamma_{\text{Short}}} - \frac{\left(\Gamma_{\text{Open}}\right)}{1-e_{11}\cdot\Gamma_{\text{Open}}}\right] \qquad (44)$$

Simplifying

$$\Gamma_M^s - \Gamma_M^o = \frac{\left(\Gamma_M^o - \Gamma_M^L\right)\left(1-e_{11}\cdot\Gamma_{\text{Open}}\right)}{\Gamma_{\text{Open}}}\cdot\left[\frac{\Gamma_{\text{Short}}\left(1-e_{11}\cdot\Gamma_{\text{Open}}\right)-\Gamma_{\text{Open}}\left(1-e_{11}\cdot\Gamma_{\text{Short}}\right)}{\left(1-e_{11}\cdot\Gamma_{\text{Short}}\right)\left(1-e_{11}\cdot\Gamma_{\text{Open}}\right)}\right]$$

$$\Gamma_M^s - \Gamma_M^o = \frac{\left(\Gamma_M^o - \Gamma_M^L\right)}{\Gamma_{\text{Open}}}\cdot\left[\frac{\Gamma_{\text{Short}}\left(1-e_{11}\cdot\Gamma_{\text{Open}}\right)-\Gamma_{\text{Open}}\left(1-e_{11}\cdot\Gamma_{\text{Short}}\right)}{1-e_{11}\cdot\Gamma_{\text{Short}}}\right]$$

$$\frac{\Gamma_M^s - \Gamma_M^o}{\Gamma_M^o - \Gamma_M^L} = \frac{1}{\Gamma_{\text{Open}}}\left[\frac{\Gamma_{\text{Short}}\left(1-e_{11}\cdot\Gamma_{\text{Open}}\right)-\Gamma_{\text{Open}}\left(1-e_{11}\cdot\Gamma_{\text{Short}}\right)}{1-e_{11}\cdot\Gamma_{\text{Short}}}\right]$$

$$\frac{\Gamma_M^s - \Gamma_M^o}{\Gamma_M^o - \Gamma_M^L} = \frac{1}{\Gamma_{\text{Open}}}\left[\frac{\Gamma_{\text{Short}} - \Gamma_{\text{Open}}}{1-e_{11}\cdot\Gamma_{\text{Short}}}\right]$$

$$\frac{\Gamma_M^s - \Gamma_M^o}{\Gamma_M^o - \Gamma_M^L} = \left[\frac{\Gamma_{\text{Short}} - \Gamma_{\text{Open}}}{\Gamma_{\text{Open}}}\right]\cdot\frac{1}{1-e_{11}\Gamma_{Short}}$$

and (45)

$$\cdot\frac{1}{1-e_{11}\Gamma_{Short}} = \frac{\Gamma_M^s - \Gamma_M^o}{\Gamma_M^o - \Gamma_M^L}\cdot\left[\frac{\Gamma_{\text{Open}}}{\Gamma_{\text{Short}} - \Gamma_{\text{Open}}}\right]$$

Now, let

$$K = \frac{\Gamma_M^s - \Gamma_M^o}{\Gamma_M^o - \Gamma_M^L} = \left[\frac{\Gamma_{\text{Open}}}{\Gamma_{\text{Short}} - \Gamma_{\text{Open}}}\right], \text{ hence } K = \frac{1}{1-e_{11}\cdot\Gamma_{\text{Short}}} \qquad (46)$$

Such that

$$e_{11} = \frac{K-1}{K} \cdot \frac{1}{\Gamma_{Short}} \tag{47}$$

So, it is now possible to find coefficients e00, e01e10 and e11 from (37), (41) and (47) respectively. By rearranging (35), it is possible to obtain an expression for Γ_A in terms of the error coefficients and the measured reflection coefficient

$$\Gamma_A = \frac{\Gamma_M - e_{00}}{e_{10}e_{01} + \Gamma_M e_{11} - e_{00}e_{11}} \tag{48}$$

So using the above approach, it is possible to measure the IF load being presented to the Doherty. In addition to this, if an active signal source is used to inject energy into the IF load-pull port as defined in Figure 99, then the IF load can be controlled.

By using software to control this process, the system firstly measures the IF reflection coefficient, and then calculates and applies the required phase and magnitude of IF load pull in order to achieve the required load.

Appendix 2. Harmonics and the Doherty

Analysis approach

The following approach uses the ADS simulation environment and a relatively ideal device model to identify the harmonic behaviour of classical, adaptive-bias and input-attenuation Doherty approaches. Behaviour is initially summarised in terms of device output current spectra as for a purely trans-conductive device, this quantity is largely insensitive to harmonic impedance. With this knowledge, it is possible to identify the harmonic terminations required in achieving ideal performance in each Doherty implementation, to discuss the difficulties in achieving these conditions and to analyse the consequences of non-ideal harmonic termination.

Spectral current behaviour for the different approaches

Figure-222 and Figure-223 show the harmonic spectral current produced by *main* and *auxiliary* devices when configured in the input-attenuation Doherty approach, where both devices are biased near pinch-off (class-B).

One of the advantages of this approach is that the significant odd-order harmonics are naturally suppressed through the use of optimal class-B static biasing, which is evident from the spectral current plots shown in Figure-223. Ideal Doherty behaviour would generally then be recovered by terminating the dominant even-order harmonics using a shorted quarter-wave line.

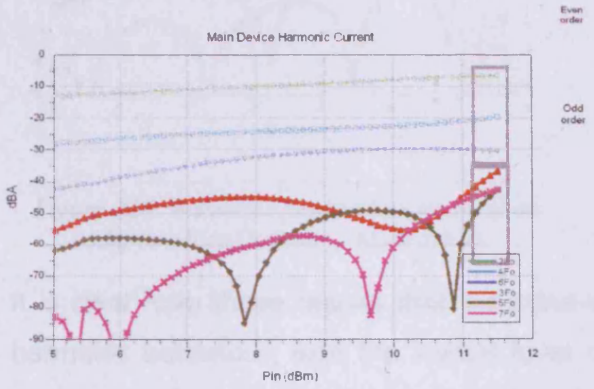


Figure-222 harmonic current behaviour of input-attenuation Doherty - Main device

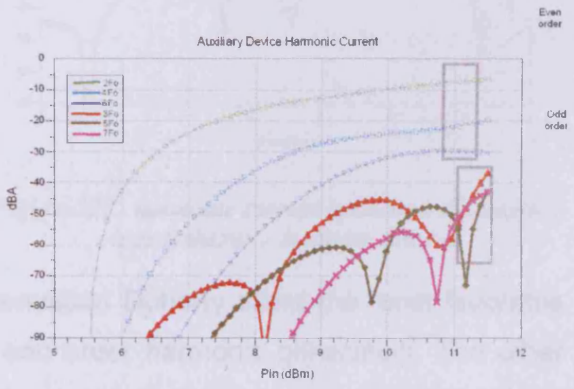


Figure-223 harmonic current behaviour of input-attenuation Doherty – Auxiliary device

Figure-224 and Figure-225 show the harmonic behaviour of the classical Doherty approach, where the *main* device biased near pinch-off, and the *auxiliary* device is biased in the required depth of class-C.

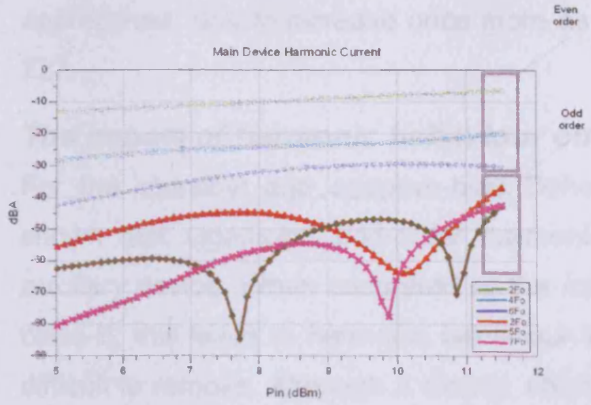


Figure-224 harmonic current behaviour of classical Doherty - Main device

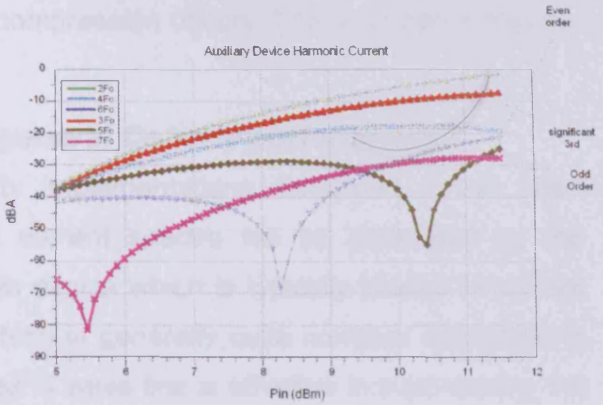


Figure-225 harmonic current behaviour of classical Doherty - Auxiliary device

Similarly, Figure-227 and Figure-226 show the harmonic behaviour for the adaptive-bias approach, where as in all cases here, the *main* device is biased in class-B near pinch-off, but now the *auxiliary* device is dynamically biased between deep class-C and optimal class-B.

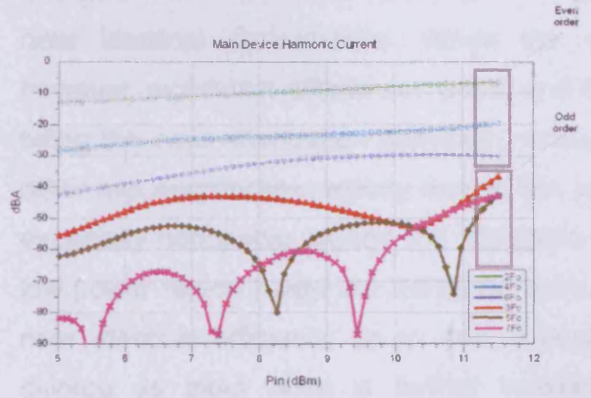


Figure-226 harmonic current behaviour of an adaptive-bias Doherty - Main device

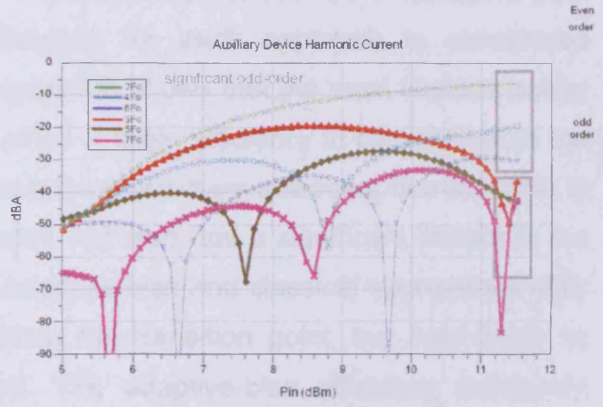


Figure-227 harmonic current behaviour of adaptive-bias Doherty - Auxiliary device

It is clear from these results that the input-attenuation Doherty offers the most favorable harmonic behaviour, with the lowest level of odd order harmonic generation. The other two approaches result in more complex behaviour and significant levels of both even and odd order harmonics, which is expected as the conduction angle of the *auxiliary* device is changing throughout the entire 6dB of the high power region of operation. The most significant observation can be made from the classical Doherty results presented in Figure-225, where although the second harmonic is dominant, the third harmonic is the second largest component throughout the entire 6dB of dynamic range. This situation is slightly different for the adaptive bias approach where the *auxiliary* device's third harmonic magnitude peaks at approximately PEP-3dB, before diminishing significantly as PEP is

approached, only to increase once more as compression occurs. This is shown in Figure-227.

The impact of harmonic behaviour on general Doherty performance

For the classical and adaptive-bias Doherty implementations discussed, it has been shown that significant odd-order harmonic current spectra will be generated by the *auxiliary* device. When compared to the *main* device which is typically biased in optimal class-B, this leads to harmonic behaviour which is generally quite complex and possibly difficult to remove. Although a simple, shorted ¼ wave line is effective in suppressing the significant even-order harmonics generated by both devices. Due to the unavoidable loading of the fundamental, the approach cannot easily be used in the same way to suppress odd-order harmonics. As a consequence, there are a number of questions that arise regarding the effect of unavoidable and significant odd-order harmonic current spectra. Specifically, how the behaviour of both devices is affected, and how this in turn impacts the device voltage and current waveforms and overall performance.

It is clear from *Figure-228* that in terms of gain and output power, all ideal topologies offer near identical performance. When the efficiency for each approach is considered however, significant differences arise, and Figure-229 shows that the most obvious outlier being the input-attenuation approach, which offers a lower efficiency in comparison to the other two approaches, mainly due to the presence of *auxiliary* quiescent current. This is especially noticeable around the transition point, but also has a significant impact in the low power region below the transition point. Adaptive-bias and classical approaches offer near identical efficiency up to and approaching the transition point, but then begin to diverge as input drive is further increased. The adaptive-bias efficiency eventually converges with that of the adaptive-bias approach at PEP, and this is no surprise as the bias conditions are identical at this drive level. The interesting observation from *Figure-229* is the classical Doherty efficiency shows an approximate 5% improvement over the adaptive-bias Doherty in the high-power region between PEP and PEP-6dB, and approximately 10% better than the input-attenuation Doherty throughout the entire dynamic range. Through further analysis, it will become clear that the enhanced efficiency offered by the classical approach is mainly due to the presence of odd-order harmonics and their influence in shaping the *main* device voltage waveform.

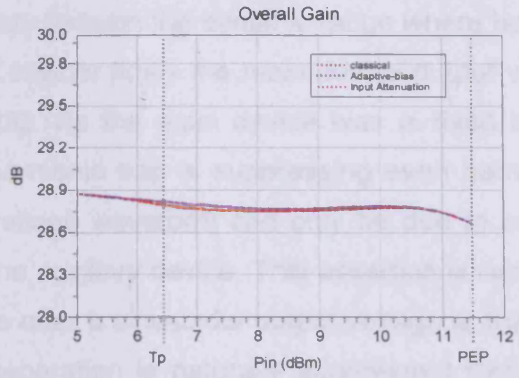


Figure-228 overall gain as a function of P_{in}

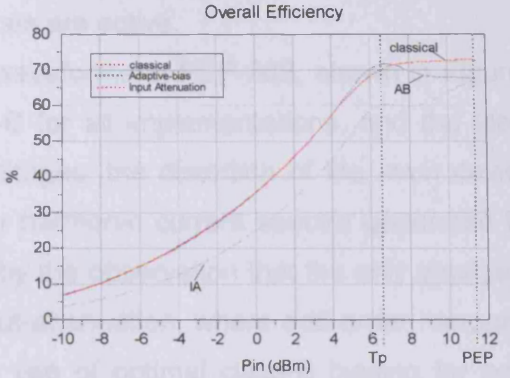


Figure-229 overall efficiency as a function of P_{in}

Linearity is another important performance metric and is probed here when using CW excitation by examining harmonic voltage developed in the load as a function of P_{in}, for the different approaches. *Figure-231* shows the suppressed even-order harmonics and the effectiveness of the capacitor-shorted λ/4 line. As expected, the magnitude of the odd-order harmonic power components are larger, but the remarkable observation from *Figure-230* is the similarity in terms of odd harmonic behaviour. This is especially so when considered in contrast to the large odd-order harmonic dissimilarity between approaches that is evident in *Figure-223 and Figure-226* earlier in this chapter.

Figure-230 odd-order spectral power at the load

Figure-231 even-order spectral power at the load

The impact of harmonic behaviour on voltage and current waveforms

So far in this chapter, harmonic analysis has been explored in terms of the frequency domain. It is constructive however to extend this analysis to include observations in the time domain. The following collection of graphs shows the time domain voltage and current waveforms for all three Doherty approaches. This is presented at two different

drive levels: Peak Envelope Power (PEP) and PEP-3dB which corresponds to a point mid-way through the dynamic range where both devices are active.

Consider firstly the *main* device output voltage waveforms at PEP-3dB, shown in Figure-232. As the main device bias is fixed in class-B for all implementations, and the ideal harmonic trap is suppressing even harmonic voltages, the distortion of the *main* device voltage waveform can only be due to odd-order harmonic current spectra generated by the *auxiliary* device. This assertion is reinforced by the observation that the only approach to offer a sinusoidal output voltage is that of input-attenuation, where odd-order harmonic generation is naturally suppressed through the use of optimal class-B biasing for both devices.

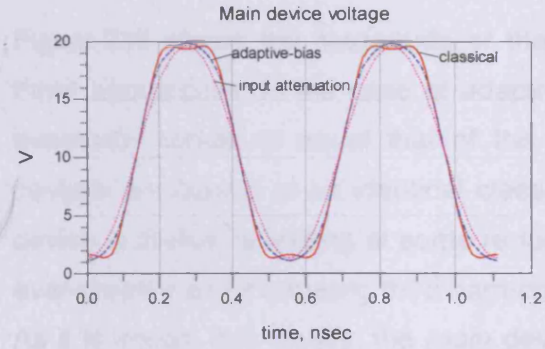


Figure-232 output voltage waveforms - main device

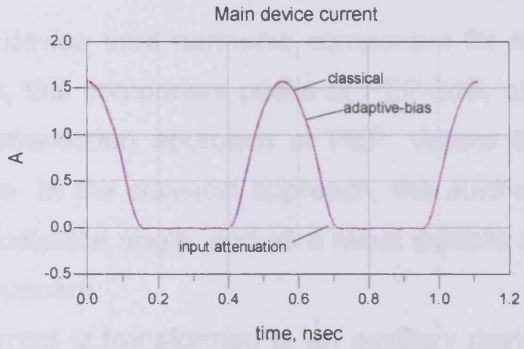


Figure-233 0utput current waveforms - main device

As long as the device model used is ideally trans-conductive, the current spectra will be insensitive to harmonic impedance. This explains why the *main* device current waveforms presented in Figure-233 take-on an identical, classical class-B profile for all Doherty approaches. These waveforms already tell us something about the expected Doherty performance, as it is the *main* device current that is transformed to a voltage at the load. In other words, a well behaved, linear current at the output of the *main* device will ideally lead to a well behaved, linear voltage at the load.

Turning attention to the *auxiliary* device, from Figure-234 it can be seen that the current waveforms are different for each approach, both in terms of conduction angle and peak amplitude. Figure-235 shows the *auxiliary* output voltage for all approaches, and for both drive conditions of PEP and PEP-3dB. From this plot it is clear that the output voltage waveforms are nearly identical for all implementations, for both power levels.

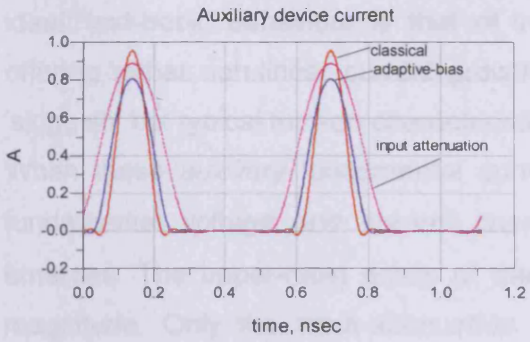


Figure-234 output current waveforms - auxiliary device

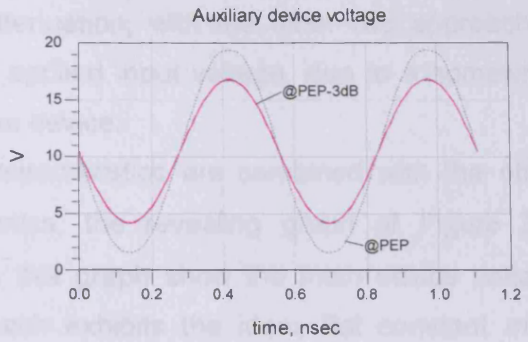


Figure-235 output voltage waveforms - auxiliary device (at PEP and PEP-3dB)

Figure-236 shows the magnitude of the *main* device third harmonic component for the three approaches. In the case of adaptive-bias, this component peaks at PEP-3dB, and eventually comes to equal that of the input-attenuation approach at PEP, Where the devices are biased in an identical class-B state. In the classical approach, the *auxiliary* device is always operating at some reduced conduction angle, and as a result exhibits an ever-present and increasing third harmonic component.

As it is known that ideally; the *main* device current is transformed to an *auxiliary* device voltage, Figure-237 is particularly interesting and shows that a linear relationship exists between input voltage and output current, resulting in overall linear behaviour for all implementations.

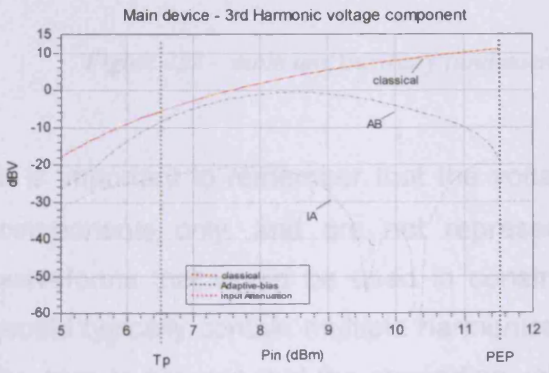


Figure-236 3rd harmonic voltage spectra as a function of P_{in} – main device

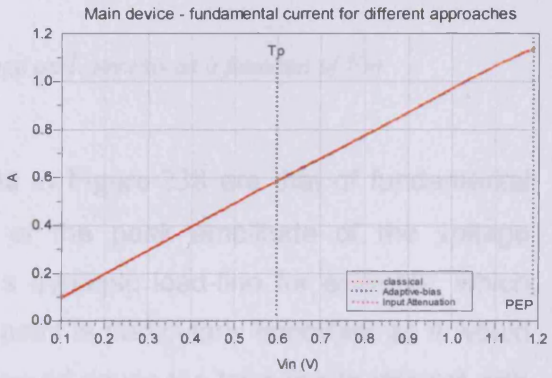


Figure-237 fundamental current component as a function of P_{in} – main device

It has been mentioned several times in this chapter how one of the basic requirements for Doherty behaviour is the correct control over fundamental *auxiliary* current growth, as illustrated earlier in Figure 12 and Figure 26. Figure-239 shows the fundamental current

magnitude as a function of input voltage for all approaches. The only approach to offer ideal 'text-book' behaviour is that of input-attenuation, with the other two approaches offering rather non-linear current growth with applied input voltage, due to a somewhat 'sluggish' but typical turn-on characteristic of the device.

When these *auxiliary* fundamental current characteristics are combined with the other fundamental voltage and current characteristics, the revealing graph of Figure 238 emerges. The upper-most group of traces in this graph show the *main* device voltage magnitude. Only the input-attenuation approach exhibits the ideal, flat constant *main* device voltage characteristic, with the other approaches showing an expansion followed by a compression, which is characteristic of when reduced conduction angle modes are used within the Doherty.

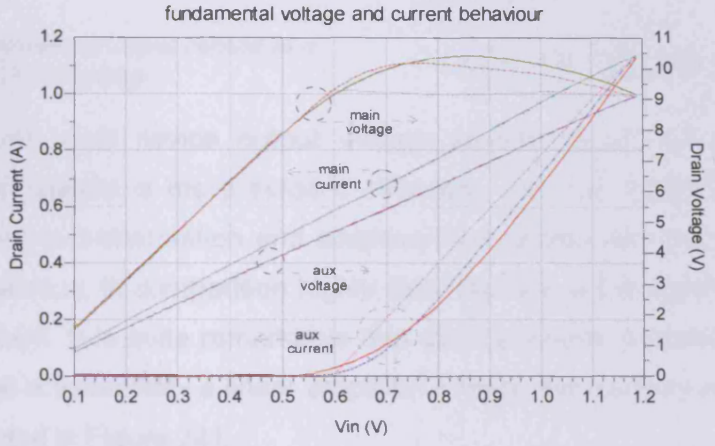


Figure 238 - main and auxiliary fundamental voltage and currents as a function of Vin

It is important to remember that the voltage plots in Figure 238 are that of fundamental components only, and are not representative of the peak amplitude of the voltage waveforms that would be used in constructing a dynamic load-line for example, which would typically contain multiple harmonics. This point is particularly important as it would be easy to assume that the expanding voltages would cause the load-line to interact with the knee-region. This is not the case however and the presence of significant third harmonic effectively 'pulls' the load-line away from the knee region. The expanding fundamental voltage is in fact the cause of the improved efficiency of the classical approach.

Figure 238 also shows how the *main* device fundamental current, and *auxiliary* device fundamental voltage are linear functions of input voltage, further illustrating the point that

the linearity of the Doherty is fundamentally a function of the linearity of the *main* device, and is much less a function of the linearity of the *auxiliary* device, which can be seen here to be highly non-linear in two of the three approaches.

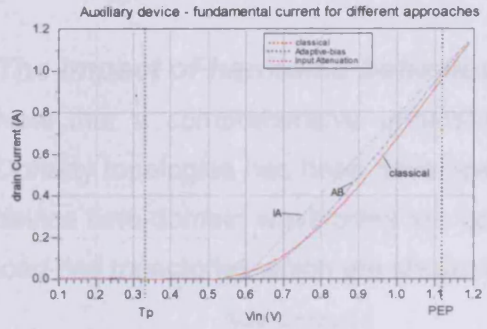


Figure-239 auxiliary fundamental output current as a function of input voltage

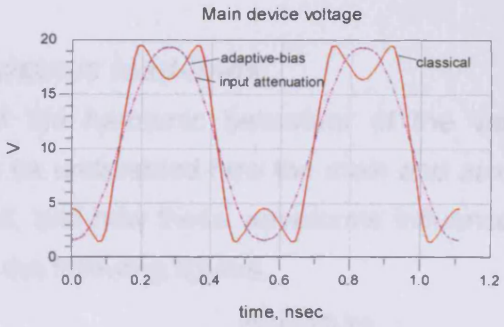


Figure-240 main device output voltage at PEP

Re-examining the *main* device output voltage waveforms at PEP, the impact of the *auxiliary* current spectra is more evident. Whereas the *main* device voltage waveforms produced by the input-attenuation and adaptive-bias approaches are near sinusoidal, the classical equivalent is, in comparison highly distorted due to the significant third harmonic voltage component. It is quite remarkable that such a heavily distorted voltage waveform can exist in what is essentially a linear amplifier. Finally, the *auxiliary* current waveforms at PEP are presented in Figure 241.

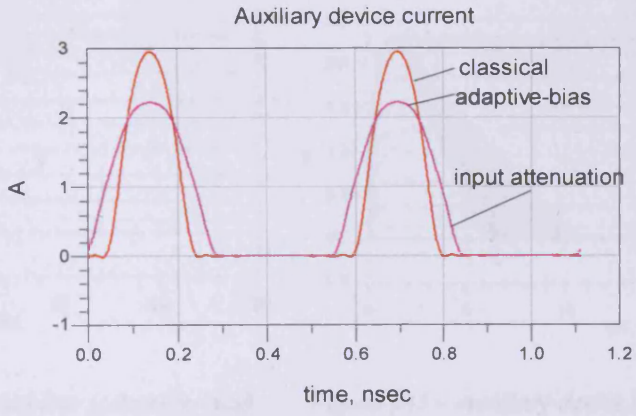


Figure 241 - auxiliary device output current at PEP

As expected, both the input-attenuation and adaptive-bias approaches produce identical waveforms, as they are biased identically at PEP, whilst the classical approach produces

a narrower but 'taller' current pulse. The important point is that all current waveforms contain the same fundamental energy at PEP. It is also important to note the additional *auxiliary* maximum current required by the classical approach, which in this case can be seen to be approximately 1.3 times that of the other approaches.

The impact of harmonic behaviour on dynamic load-lines

Now that a comprehensive understanding of the harmonic behaviour of the various Doherty topologies has been developed, it can be understood how the *main* and *auxiliary* device time-domain waveforms are constructed, and how these waveforms influence the load-line trajectories which are shown below in the following figures.

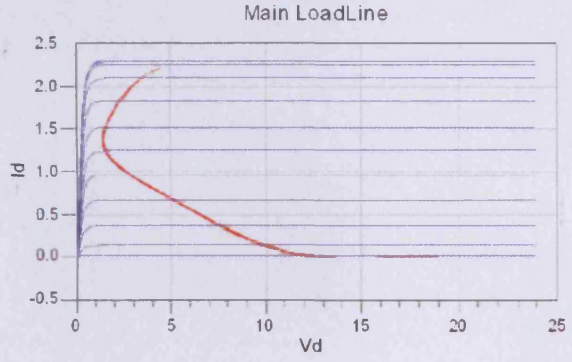


Figure 242 – main device load-line (classical)

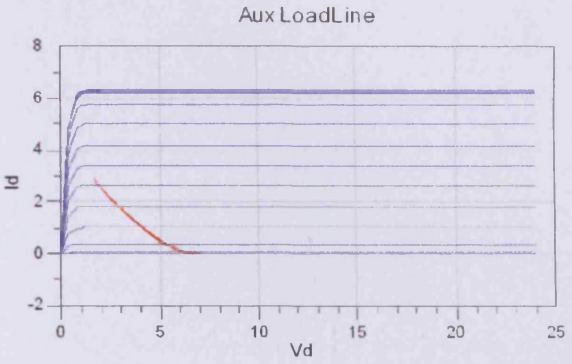


Figure 243 – auxiliary device load-line (classical)

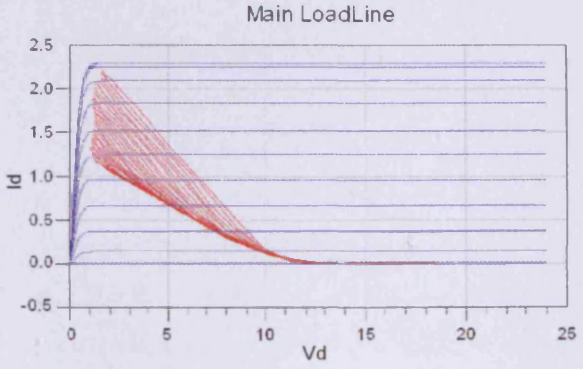


Figure 244 – main device load-line (adaptive-bias)

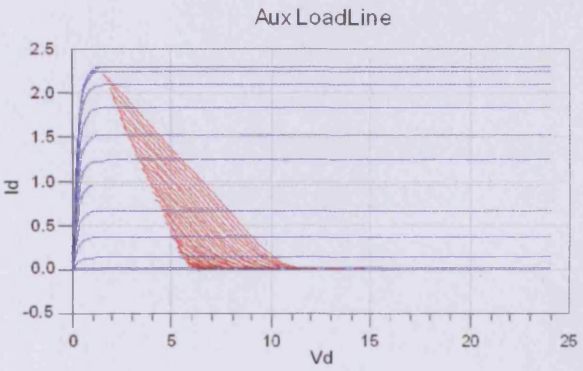


Figure 245 – auxiliary device load-line (adaptive-bias)

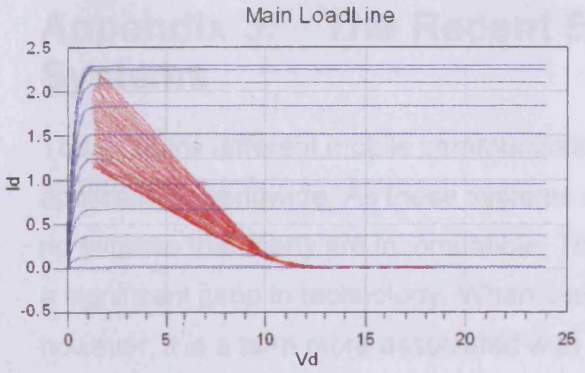


Figure 246 – main device load-line (input-attenuation)

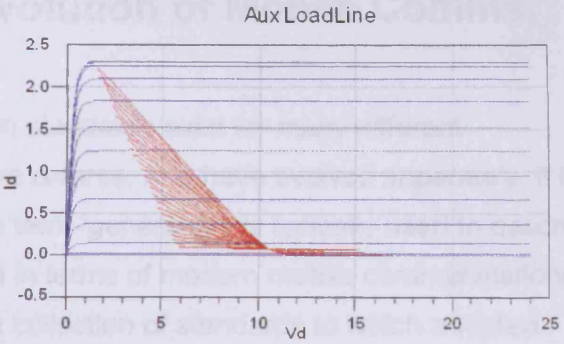
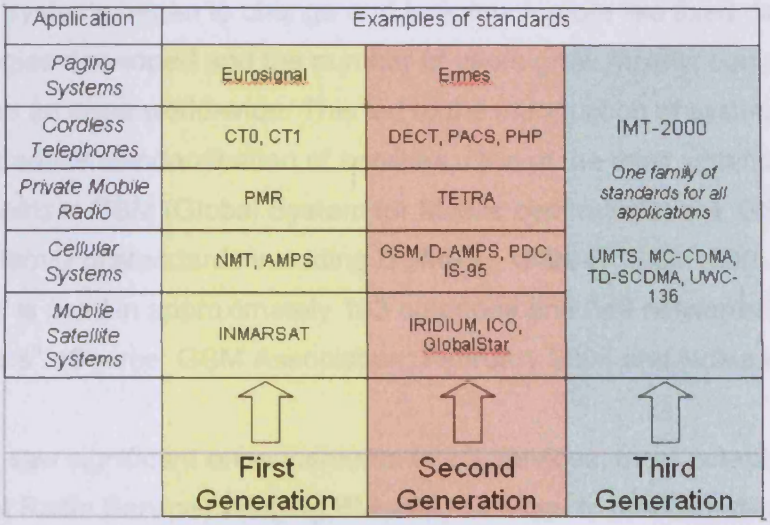


Figure 247 – auxiliary device load-line (input-attenuation)

Appendix 3. The Recent Evolution of Mobile Comms. Systems

Today, many different mobile communication standards exist for many different applications worldwide. As these systems are diverse, and have evolved separately, it is no surprise that many are incompatible. The term 'generation' is typically used to describe a significant jump in technology. When used in terms of modern mobile communications however, it is a term more associated with a collection of standards to which adopted systems must comply. GSM is a good example of such a standard within the second generation (2G) category.

The classification of standards is illustrated in fig nn below.



Pre - First generation

Mobile wireless based upon analogue communication systems have been around since the 1950s. The early 'pre-first' generation systems operated on a single channel basis where a single base station serviced an entire urban area. These systems had some major disadvantages including limited mobility, low capacity and poor speech quality. The equipment was heavy, bulky, expensive and prone to interference, with less than 1 million users were registered world-wide by the early 1980's.

First generation (1G)

Technology was improving rapidly, and single-point mobile communication systems were quickly being replaced with so called first generation (1G) cellular communication networks. This new approach, although still analogue allowed for significantly increased capacity and mobility, and coupled with smaller, lighter and more sophisticated handsets represented a technology that was much more attractive and accessible to the masses.

The most significant 1G systems world-wide were the UK based Total Access Communication System (TACS), Nordic Mobile Telephone (NMT) and the American Advanced Mobile Phone System (AMPS).

Second generation (2G)

The significant development of digital technologies over the latter part of the 1980's meant that radical improvements to analogue mobile communications systems were possible. The mass adoption of digital techniques allowed improvements in quality of service, system capacity and system coverage. Transmission and reception of digital media, e.g., fax, SMS and internet connection became a reality, and demand for such services began to grow rapidly. Digital techniques also allowed networks to be more secure due to encryption and other security features. Due to these evolutions, the topology of mobile communication systems began to change and look much more like fixed data networks. As the technologies developed and the number of users grew rapidly, compatibility of systems became an issue world-wide. This led to the introduction of systems that attempted to introduce standardisation of services. One of the most significant second generation systems is GSM (Global System for Mobile communication). GSM is better described as a family of standards including GSM900, GSM-R, GSM1800, GSM1900 and GSM400. "GSM is used in approximately 183 countries and 549 networks by nearly 1.5 billion subscribers". (Source: GSM Association, February 2004 and Nokia Horizons, Q3,2004).

The mid 1990's saw significant enhancements to 2G services, most notably GPRS (General Packet Radio Service) bringing IP-based services to mobile networks. GPRS provided higher throughput capacity, Internet-based content, and packet-based data services, enabling Internet browsing, email, powerful visual communications and multimedia messaging. GPRS has quickly become an established technology for delivering advanced data services over GSM networks worldwide.

Mid generation (2.5G)

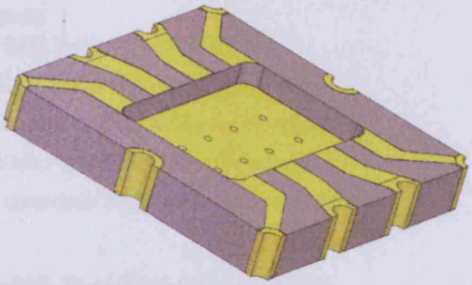
There are a number of so called mid-generation technologies sitting between 2G and 3G systems. These include EDGE and TETRA. EDGE (Enhanced Data Rates for Global Evolution) is built on the existing GSM/GPRS networkand on average triples the current GPRS data rates. TETRA (TErrestrial Trunked RAdio) is a purpose built technology that offers public safety and security organisations major advantages over conventional radio systems.

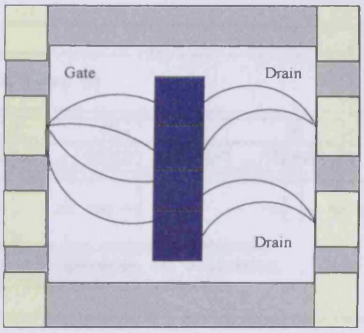
Third generation (3G)

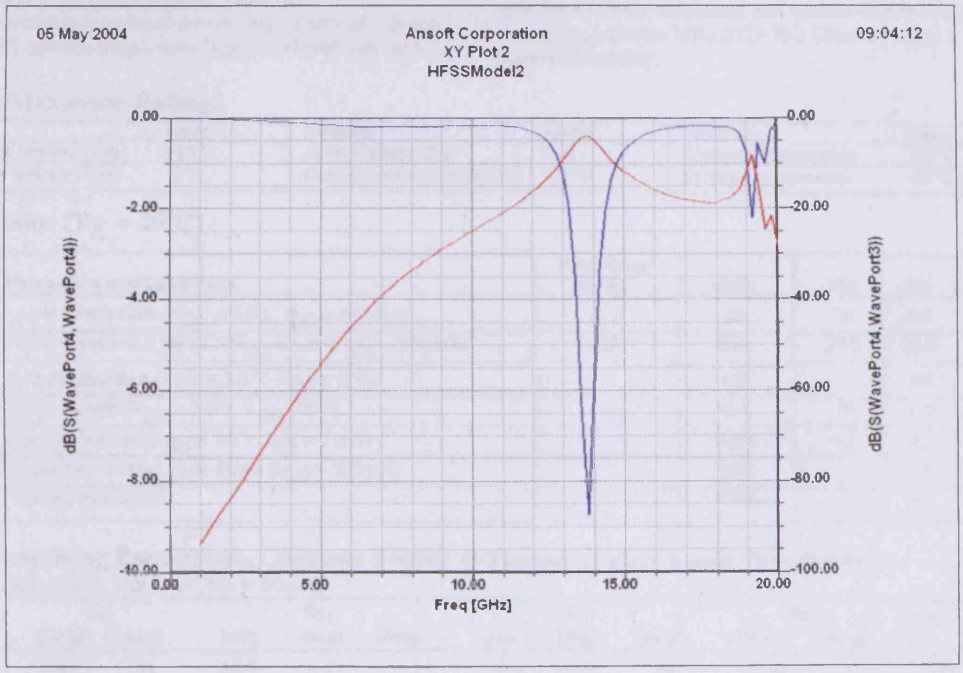
Third generation mobile communication systems are known collectively as IMT-2000. IMT-2000 is an internationally recognised collection of standards that apply to all mobile applications, offering high data rates up to 2MBit/s and high spectral efficiency. The most important IMT-2000 proposals are UMTS, otherwise known as W-CDMA, as the successor to GSM and CDMA-2000 as the successor to IS-95. In W-CDMA, user data is spread over a bandwidth of circa 5 MHz. The wide bandwidth supports high user data rates and also provides performance benefits due to frequency diversity.

Appendix 4. Device Data Sheets and Information

1. Celeritek F15-11 MESFET and LCC-8 chip carrier, bonding diagrams and data sheet







CELERITEK

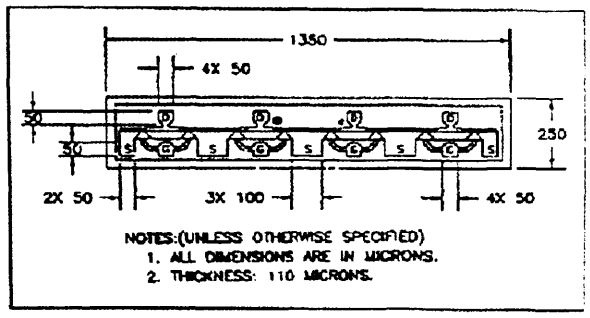
CF015-11

Product Specifications
December 1995 *(1 of 1)*

Broadband Power GaAs MESFET Chip

Features

- ❑ **P1dB Power: +26 dBm**
- ❑ **High Gain (@12 GHz): 8 dB**
- ❑ **Broadband: Usable to 18 GHz**
- ❑ **Wafer Qualification Procedure**
- ❑ **Customer Wafer Selection Available**



Celeritek Broadband Power Chip

Celeritek's CF015-11 Medium Power Chip is a GaAs MESFET device with a 1200 µm gate width, 1/4 micron gate length, Celeritek's proprietary Silicon Nitride passivation, and is fabricated on ion implanted wafers.

Celeritek's Wafer Qualification Procedure for this device consists of DC, RF and reliability testing of both individual die in 6 to 18 GHz amplifier modules.

Celeritek's broadband power chips make up a family of GaAs FET devices which have high broadband gain and provide up to 1 Watt in balanced 6 to 18 GHz amplifier circuits. These devices are also suitable for high power oscillators. In narrow band applications they offer superior associated gain.

These devices are available in chip form and are suitable for airborne, shipboard and ground-based equipment. Screening includes MIL-STD-750 Class B, Class S and commercial screening.

Absolute Maximum Ratings

Parameter	Rating	Parameter	Rating	Parameter	Rating
Drain-Source Voltage (Vds)	+10 V	Drain Current (Ids)	Idss	Channel Temperature	175°C
Gate-Source Voltage (Vgs)	-5 V	Continious Dissipation (Pt)	3.0 W	Storage Temperature	-65°C to +150°C

Specifications (T_A = 25°C)

Symbol	Parameters and Conditions	Frequency (GHz)	Units	Min	Typ	Max
G_L	Linear Power Gain (V_{DS} = 6.0 V, I_{DS} = 160 mA)	12.0	dB	7.0	8.0	
P_{1dB}	Power Output @ 1 dB GC (V_{DS} = 6.0 V, I_{DS} = 160 mA)	12.0	dBm	25.0	26.0	
g_m	Transconductance (V_{DS} = 3.0 V, V_{GS} = 0 V)		mS		240	
I_{DSS}	Drain Current (V_{DS} = 3.0 V, V_{GS} = 0 V)		mA	180	310	380
V_P	Pinchoff Voltage (V_{DS} = 3.0 V, I_{DS} = 1 mA)		Volts	-1.2	-2.1	-3.0
BV_{GD}	Breakdown Voltage, Gate-Drain (I_{GD} = 200 µA)		Volts	-12	-18	
R_{th}	Thermal Resistance		°C/W		40	

Typical Scattering Parameters, Common Source (S-Parameters Include Bonding Wire Parasitics)

CF015-11 (TA = 25°C, Vds = 6V, Ids = 80mA)

Frequency	S_{11}		S_{21}			S_{12}			S_{22}		K	MSG
(GHz)	(Mag)	(Ang)	(dB)	(Mag)	(Ang)	(dB)	(Mag)	(Ang)	(Mag)	(Ang)		(dB)
2.0	0.91	-93	16.5	6.67	123	-25.9	0.05	44	0.26	-131	0.21	21.2
4.0	0.86	-136	12.5	4.19	96	-24.1	0.06	28	0.34	-148	0.37	18.3
6.0	0.83	-157	9.4	2.95	78	-23.8	0.06	20	0.41	-155	0.54	16.6
8.0	0.82	-171	7.0	2.24	66	-24.3	0.06	18	0.43	-156	0.82	15.7
10.0	0.84	179	5.1	1.80	56	-24.8	0.06	20	0.45	-154	0.97	14.9
12.0	0.85	171	3.5	1.49	46	-25.1	0.06	22	0.48	-154	1.03	14.2
14.0	0.86	164	2.0	1.26	36	-24.9	0.06	21	0.52	-157	1.11	13.5
16.0	0.87	157	0.7	1.09	26	-25.1	0.06	19	0.54	-161	1.07	12.9
18.0	0.89	150	-0.4	0.96	16	-24.5	0.06	13	0.57	-169	0.95	12.1

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Appendix 5. Extending the Doherty's Dynamic Range

One of the defining properties of the classical Doherty is a 6dB dynamic range that extends between PEP and the transition point. Modern communication systems posess peak-to-average power ratios typically extend over 10 dB however, and this results in a problem: the Doherty's high efficiency plateau does not capture the majority of the dynamics of the modulation envelope. In other words, the region of high efficiency exists where the modulation envelope spends relatively little of its time. It is clear then that for the Doherty to be effective in its role of efficiency enhancement, the dynamics of the modulation envelope need to be largely contained by the Doherty's efficiency plateau.

In order to extend the dynamic range of the Doherty, it is necessary to arrange for the main device to achieve its maximum voltage, high-efficiency state 'earlier' in the dynamic range, at a reduced input drive power. Consequentially, the auxiliary device needs to conduct at a transition point that exists at a lower input drive level. This can be done by simply adjusting the characteristic impedance of the main combining transformer such that the usual, classical load of $R_{opt}/2$ is transformed to something higher than $2R_{opt}$ at the output of the main device. Although the role of the auxiliary device is unchanged: *to prevent the main device load-line from expanding into the knee region*, the auxiliary current necessary to bring this effect about is very different to that of the classical case.

The extended or asymmetric Doherty arrangement is discussed at length in [9] where it is clear that the advantage of extended dynamic range is limited due to the fact that the characteristic efficiency 'dip' between the transition point and PEP deepens with increasing dynamic range. The approach is still a very important aspect of Doherty operation however, and is further discussed here for completeness.

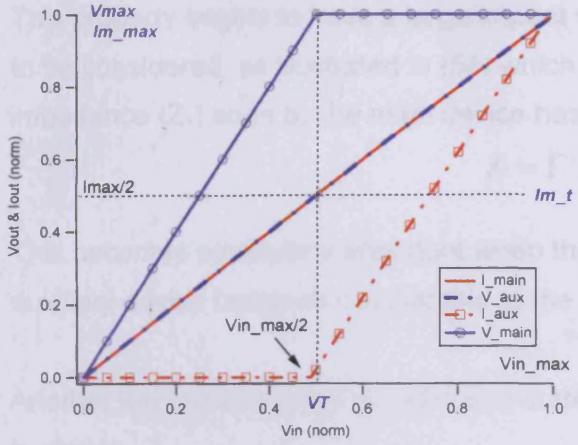

Figure 248 – Ideal Doherty characteristics (classical)

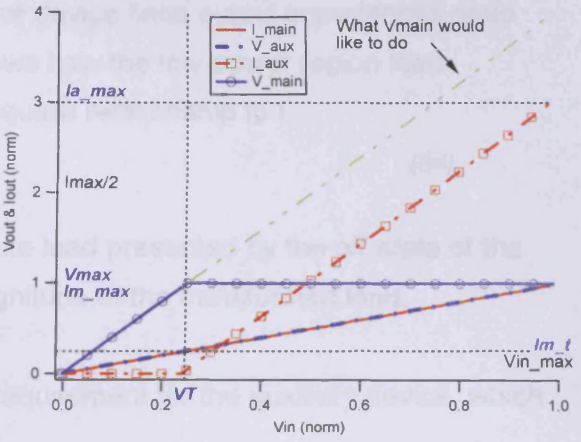

Figure 249 – Ideal Doherty characteristics (asymmetrical)

This analysis begins by defining a parameter Γ that describes the dynamic range of the Doherty.

$$\Gamma = \frac{\text{Vin\_max}}{\text{VT}} \quad \text{or} \quad \Gamma = \frac{\text{Im\_max}}{\text{Im\_t}} \tag{49}$$

Whereas Γ is usually defined in terms of input voltage, there is a good reason to describe it in terms output current (which is the same for an ideally trans-conductive device) as it allows concise definition of the auxiliary device current.

$$Iaux = \begin{cases} 0, \text{I\_main} < \text{Im\_t} \\ \Gamma(\text{I\_main} - \text{Im\_t}), \text{I\_main} \geq \text{Im\_t} \end{cases} \tag{50}$$

In other words, below the transition point there is no auxiliary fundamental current. Above the transition point however, the auxiliary current needs to expand from zero to Im_max at a rate proportional to Γ. In the classical Doherty, Γ =2.

The scaling factor Γ can be used to define key parameters:

$$Dynamic\ Range\ (DR) = 20\log(\Gamma) \tag{51}$$

$$\Gamma = 10^{\left(\frac{DR}{20}\right)} \tag{52}$$

In terms of circuit design, the characteristic impedance of the main combining transformer and the required load are also linked to the scaling factor, such that

$$R_L = R_{OPT}/\Gamma \quad \text{and} \quad Z_T = \Gamma R_L \tag{53}$$

This property begins to have a large impact where device finite output impedances need to be considered, as illustrated in (54) which shows how the low-power region load impedance (Z_1) seen by the main device has a square relationship to Γ.

$$Z_1 = \Gamma^2 R_L \qquad (54)$$

This becomes particularly important when the finite load presented by the off-state of the auxiliary device becomes comparable to the magnitude of the transformed load.

Another key parameter is the maximum current requirement for the auxiliary device, which is simply:

$$Iaux\_max = (\Gamma - 1) I\_main\_max \qquad (55)$$

The other way to understand what is going on in the asymmetrical Doherty is to consider Figure 249 and what the auxiliary current is 'trying' to do. If the main device saturates early in the dynamic range, we can think of it as 'trying' to achieve higher voltages than are possible. The role of the auxiliary device can similarly be considered as to counteract this expanding voltage, limiting it to Vmax. Thus Iaux rises in tandem with and parallel to the notional trace of unrestricted Vmain (green trace in Figure 249)

Consider the example case where Γ=4.
The dynamic range DR=20log(4)=12 dB
The impedance of the main combining transformer is $Z_T = \Gamma R_L = 4(R_{opt}/2) = 2R_{opt}$.
The low-power impedance seen by main is $Z_1 = \Gamma^2 R_L = 16R_L = 8R_{opt}$
Iaux_max = (Γ-1)Imax_main = 3Imax_main.

Appendix 6. Three-tone modulation calculations

In terms of classical Double Side-Band Amplitude Modulation, the modulation index (Index) is given as:

$$\text{Index} = \frac{V_{fm}}{V_{fc}} \tag{56}$$

Spectrally, these components mix to give voltage spectra located at Fc, Fc-Fm and Fc+Fm. The magnitude of the modulation component can be expressed as:

$$V_{fm} = \text{Index} \cdot V_{fc} \tag{57}$$

The peak envelope voltage occurs when modulation and carrier components add in phase, and is given by:

$$V_{pep} = V_{fm} + V_{fc} \tag{58}$$

Substituting from *(57*:

$$V_{pep} = \left[\text{Index} \cdot Vfc\right]_{+} V_{fc} \tag{59}$$

$$V_{pep} = V_{fc}\left[1 + \text{Index}\right] \tag{60}$$

So,

$$V_{fc} = \frac{V_{pep}}{1 + \text{Index}} \tag{61}$$

Normalising to PEP

$$V_{fc} = \left[\frac{1}{1 + \text{Index}}\right] \quad \text{and } V_{usb}=V_{lsb}=\frac{V_{pep} - V_{fc}}{2} \tag{62}$$

And

$$V_{usb} = \frac{1}{2}\left[1 - V_{fc}\right] \quad \text{or } V_{usb} = \frac{1}{2}\left[1 - \frac{1}{\text{Index}}\right] \tag{63}$$

Appendix 7. Relevant Publications

First author papers directly relevant to this thesis and included in this appendix.

1. **The Design of a GaN Doherty Amplifier using Waveform Measurements and Active Harmonic Load-Pull**
   *Published - **INMMiC-2006, Aveiro, Portugal, Jan 2006***
   ***Jonathan Lees**, Aamir Sheikh, Johannes Benedikt and Paul J. Tasker*

2. **An Experimental Gallium Nitride Microwave Doherty Amplifier**
   *Published - **IET Electronics Letters, Dec 2005***
   ***Jonathan Lees**, Johannes Benedikt, Keith P Hilton, Jeff Powell, Richard S Balmer, Michael J Uren, Trevor Martin and Paul J. Tasker*

3. **Characterisation of an Experimental Gallium Nitride Microwave Doherty Amplifier**
   *Published - **EuMC, Paris, Oct 2005***
   ***Jonathan Lees**, Johannes Benedikt, Keith P Hilton, Jeff Powell, Richard S Balmer, Michael J Uren, Trevor Martin and Paul J. Tasker*

4. **An Automated Multiple-stimulus Measurement system for Characterising Multiple-Device Amplifiers**
   *Published - **EuMC, Amsterdam, Oct 2004***
   ***Jonathan Lees**, A. Haczewski, Johannes Benedikt and Paul J. Tasker*

5. **Single-Tone Optimisation of an Adaptive-Bias Doherty Structure**
   *Published – **MTT-S, Philadelphia, June 2003***
   ***Jonathan Lees**, Martin Goss, Johannes Benedikt and Paul J. Tasker*

6. **Comparison of Load-Pull Measurement Results of a 4W pHEMT Involving Five European Laboratories**
   *Published - **EuMC, Paris, Oct 2005***
   ***Jonathan Lees**, Johannes Benedikt, Bernd Bunz, Christophe Gaquiere, Damien Ducatteau, E. Marquez-Segura, T.M. Martin-Guerrero, Alain Barel*

Joint authorship papers that are not included in this appendix.

7. **High Power Active Harmonic Load-Pull System for Characterization of High Power 100Watt Transistors**
   *Z. Aboush, C. Jones, G. Knight, A. Sheikh, H. Lee, **J. Lees**, J. Benedikt and P. J. Tasker*
   Published - EuMC, Paris, Oct 2005

8. **Active Harmonic Load-Pull System for Characterizing Highly Mismatched High Power Transistors**
   Published -
   *Zaid Aboush, **Jonathan Lees**, Johannes Benedikt and Paul Tasker*