Integration of InP and InGaAs on 300mm Si wafers using chemical mechanical planarization

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Abstract

Integration of III-V high mobility channel materials in complementary metal oxide semiconductors (CMOS) and III-V photonic materials for integrated light sources on Si substrates requires low defect density III-V buffer layers in order to enable epitaxial growth of high crystal quality active layers. For the fabrication of $In_{0.53}Ga_{0.47}As$ n-channel MOSFET on Si, a lattice matched InP buffer layer is one of the most effective approaches when used in combination with the aspect ratio trapping technique, an integration method known for reducing the density of defects formed during relaxation of strain induced by the lattice mismatch between InP and Si. The InP buffer should be planarized in order to improve thickness uniformity and roughness before subsequent deposition of active layers. In this work we discuss the development of InP planarization on 300mm Si wafers and investigate slurry composition effects on the final oxide loss and condition of the InP surface. To further explore viability of this approach we deposited an epitaxial $In_{0.53}Ga_{0.47}As$ n-MOS channel layer on top of the planarized InP buffer.

Introduction

III-V high mobility channel materials are attractive potential candidates for continuing voltage scaling in advanced complementary metal oxide semiconductor (CMOS) devices. Amongst them, $In_{53\%}Ga_{47\%}As$ has been extensively studied due to its high electron mobility and injection velocity compared to Si.[1,2] Historically, the 53% In content has been selected to match the lattice constant of InP substrates, hence minimizing crystallographic defect density in the InGaAs channel. However, in order to grow $In_{53}Ga_{47}As$ on Si, a large 8% lattice mismatch between film and substrate has to be taken into account. The development of an integration approach that enables the deposition of low defect density III-V channel layers on Si is one of the biggest challenges to overcome. The blanket deposition of III-V layers directly on silicon typically results in a high density of defects. The annihilation of defects through the use of thick strain relaxed buffer layers has limited usefulness due to thickness

constrains imposed by thermal expansion coefficient mismatch, material cost and process throughput considerations. To overcome the large lattice mismatch a novel methodology for forming a "virtual" substrate by exploiting SiGe buffer approach has been proposed to achieve high quality III-V on Si blanket films.[3]

Other strategies have been reported in the literature, such as the use of a low temperature nucleation layer to grow a GaAs/InP buffer heterostructure directly on Si,[4] or the use of the aspect ratio trapping approach (ART).[5] The aspect ratio trapping (ART) technique utilizes patterned oxide templates on Si substrates to grow III-V materials inside isolated trenches, allowing confining defects at their bottom, and reduces the limitation on the overall buffer layer thickness. For the fabrication of $In_{0.53}Ga_{0.47}As$ n-channel MOSFET on Si, a lattice matched InP buffer layer is one of the most effective approaches when used in combination with the aspect ratio trapping technique.

The deposition of InP in the patterned oxide template normally creates a non-uniform thickness distribution as the growth rate is affected by the presence of defects in the growing film. Moreover, {111} facet formation has been frequently reported.[6] As a consequence, sub-nanometer roughness and thickness control cannot be achieved. The InP buffer should thus be planarized in order to improve thickness uniformity and roughness before subsequent deposition of the active layers. One of the possible solutions is to implement an intermediate III-V buffer planarization step.[7,8,9] Buffer planarization can be followed by the in-situ pre-clean, including optional InP recess integrated with barrier and channel layer regrowth to yield high-mobility channels in the shape of a fin suitable for transistor fabrication.

Experimental

When growing InP directly on Si to support the growth of an $In_{53\%}Ga_{47\%}As$ channel, strong 3D nucleation due to strain relaxation is observed. Whenever InP 3D islands coalesce, stacking faults and twin boundaries form at the merging fronts contributing to an increase in the roughness of the heteroepitaxial layer. In order to control the roughness and the crystal quality of the deposited film, two main strategies are usually adopted: a very low temperature (< 425˚C) deposition of a nucleation layer to inhibit In diffusion and promote the formation of a high density of small islands, and the use of {111} Si surfaces to prevent the formation of anti-phase boundaries (APB)[10] and minimize threading dislocations due to an unusual relaxation mechanism based on the formation of twins and stacking faults parallel to the InP/Si (111) interface.[11] In this development we adopted both strategies within the ART approach to deposit InP directly on 300mm exact Si (001) substrates and achieve complete trench filling. This enabled the development of an InP CMP process that allowed the subsequent growth of an $In_{53\%}Ga_{47\%}As$ channel.

An AIXTRON CRIUS-R MOCVD system was used to grow InP films on patterned 300mm on-axis Si (001) wafers. SEMI-standard 300mm wafers with (001) silicon surfaces were used to fabricate experimental test structures for III-V epitaxial deposition. These structures were created on Si substrates by forming a 180 nm thick thermal SiO_2 layer followed by lithography and dry etching of trenches in the oxide in the [110] direction. 65 nm wide trenches were opened in the oxide and spaced at 130 nm pitch. The oxide etch step

created a 15 nm deep over-etch into the Si, with approximately 6 nm thick residual oxide left at the bottom of Si (001) trench while lateral {110} Si surfaces had significantly less residual oxide on them, as discussed previously.[6] The dimension of the trenches along the [110] direction was 25.4 mm.

Prior to deposition of InP, the oxide at the bottom of the trenches was removed by using a vapor HF/NH_3 process,[12,13] targeted to etch 2 to 3 nm of silicon dioxide, leaving the (001) surface at the trench bottom covered with a few nm of SiO_2, to prevent InP nucleation on that (001) surface, as explained in detail in [6]. However, the sidewalls of the bottom of the trench recessed into Si became oxide free during this process and exposed {111} facets during the bake step prior to the nucleation of InP. The formation of {111} facets can be explained as follows: the bake is conducted at high temperature (> 800 °C) for few minutes in pure H_2 ambient to remove the hydrogen passivation layer and any residual native oxide. During this bake step a thermal etch of the trench bottom {110} planes occurs at a significantly faster rate compared to {111} planes, resulting in exposing {111} Si facets that slightly undercut the SiO_2 sidewalls as shown in Figure 1. This faster etch rate could be explained by the lower surface energy associated with the formation of {111} planes. The rest of the trench bottom still has the (001) surface covered with a thin layer of oxide which prevents InP nucleation.

For the growth of InP films, trimethylindium (TMIn) was used as the group-III precursor, and tertiarybutylphosphine (TBP) and phosphine (PH_3) were used as the group V precursors. The growth was carried out at low pressure and the temperature was measured with a multi-channel pyrometer, allowing real-time surface temperature profile monitoring. After the high temperature bake step completed, the surface of the wafer was saturated with arsenic in order to provide charge neutrality along the interface and promote the growth of single domain InP film.[14] The saturation with arsenic was achieved by introducing tertiarybutylarsenic (TBA) in the reactor at a temperature below 500°C, immediately preceding the InP nucleation step. A highly inert arsenic passivation layer forms on the silicon {111} surface as the result of arsenic atoms adsorption and is limited to single monolayer coverage.[14]

A two-step growth approach was also implemented, in which the first step aims at depositing an InP seed layer at low temperature (below 425 °C) using TBP with a V/III ratio of 25, and the second step is needed to bulk fill the oxide trenches with InP at 600 °C and with a V/III ratio of 100 by utilizing PH_3 precursor.

Planarization of deposited InP buffer layer was performed on a 300mm AMAT Reflexion CMP tool. The slurry formulation was optimized for pH level and abrasive solids' concentration to evaluate process window, removal rate and selectivity to silicon oxide. In the first two iterations removal rates were evaluated using blanket InP wafers for an approximate process window, and then the effect of pH was studied on the patterned ART InP wafers before the final fine tuning experiment was conducted. It was found in the initial iteration that the removal rate was highly dependent on the pH of the slurry formulation and a fairly narrow range of pH value in the range between 2.3 and 3.0 was identified where the removal rate could be finely controlled. At pH levels above 3.0 the removal rate was reduced to almost zero and below 2.3 the removal rate increased rapidly but a large amount of phosphine gas

was detected prohibiting operating in this regime due to safety considerations.

Results

InP Buffer Growth

Figure 2a shows a top down view of the InP fins grown on Si. The overall filling of the trenches is good but several pits and thickness non-uniformities are visible in most trenches. The formation of pits on GaAs on Si fins has been previously associated with a high density of nanotwins propagating and kinking along the trench direction.[6] Twinned planes have been frequently observed on InP fins in cross sectional TEM micrographs along [110], as shown in Figure 2b. Twin plane formation can be either the consequence of InP islands merging during the nucleation step or can be caused by thickness non-uniformities of the thin oxide layer at the trench bottom.[6] The dark band at the trench bottom in Figure 2b is caused by the superposition of InP and Si crystal lattices in the trench recess, which generates two dimensional translational Moiré fringes; dark meandering lines in the lower half of the fin are threading dislocations annihilating on the oxide walls.

The cross sectional SEM image of the InP layer in Figure 3a reveals that III-V fins, when they grow outside the trenches, have a 54.7˚ tilt towards $[1\bar{1}0]$ or $[\bar{1}10]$. When two adjacent fins have opposite tilt angles coalescence occurs as observed in several trenches in Figure 2a. The cross sectional TEM image of InP fins in Figure 3b shows several twinned lamellas nucleating at the SiO_2 sidewalls and propagating in the InP layer; some end up being trapped at the opposite sidewall while others propagate outside the trenches. At these process conditions InP grows exposing {111} facets. Twin boundaries form on {111} planes which have a 54.7˚ angle with (001). When a twin boundary forms, the growth rate perpendicular to the boundary plane drops, causing the fin to tilt in the opposite direction where the growth rate is higher. It is not clear yet why the formation of twinned lamellas in the upper part of the oxide sidewalls seems to be specific to InP and has not been observed on GaAs on Si fins.[6]

In order to prevent InP tilting outside the trenches, we reduced the InP growth time and targeted a filling of only 2/3 of the trenches. We then switched precursors and continued to grow InGaAs on top of the InP buffer, to evaluate the crystal quality and the morphology of the channel material without the planarization step. InGaAs was grown at 600^0C using trimethylindium (TMIn) and trimethylgallium (TMGa) as the group-III precursor, and arsine (AsH_3) as the group V precursor. Despite the good trench filling achieved, as shown in Figure 4a, most of the InGaAs fins still show the 54.7˚ tilt towards $[1\bar{1}0]$ or $[\bar{1}10]$ when growing outside the trenches (Figure 4b), suggesting the formation of nanotwins at the oxide sidewalls.

The cross sectional STEM image reported in Figure 4b shows the interface between InP and InGaAs. InP grows inside the trenches exposing mainly {111} facets; the driving force for facet formation is believed to be the minimization of the oxide sidewall/III-V fin interfacial energy, which is achieved with the intrinsic reduction in contact area that occurs when {111} facets form.[15] The In content of the InGaAs layer was designed to be 53%. The Ga EDS map of the III-V fin structure reported in Figure 4c shows that InGaAs stoichiometry is not uniform and phase separation occurs. Considering that InGaAs grows exposing {111}

facets, an Indium content increase (or Gallium content decrease) is observed in correspondence of {111} InGaAs facets: Indium likely diffuses away from low angle planes like {113} {115} or (001) and accumulates on {111} facets. In order to confirm that the presence of {111} facets on the InP buffer promotes phase separation on the InGaAs layer we introduced a CMP step after the InP growth to planarize its surface and improve the control of the InGaAs channel stoichiometry. Moreover, the planarization step would allow a better control of the active layer thickness, which remains a significant challenge within the direct growth of InGaAs on the partial InP buffer layer when merged into one epitaxial step. In order to reduce void density to a level where it is sound for manufacturing, a significant InP overgrown thickness of more than 100 nm was required before the intermediate InP planarization step to address closing all the gaps in the fill. The overburden created as a result of this approach was removed by the CMP step leaving the trenches completely filled with InP.

InP Chemical Mechanical Planarization

The fine tuning of the InP CMP process was completed for the slurry formulation with pH levels in the range between 2.3 and 3.0. The concentration of solids was tuned in the range between 0.1% and 0.5%. Particle sizes were in the range of 35 - 120 nm. Most of the slurries which were tested incorporated particles within a range of 40-70 nm in size. A 5-point design of experiments was completed using these parameters at 60 second polishing times and a center point polished at 60 and 90 seconds (Figure 5). Hydrogen peroxide concentration was kept constant for all points at 0.5%. PH level was adjusted with either HNO_3 or KOH after all chemicals and particle suspensions were combined. In those cases where addition of the particle suspension to the mixed chemicals would cause for a pH change into a range where colloidal instability might manifest, an intermediate pH adjustment was performed, prior to the addition of the particle suspension.

InP polishing was performed on full 300mm wafers with the goal of removing all of the InP overburden and stopping on the silicon oxide template with the maximum oxide thickness loss limited to less than 10 nm. A single wafer was used for each point in the design of experiments and wafers were cross-sectioned in order to collect tilt and cross-SEM images from the center of each wafer. The results of the physical analysis are shown in Figures 6 and 7.

The optimal performance was achieved at 60 second polish with 0.5% solids and a pH of 2.3 which produced 2.3 nm root mean square roughness as measured by AFM. A similar result was observed with a 90 second polish time at 0.3% solids and a pH of 2.65 and an AFM root mean square roughness of 2.4 nm. The estimated oxide loss was 9 nm for 60 second polish time and close to 10 nm for 90 second polish time wafer. The optimal process window was defined for slurry with pH in the range between 2.3 and 2.65, solids composition in the range between 0.3% and 0.5% and polishing time between 60 and 90 seconds. Additional components in the slurry for topography and corrosion control as well as overpolish extension are not disclosed.

An additional wafer was produced for continuing InGaAs regrowth experiment using the

parameters established as yielding optimal results in the fine tuning InP CMP experiment.

InGaAs channel regrowth demonstration

After the CMP step, the wafer was reintroduced into the MOCVD reactor and baked at 550 ˚C to remove the native oxide that formed on top of the InP buffer; a thin 20 nm $In_{53\%}Ga_{47\%}As$ channel was then regrown on top of it, using the same process conditions that produced phase separation on the previous sample. Figure 8a shows a top down SEM image of the InGaAs channel; pits that formed during the deposition of the InP buffer are still present. The inset in Figure 8a, as well as the cross sectional TEM micrographs of Figure 8b and Figure 8c show that the InGaAs channel retraces the curved morphology of the underlying InP buffer: small {111} facets are present together with a large (001) surface. The distance between InGaAs and InP (001) planes is 20 nm. The high resolution TEM micrograph in Figure 9 shows a sharp interface between the two layers. No phase separation is observed in these layers, confirming that the issue is likely related to the presence of {111} facets in the underlying InP buffer, a phenomenon that is currently under investigation. However, the asymmetric InGaAs fin shape shown in the inset of Figure 8a suggests that twin defects nucleating on the upper part of the oxide sidewalls propagate into the InGaAs channel as well.

Summary

In this work we have demonstrated the integration of an InP buffer on 300mm wafer size silicon substrates utilizing chemical mechanical planarization and aspect ratio trapping technique. The planarization process was investigated to determine the removal rate, overpolish and residual roughness as a function of the slurry pH and solids' concentration. An optimized process, showing good stopping capability on the oxide template and low dishing of the oxide layer after the complete removal of InP buffer overburden, was established. The developed process is considered to be essential for integrating InP buffer materials on the silicon substrate as it was shown that the typical roughness of the as-grown InP layer, if used alone without the planarization step, is too high in order to fabricate uniform high mobility n-MOS channel or optoelectronic device layers. In order to explore the feasibility of the InP planarization approach for multi-layer III-V film stack structures, we demonstrated the deposition of a uniform InGaAs channel layer on top of the patterned InP buffer.

Acknowledgments

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Figures

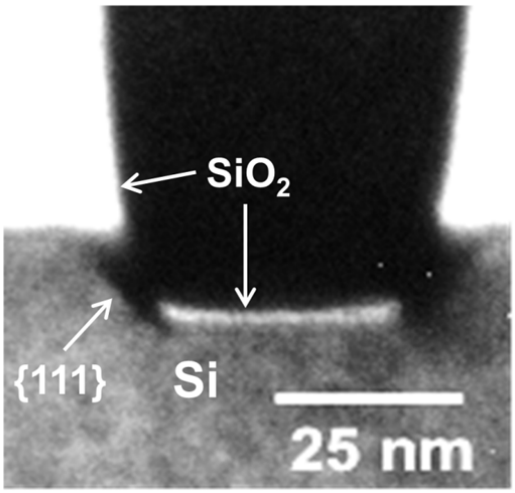


Figure 1. TEM image of a cross section of the SiO_2 trench with {111} Si facets exposed at the bottom edges**.**

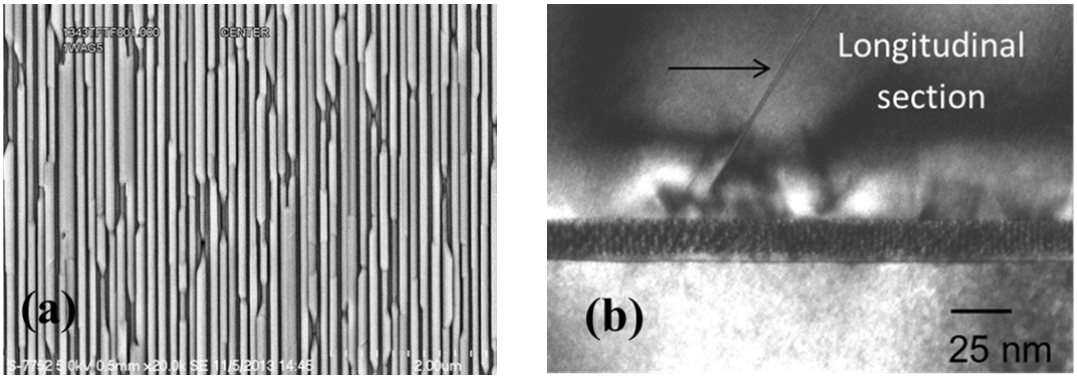
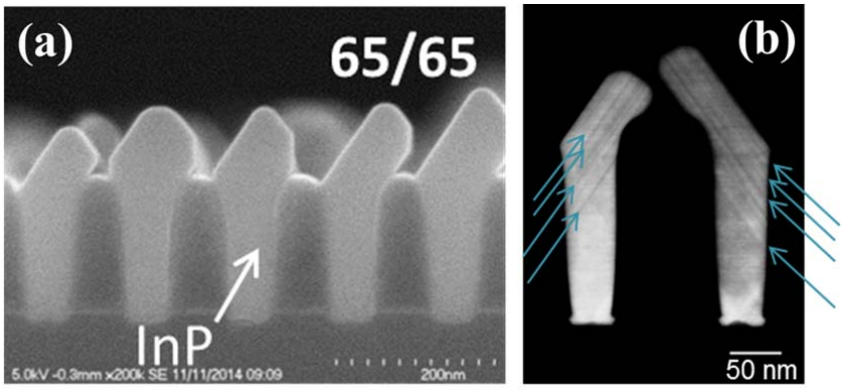


Figure 2. (a) Top-down view SEM image of InP fins on Si (001); (b) TEM image of a cross section along [110], the direction parallel to the trenches.



286 **Figure 3.** (a) SEM image of a cross section along [1$\bar{1}$0] of InP fins selectively grown in 180
287 nm deep SiO_2 trenches with a nominal width of 65 nm. (b) TEM image of a cross section
288 along [1$\bar{1}$0], showing the twinned lamellas, indicated by arrows.

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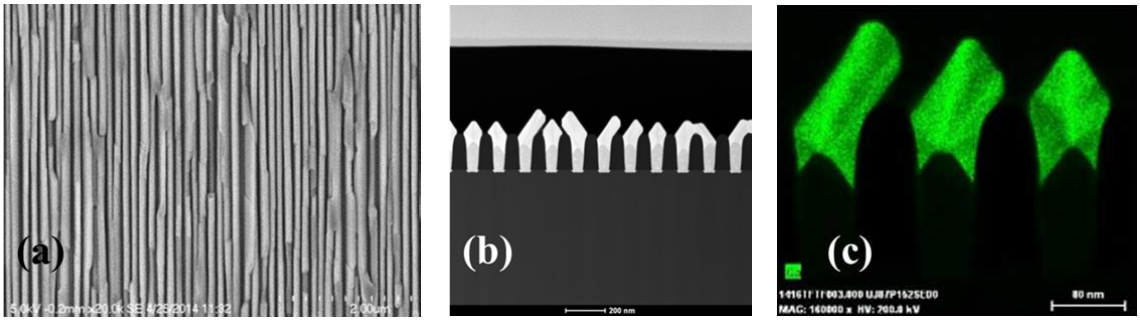

291 **Figure 4.** (a) Top-down view SEM image of InGaAs/InP fins on Si (001); (b) bright field
292 HAADF-STEM image of a cross section along [1$\bar{1}$0], showing the tilted InGaAs fins; (c)
293 (EDS)-TEM map of the Gallium Kα peak.

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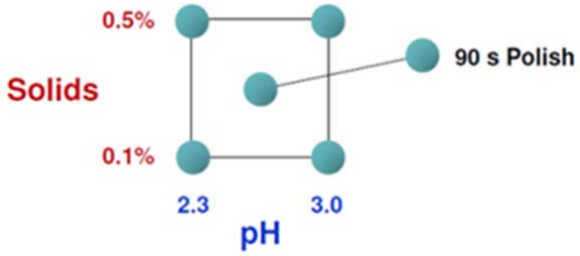

296 **Figure 5.** Illustration of the InP CMP design of experiments.

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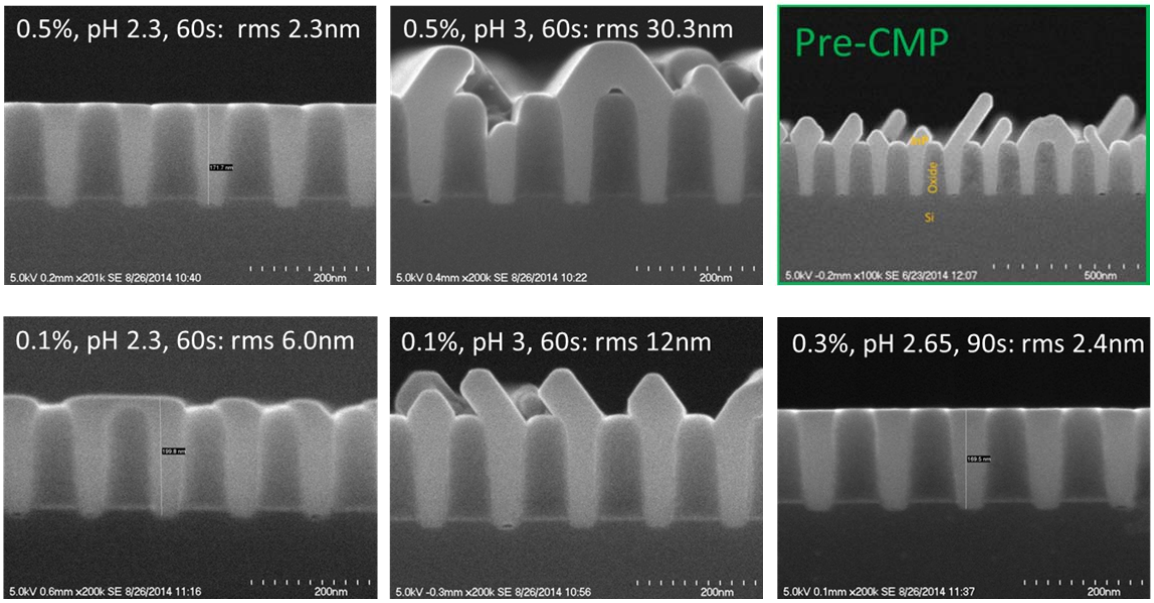

Figure 6. Cross-section SEM images of test structure post InP CMP. CMP parameters and measured AFM roughness are indicated for each cross-section.

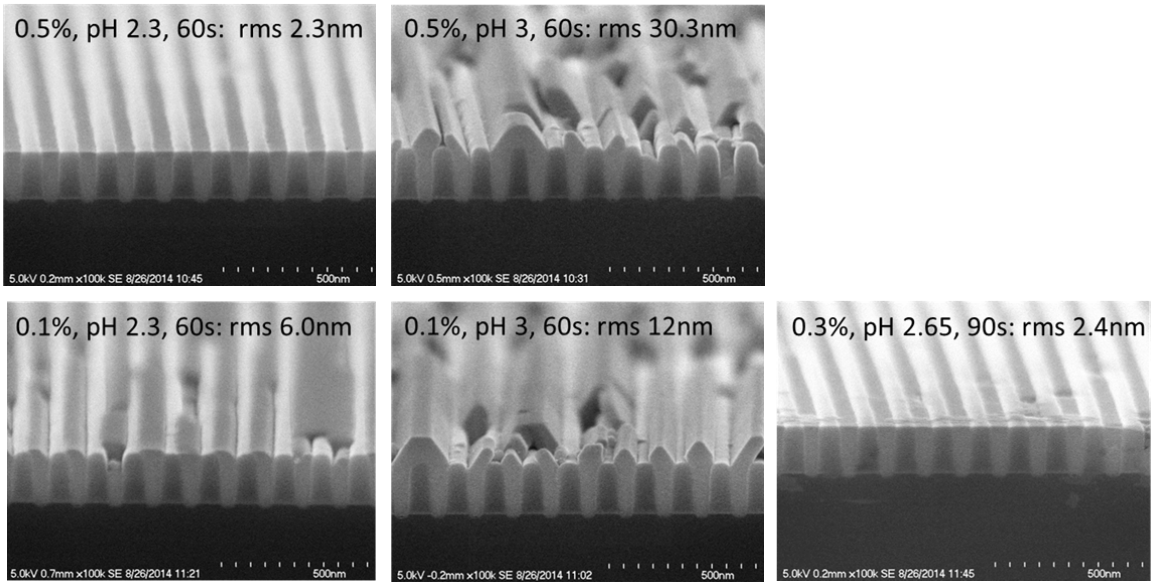

Figure 7. Tilt cross-section SEM images of test structure post InP CMP.

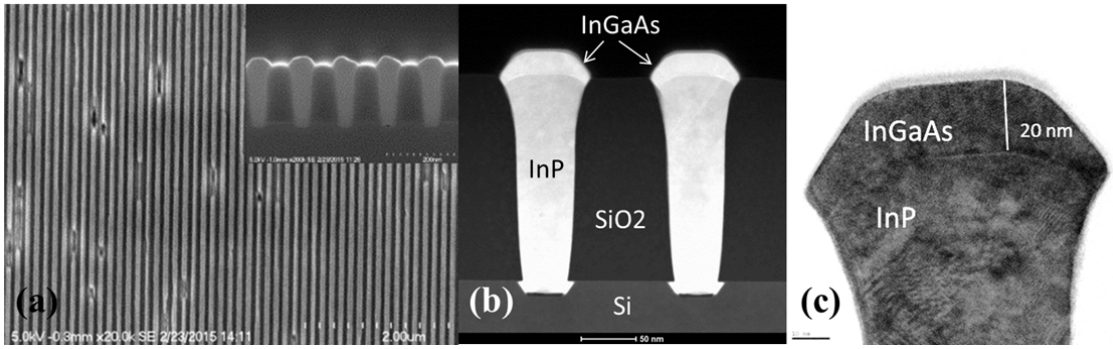

Figure 8. (a) Top-down view SEM image of InGaAs/InP fins on Si (001); Inset: SEM image of a cross section along [1$\bar{1}$0] of InGaAs/InP fins and (b) TEM bright field image of InGaAs/InP fins; (c) TEM dark field image of the InGaAs/InP fin top.

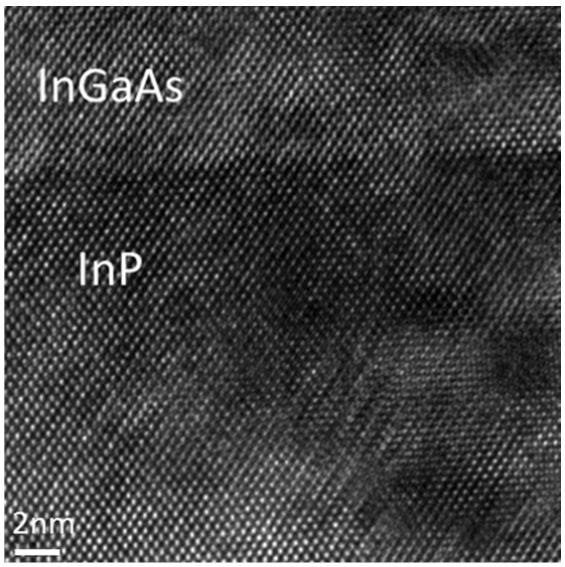

Figure 9. HAADF-STEM of the InGaAs/InP interface.