Nanoscale Properties of Molecular and Oxide Based Thin Film Devices Measured by SPM

Isam Abdullah
School of Physics and Astronomy
Cardiff University

A thesis submitted for the degree of
Doctor of Philosophy in Nanophysics
May 2016

DECLARATION

This work has not been submitted in substance for any other degree or award at this or any other university or place of learning, nor is being submitted concurrently in candidature for any degree or other award.

Signed ………………………………………… (candidate) Date………………….

STATEMENT 1

This thesis is being submitted in partial fulfillment of the requirements for the degree of ………PhD…………………(insert MCh, MD, MPhil, PhD etc, as appropriate)
Signed …………………………………………(candidate) Date …………………….

STATEMENT 2

This thesis is the result of my own independent work/investigation, except where otherwise stated.
Other sources are acknowledged by explicit references. The views expressed are my own.

Signed ………………………………………… (candidate) Date ……………………

STATEMENT 3

I hereby give consent for my thesis, if accepted, to be available online in the University's Open Access repository and for inter-library loan, and for the title and summary to be made available to outside organisations.

Signed ………………………………………… (candidate) Date ……………………

STATEMENT 4: PREVIOUSLY APPROVED BAR ON ACCESS

I hereby give consent for my thesis, if accepted, to be available online in the University's Open Access repository and for inter-library loans **after expiry of a bar on access previously approved by the Academic Standards & Quality Committee.**

Signed ………………………………………… (candidate) Date …………………..

Table of Contents

Declaration i

List of contents ii

List of figures v

List of tables xii

Abbreviations xiii

Acknowledgments xvi

Abstract xvii

1 Introduction 1

2 Theoretical background 9

- 2.1 Introduction 9
- 2.2 Thin film transistors 10
- 2.3 Thin film transistor structure 10
- 2.4 Basic operation of TFT 12
- 2.5 Basic theory of TFT characteristics 14
- 2.6 The main components of a TFT 16
  - 2.6.1 The substrate/ gate 16
  - 2.6.2 Dielectric layer 16
  - 2.6.3 Source and drain electrode 18
- 2.7 Electrical characterization of ETs 19
  - 2.7.1 Transfer characteristic 19
  - 2.7.2 Output characteristic 21
- 2.8 Contact resistance (CR) 22
- 2.9 Organic semiconductor 23
- 2.10 Charge transfer in OS 26
- 2.11 Factors affecting charge transport in OS 28
  - 2.11.1 HOMO and LUMO level 28
  - 2.11.2 Molecular structure and packing 29
  - 2.11.3 Material impurities 30
- 2.12 Semiconductor Materials investigated 31
  - 2.12.1 Organic small molecules 31

2.12.2 Metal oxide semiconductor..................34
3 Morphology control strategies for solution processed TIPS-PEN thin film..................36
3.1 Introduction..................36
3.2 Solvent blend casting..................38
3.2.1 Vitrification..................38
3.2.2 Phase separation..................38
3.2.3 Crystal nucleation..................40
3.3 Solubility parameter and TIPS-pentacene solubility..................41
3.4 Experimental details..................42
3.5 Film casting and evaporation..................45
3.6 TIPS-PEN crystalline thin film growth..................47
3.7 Evaporation dynamic and crystal growth..................54
3.8 Performance of Pure TIPS-PEN transistor..................58
3.9 Step edge grain statistics..................59
3.10 Influence of low concentration of polystyrene on crystal growth, surface roughness and OFET device performance of TIPS-PEN..................60
3.11 Conclusions..................76
4 In_2O_3 thin film transistors..................77
4.1 Introduction..................77
4.2 Experimental details..................80
4.2.1 Preparation procedure..................80
4.2.2 Device Characterization, bonding, and measurements..................81
4.3 Indium oxide Surface morphology..................82
4.4 Electric characterization of In_2O_3 TFT..................84
4.4.1 The output characteristic..................84
4.4.2 The transfer characteristics..................86
4.5 Gradual channel model for threshold and mobility extraction..................88
4.6 Effects of active layer thickness and device dimension..................88
4.7 Bias stress and device instability..................93
4.8 Surface potential images about charge trapping (Spatial distribution of trapped charges)..................101
4.9 Surface potential study of indium oxide TFT..................108
4.10 Mapping of Aluminium diffusion in In_2O_3 Thin film transistor and modelling potential profiles..................119
4.11 Conclusions..................125
5 High Sptial Resolution Electrostatic Force Microscopy (EFM)..................126

5.1 Introduction……………………………………………………………………..127
5.2 EFM phase measurements and its theory………………………………………128
5.3 Experimental details……………………………………………………………132
5.4 Imaging processing and data analysis…………………………………………135
5.4.1 Study 1 :Effect of scan size..137
5.4.2 Study 2: Effect of tip height..137
5.4.3 Study 3: Effect of tip bias 140
5.4.4 study 4:Effect of signal frequency 141
5.5 Design of a new software for EFM data………………………………………145
5.5.1 Au(111)/mica 152
5.5.2 MDMO-PPV/PCBM...154
5.6 Further improvements in EFM data……………………………………….. 155
5.7 Organizing the new experiment set up for transistor measurements…………. 157
5.7.1 Study 1: At low drain bias (linear region). 161
5.7.2 Study 2: At high drain bias (saturation region)..162
5.8 Comparison between SKPM and EFM (new software) images……………….164
5.9 Conclusions……………………………………………………………………167
6 Conclusions and potential future work……………………………………………..168
References…………………………………………………………………………175

List of figures

Figure 1.1: Schematic Atomic Force Microscopy operation…………………………2

Figure 1.2: The tip-sample interaction as a function of the distance…………………3

Figure 1.3: The molecular structure of 6,13-bis(triisopropyl-siylethynyl) pentacene (TIPS-PEN)………………………………………………………………………5

Figure 2.1: Basic structures for thin film transistor presenting top contact bottom gate and bottom gate bottom contact……………………………………………………...11

Figure 2.2: The flow direction of current in top contact- bottom gate and bottom contact-bottom gate configratios…………………………………………………12

Figure 2.3: (a) TFT structure and corresponding gate biasing conditions. (b) The equilibrium condition. (c) $V_g < 0$V. (d) $V_g > 0$V……………………………………13

Figure 2.4: Application of a negative gate bias on p-type organic semiconductor. The E_F of metal raises by gate bias and leads to OS band to bend as they re-equilibrate .14

Figure 2.5: Dielectric constant versus band gap of some gate oxides ..…….………17

Figure 2.6 : Schematic diagram for sub-threshod slop and drain current I_{on}/I_{off} ……20

Figure 2.7: Typical output curves for metal oxide TFT with V_g=1 to 10(step 1V)….21

Figure 2.8: Schematic diagram for Top contact bottom gate TFT describing channel and interface resistance…………………………………………………………23

Figure 2.9: Two connected carbon atom with its orbitals, and energy levels of occupied and unoccupied levels for σ and π levels……………………………………………25

Figure 2.10: Energy gap dependence on conjugation length………………………...27

Figure 2.11: Energy level diagram of charge injection process in OS………………29

Figure 2.12: Metal work functions relative to HOMO and LUMO for different organic material………………………………………………………….…………..….29

Figure 2.13: Highly ordered TIPS-PEN molecules on SiO_2 substrate………………30

Figure 2.14: Chemical structure of impurities found in pentacene …………………31

Figure 2.15: Edge to face herringbone structure……………………………………32

Figure 2.16: Two dimensional Brickwork arrangements. The arrow refers to the direction of charge transport which can take place...33

Figure 2.17: Face to face 1D ***slipped stack*** arrangements. Again the arrow refers to the charge transport which can take place only in one direction…………………….…33

Figure 2.18: Electron transport and conduction path in [a] crystalline Silicon [b] amorphous Silicon [c] crystalline metal oxide [d] amorphous metal oxide…………35

Figure 3.1: Free energy as a function of composition change and spinodal, binodal curves at various temperatures……………………………………………………39

Figure 3.2: Homogenous nucleation mechanism 40

Figure 3.3: Crystallization starts from seed crystal followed by crystal nucleation and formation of large crystal..41

Figure 3.4: Drop casting TIPS-PEN solution with different composition of anisole and decane on Si wafer..44

Figure 3.5: Specialized Glove box for gold evaporation and deposition of contacts through shadow mask..44

Figure 3.6: Image of microprobe station and semiconductor device analyser.........44

Figure 3.7: anisole and decane chemical structure......................................45

Figure 3.8: Optical microscope (OM) images of TIPS-PEN droplet with various solvent compositions..47

Figure 3.9: Scanned AFM image in tapping mode of a crystalline domain taken from edge of droplet..48

Figure 3.10: AFM image taken from centre of droplet and corresponding profile across drown line. The line profile reveals some peaks when the line crossing grains..49

Figure 3.11: AFM images in tapping mode of TIPS-PEN drop-cast from anisol:decane 95:5 vol/vol with total vertical range 25nm. Line profile across terraces shows step height of 1.53± 0.09 and 1.61±0.11 nm respectively..50

Figure 3.12: A) AFM images of 9% decane concentration and the line presenting step heights (1.41, 1.60 and 3.5nm respectively from left)...................................52

Figure 3.13: Tapping mode AFM images of A) 15% decane. B) 20 percent of decane , we notice that the steps become unclear or undefined...................................53

Figure 3.14: Change of roughness with decane concentration..........................54

Figure 3.15: A droplet of TIPS-PEN solution on tilted substrate and the possible growth mechanism..55

Figure 3.16: Schematic presentation of film drying by using binary solvents system the dark blue shows solvent with high boiling point...56

Figure 3.17: UV/Vis absorption spectra of TIPS-PEN dissolved in different anisole/decane solvent mixtures..57

Figure 3.18: Grains statistic according to their mean height and equivalent mean disc radius..59

Figure 3.19: Polarized Optical micrographs for pure TIPS-PEN film and four TIPS-PEN/PS blends ratio at 30C°..61

Figure 3.20: Tapping mode AFM image of 5% Ps shows step height (1.62± 0.15) ..62

Figure 3.21: AFM height and phase images of 5% polystyrene blend with cross sectional line profile. The measured step height is (1.96±0.11) nm. The phase image shows the appearance of larger grain size suggesting polystyrene visage during phase segregation..62

Figure 3.22:10% polystyrene blends AFM images with dendrite style and wide terrace……….……………………………………………………………………63

Figure 3.23: Atomic force microscopy images of drop cast film of TIPS-PEN:15% aPS 2%wt blends…………………………………………………………………………64

Figure 3.24: 20% polystyrene blend. The terraces contain lots of holes or openings sharing only with one white ball...65

Figure 3.25: Flat area roughness variations with aPS composition in the blend on SiO_2..65

Figure 3.26: Polarized optical microscopy images of pure TIPS-PEN and TIPS-PEN:Polystyrene blends according to Ps weight fraction…………………………..67

Figure 3.27: AFM images for pristine TIPS-PEN on PVP dielectric. The top images show TIPS-PEN islands distribution while the bottom image reveals well defined large terraces………………………………………………………………………...68

Figure 3.28: AFM images for 95:5 of TIPS-PEN/aPS blend. The wavy style of ordered film is clear and the terraces fluctuate between narrow and wide…………………..69

Figure 3.29: AFM images for 10 percent ratio blend composition. The images exhibit straight line ordering and well defined film pattern…………………………………70

Figure 3.30: AFM images for TIPS-PEN:PS of 85:15, the appearance of wavy style of molecular ordering again……………………………………………………………71

Figure 3.31: AFM images for 80/20 TIPS-PEN and Ps ratio. Appearance of wide terraces with white grains again……………………………………………………..71

Figure 3.32: Flat area roughness of TIPS-PEN/aPS blends on PVP………………..72

Figure 3.33: The mobility change according to TIPS-PEN/aPS blends ratio on PVP dielectric. Black graph refer to maximum mobility, red presents average mobility, and the blue is minimum mobility..……………………………………………………….. 73

Figure 3.34: Average mobility changes of transistors according to the active layer composition of TIPS-PEN and its blends of polystyrene on PVP and SiO_2 dielectric…………………………………………………………………………...74

Figure 4.1: a) The specific transistor before bonding, b) after bonding with gold wire…………………………………………………………………………………..81

Figure 4.2: AFM images of single spin coating and double spin coating film of ndium oxide…………………………………………………………………………………83

Figure 4.3: Single spin coating transistor of dimension W1500L40S. The gate bias Vg= 1, 2, ..10V step 1V bottom images are for corresponding devices with Al electrodes……………………………………………………………………………85

Figure 4.4: The output and transfer charaacteristic of: a), double spin coating W1000L30D, b), single spin coating W1000L30S. The gate bias V_g= 1, 2,3,…10V step 1V for both doable and single spin…………………………………………………..89

Figure 4.5: The output characteristics at V_g= 1, 2,3,…10V step 1 V of double (a) and single (b) spin coating thin film transistor of dimension W1000L20. c and d), the corresponding transfer characteristics at V_d =10V..…………………………………91

Figure 4.6: Transfer characteristic curves shift with stressing time on W=1000µm and L=30µm single spin coating device……………………………………………………94

Figure 4.7: Time dependence of threshed voltage shift under the applied gate bias stress 10V in linear scale and logarithmic scale…………………………………………....97

Figure 4.8: Drain current decrease with stress time…………………………………98

Figure 4.9: Transfer characteristics back shift after stress release of device W= 1000µm and L=30µm……………………………………………………………………..…….100

Figure 4.10: Threshold voltage recovery after switching off the gate bias. The data is plotted in both linear and logarithmic scale……………………………………...100

Figure 4.11: The output and transfer characteristics of W=1500, L= 40µm………..102

Figure 4.12: Surface potential images before and after applying +5V gate bias with source and drain electrodes grounded………………………………………………102

Figure 4.13: Surface potential image after setting gate bias to zero ……………….104

Figure 4.14: Surface potential profiles variation as a function of scanning time with the slow scan axis disabled…………………………………………………………..104

Figure 4.15: Captured surface potential and line profiles, continuing from Figure 4.14, showing device recovery with time for the second scan from top to bottom………………………………………………………………………………105

Figure 4.16: AFM height image a), across two electrodes b), 5µmx5µm AFM image captured between two electrodes c), EFM surface potential before applying gate bias d), EFM after applying +8V gate bias……………………………………………..106

Figure 4.17: Recovery of the device after switching the gate bias to zero. a), Scanning from top to bottom, b), scanning from bottom toward top, c), scanning from top toward bottom. The time taken per image is about 8.1min……………………………………………………………………………107

Figure 4.18: Experimental setup used for indium oxide TFT surface potential measurements……………………………………………………………………109

Figure 4.19: AFM topographic image of W1000L30S device and the corresponding line profile. The channel between electrodes is clearly seen and contain no voids or discontinuity……………………………………………………………………..110

Figure 4.20: 2D surface potential images of L30W1000S device at 0, 1, 2, 4, and 6V drain bias……………………………………………………………………………111

Figure 4.21: The W1000L30S device potential profiles acquired for different drain biases with grounding the source and gate terminals. The drain electrode edge is marked as a dashed red line…………………………………………………………....112

Figure 4.22: The W1000L30S device potential profiles at fixed 5V gate voltage and varied drain biases………………………………………………………………….113

Figure 4.23: Change of first derivative of potential across the channel and pecification of electrode and diffusion position. The green curves represents the potential and the red curve is the first derivative of potential. The plotted data corresponding to Figure 4.20 and Figure 4.21 for drain bias values 0, 1, 2, 4, and 6V………………………115

Figure 4.24: Potential profiles as a function of gate bias where V_d =1V (linear region) and gate bias changed from 0 to 10V step 2V…………………………………….116

Figure 4.25: Potential profiles inside the operating device where drain voltage kept constant at high voltage 9V and gate bias changed with step 2V from 0 to 10V…..116

Figure 4.26: Surface potential profiles across W200L40D device at fixed gate bias +5V. ……………………………………………………………………………….117

Figure 4.27: Gate voltage dependence potential profiles inside operating L40W200D device. The drain bias was constant +8V during the experiment and gate voltage changed from 1 to 10V step 1V. The profiles obtained after subtraction the reference profile at V_d= 0 from all $V_d \neq 0$…………………………………………………….118

Figure 4.28: The potential distribution at the surface when the single-spin TFT is grounded. Only the source and drain electrodes can be detected at 0 V. (b) Measured and simulated potential profiles at V_d=0 V and V_d=5 V when V_g=0V. (c) Calculated second derivative of the surface potential at V_d=0 V (dashed line) and V_d=5 V (solid line) represents a change in the lateral electric field and allows determining exactly a diffusion region edge………………………………………………………………122

Figure 4.29: Measured and simulated potential profiles at V_d= 3V for the single –spin In_2O_3 TFT at V_g =0 and V_g= 5V…………………………………………………….123

Figure 4.30: Height line scans for V_d from 0V to 3V demonstrate the electrostatic contribution to the apparent morphology of the sample and for the drain bias V_d > 2V position of the diffusion region can be determined………………………………...124

Figure 5.1: Multimode base plate showing location and orientation of jumpers….132

Figure 5.2: Jumper configuration of applied voltage to the tip……………………133

Figure 5.3: Triggering module for EFM synchronization…………………………133

Figure 5.4: Diagram of EFM scanning process in height and lift mode…………...134

Figure 5.5: AFM captured image for graphite surface for 1µm scan size. The applied bias and corresponding phase shift………………………………………………...135

Figure 5.6: Phase- voltage calibration curve of AC sinusoidal signal at 1V and 10 Hz. The tip height is 20 nm, scan rate 1 Hz and scan size is 1µm……………………136

Figure 5.7: Phase-voltage parabola image for 5nm scan size, 1 Hz scan rate, frequency 10 Hz and bias 1V……………………………………………………………..137

Figure 5.8: Phase-voltage parabola with different tip height 20nm, 50nm, 70nm, 100 nm, 150nm. Scan size 5nm, tip bias 4.5V and frequency 12 Hz…………………...138

Figure 5.9: Phase-voltage parabola with tringle wave form of bias 4.5V, frequency 12Hz and tip height 20nm), 50nm, 150nm bottom…………………………………139

Figure 5.10: Phase-voltage calibration curve for various tip biases 1, 2, 3, and 4V. The signal frequency is 10 Hz, tip height 20nm and scan size is 1µm…………………..140

Figure 5.11: Phase-voltage parabola for sinusoidal wave form of varied frequency at 2Hz, 5Hz, 10 Hz, 15 Hz, 20 Hz and 25 Hz, tip bias 4.5V, and 20nm tip height.…141

Figure 5.11b: Phase-Voltage parabola for sinusoidal wave form at frequency 20 Hz and 25 Hz .Tip bias 5.4 V and 20 nm was tip height……………………………………...142

Figure 5.12: Phase-voltage curves after connecting 8 MΩ resistance at frequency 2 Hz, 5 Hz, 12 Hz, 15 Hz, 20 Hz , and 30 Hz. Tip bias is 4.5V, tip –sample separation 20nm……………………………………………………………………………..143

Figure 5.13: Parabola shifts as a function of frequency with and without connecting 8 MΩ resistance……………………………………………………………………144

Figure 5.14: The phase-voltage calibration curve for only half of signal…………145

Figure 5.15: a), Topography, b), bias of signal frequency of 30 Hz, c), the resulting phase shift obtained by using the new software……………………………………146

Figure 5.16: The measured voltage data and corresponding phase for first row obtained from figure 5.15. The applied tip bias is 2V, frequency 30 Hz……… ………..…..147

Figure 5.17: Phase-voltage calibration curves before and after applying time delay for different frequencies. a),10 Hz, b) 20 Hz, c), 30 Hz, d), 50 Hz with tip height 20 nm for all………………………………………………………………………….…….148

Figure 5.18: An improvement in phase-voltage calibration curve after applying the effect of time delay. The image is for *f*=30 Hz, *d*= 20 nm on gold surface. a), green line shows data distribution before applying time delay correction and blue circles indicate data after correction. b), the image after fitting the data…………………..149

Figure 5.19: Phase-voltage calibration when nside= 40, *f*= 30 Hz, tip bias= 2V, tip height = 20 nm, and scan size = 1µm……………………………………………150

Figure 5.20: Phase-voltage calibration curves for different values of nside. a) nside= 20, b) nside= 15, c) nside= 10, and d), nside=7. All images for gold Au(111)/mica, tip bias= 2 V, tip height=20 nm, and *f* = 30 Hz…………………………………..…151

Figure 5.21: a) Gold topography, b) the second derivative of capacitance, c) 2D images of CPD, d) phase offset, e) reduced chi square. The images taken for *d* = 20nm, *f* = 30 Hz, delay = 0.73 msec, nside=6…………………………………………………153

Figure 5.22: a) MDMO-PPV/PCBM surface topography, b) second derivative of capacitance, c) 2D images of CPD, d) phase offset. The images taken for *d* =20 nm, f=30Hz………………………………………………………………………...154

Figure 5.23: a) Surface topography of Au(111)/mica, b) random AC applied bias to the tip in contrast with Figure 5.15b, c) the resulting phase shift……………….………...155

Figure 5.24: 2D images of Au(111)/ mica surface topography, second derivative of capacitance, CPD, the phase offset and related reduced chi square at tip bias 0.5 V, *f* = 30 Hz, d = 20nm……………………………………………………………..…..156

Figure 5.25: LabJack U3-HV -USB Multifunction data acquisition ………………157

Figure 5.26: EFM experiment set up with controlling program……………………158

Figure 5.27: potential line profiles at V_d = 0, 1, 2, 3, 4 V and V_g = 0 V with grounded source. The second figure in the right is a topography image which reveal the position of two electrodes and channel, Aspect ratio is 2/1…………………………………159

Figure 5.28: 2D images for W1000L30D corresponding to the above profiles for *Vd=0, 1, 2, 3, 4, 5* V……………………………………………………………………………......160

Figure 5.29: Effects of time delay changes on potential profile for 1V drain bias…162

Figure 5.30: Effect time delay on potential profile for W1000L30D operating device under drain bias V_d = 5 V and V_g = 0 V……………………………………………163

Figure 5.31: The optimal time delay needed for fitting of parabola at drain bias 6V.....……………………………………………………………………………..164

Figure 5.32: Potential profiles comparison in SKPM (solid lines) and EFM-phase mode (dotted lines) for V_g = 0 V and V_d = 0, 1, 2, 3, 4 V. SKPM and EFM profiles confirm Al diffusion region close to the drain which appeared as a flat region. ……………...165

List of tables

Table 1.1: The work functions for some interesting metallic elements 19

Table 3.1: The value of roughness (rms) of captured overall AFM images according to decane concentration in blend 53

Table 3.2: Summarized maximum, minimum, and average mobility results obtained on transistors as a function of anisol:decane ratio 58

Table 3.3: Electrical properties of drop casted TIPS-PEN and aPS blended OFET 64

Table 3.4: Summary of mobility measurements presents the average, minimum, and average mobility according to the blend composition 72

Table 3.5: Comparison of mean saturated mobility of pure TIPS-PEN and its blend with polystyrene on PVP and SiO_2 73

Table 4.1: The electric performance of In_2O_3 devices of 100nm thick SiO_2 dielectric according to the device dimension W and L and film thickness..................................... 87

List of Abbreviations and symbols

AFM	Atomic force microscopy/ microscope
BCBG	Bottom contact- bottom gate
C	Capacitance
CPD	Contact potential difference
D	Drain
ε_o	Vacuum permittivity
E_f	Fermi level
EFM	Electrostatic force microscopy
FET	Field effect transistor
G	Gate
HOMO	Highest occupied molecular orbital
K	Dielectric constant
LUMO	Lowest unoccupied molecular orbital
MDMO-PPV	Poly[2-methoxy-5-(3,7-dimethyloctyloxy)-1,4-phenylenvinylene]
MOS	Metal-oxide semiconductor
OFET	Organic field effect transistor
OM	Optical microscopy/ microscope
OS	Organic semiconductor
OSM	Organic small molecule
P3HT	Poly(3-hexylthiophene-2,5’-diyl)
PCBM	Phenyl-C61-butyric acid methyl ester

S	Source
SC	Semiconductor
SKPM	Scanning Kelvin probe microscopy
SP	Surface potential
SPM	Scanning probe microscopy
TCBG	Top contact-bottom gate
TCBG	Top contact-bottom gate
TFT	Thin film transistor
TIPS-PEN	6,13-bis(triisopropyl-siylethynyl) pentacene

Publications

1. Isam Abdullah[a], He Lan,[b] John Morrison,[b] Ahmed Alharbi, [b] J Emyr Macdonald[a] and Stephen G. Yeates[b,*] ***The effect of formulation on the morphology and crystallization of thin film 6,13-bis(triisopropylsilylethynyl-pentacene based semiconductors.***

   (a) School of Physics and Astronomy, Cardiff University, The Parade, Cardiff CF24 3AA, U.K. (b) Organic Materials Innovation Centre, School of Chemistry, The University of Manchester, M13, 9PL, Manchester, United Kingdom.

   Submitted to **Thin Solid Films**

2. Olga Kryvchenkova*[1], Isam Abdullah[2], J. Emyr Macdonald[2], Martin Elliott[2], Thomas D. Anthopoulos[3], Yen-Hung Lin[3], Petar Igić[1], Karol Kalna[1], Richard J. Cobley[1] ***"A non-destructive method for mapping metal contact diffusion in In_2O_3 thin-film transistors''***

   [1]Electronic Systems Design Centre, Swansea University.

   [3]Department of Physics and Centre for Plastic Electronics, Blackett Laboratory, Imperial College London.

   Submitted to **ACS Applied Materials and Interfaces**

Patent

UK Patent Application No. 1514732.5
"*Generic Modulation Analysis Approach For Scanning Probe Microscopy*"

Isam Abdullah, J. Emyr Macdonald, Martin Elliott

Filed and Submitted

Conferences

1. Conference of science of inkjet and printed drop 2011 London, Nov.2011. Institute of physics, London UK

2. Conference of postgraduate students 2012.Cardiff University School of Physics and astronomy, Sep20I2. Cardiff UK.

Acknowledgment

Put God in the centre and everything will come together

Every successes I have had are due to the gorgeous people around me who I owe a lot of thanks. Firstly, I would like to express my deepest thanks to my supervisors Professor J.E.Macdonald and Dr.M.Elliot, for giving me support and encouragement throughout my research work. I highly appreciate them for guidance, consultations, correcting my mistakes, and listening to my ideas and providing fruitful discussions.

A huge acknowledgment must go to my mother for her confidence in me during childhood which made me believe I could fulfil any goal and achieve any target. I am deeply thankful to my awesome wife Muzhda whose patience, love, ongoing support through my many years of academic study made this thesis possible. A big thanks to my children, brothers, sisters, and all relatives who have always been there to share my joys and sorrows along the way.

Thanks to my friends in the research group; Rangeen, Athraa, Adam, and Susanne for assistance and a lovely friendly atmosphere in our lab. My gratitude to Mr. R Tucker for his help on the technical side.

Finally, a special acknowledgment to the Iraqi Cultural Atteche and Salahaddin University for financial and ongoing support.

Abstract

Organic and inorganic-metal oxide thin film transistors can be solution-processed, providing large area, low cost and low processing temperature leading to strong industrial and research interest. The nanoscale properties of each material system have been investigated using scanning probe techniques.

Pentacene is a model small molecule organic semiconductor but it is an air sensitive material and insoluble. However, its derivative 6,13-bis(triisopropyl-silylethynyl) pentacene (TIPS-PEN) is amenable to solution processing. The motivation to study TIPS-PEN is not to chase performance figures only but to investigate how the solution deposited film topography can be controlled by varying the solvent composition and the insulating polymer binder concentration. We report the effect of anisole / decane binary solvent mixture and the subsequent addition of low percentage weight of (atactic amorphous polystyrene) aPS on the surface morphology of TIPS-PEN thin films. It was found that addition of up to 20 wt% decane has little impact on micro-scale crystal morphology but has a significant influence on the growth mode, mean grain size and terrace roughness. The effect of the TIPS-PEN / aPS blend ratio up to 20 wt% of aPS in drop-cast thin film was similarly investigated on untreated SiO_2 and on poly(4-vinylphenol) (PVP) interlayers. It is found that addition of aPS has a vital effect on macroscopic crystal properties such as surface coverage, unity of orientation, long range order, and average field effect mobility. It also changes the surface morphology and layer ordering on the nano-scale. Mobility values obtained from PVP treated surface were higher than those from SiO_2 surface by five times, which was consistent with preferred TIPS-PEN crystal growth on hydrophobic surface PVP of low surface energy.

Indium oxide (In_2O_3) is an n-type (electron transport), optical transparent with wide band-gap values between 3.5 and 4 eV, and high performance semiconductor. Spin coating was

used to prepare indium oxide thin film transistors (TFT) of two different thicknesses of the device channel.

As the thickness of the In_2O_3 active layer is increased, the device mobility increases, the threshold voltage is shifted in the negative direction, off-drain current is increased, and on-drain current is less pronounced. A systematic study was carried out to investigate the transistor stability under bias stress.

Applying a positive gate bias stress to indium oxide transparent TFTs was found to induce a parallel shifts of threshold voltage in positive direction without changing the device mobility or the subthreshold gate voltage swing.

Scanning Kelvin Probe Microscopy (SKPM) was used to study the surface potential distribution of operating devices under a range of drain and gate biases. The potential profiles showed evidence of metal contact diffusion into the channel region which appeared as a flatting of the profile close to the drain electrode. The experimental data was confirmed and complemented with simulation results for contact material diffusion into the In_2O_3 channel.

A new method of performing Electrostatic Force Microscopy (EFM) was developed and applied to the In_2O_3 TFT. The tip bias was modulated and the resulting phase difference between the cantilever response and the applied bias was recorded. The measurements were affected by a time delay, likely to be caused by capacitive charging of the semiconductor beneath the tip. The effects of the time delay were corrected by the use of an inverse filter in the analysis software developed. This new version of the EFM-phase method was applied to the operating biased In_2O_3 TFTs and the results compared with those obtained with SKPM.

Chapter One

Introduction

The field of nanomaterials research has emerged in the last three decades. It concentrates on the characterisation, manipulation, creation and development of materials at nano-meter length scales. Some materials, which are well understood in the bulk phase offer interesting new properties when the size is decreased to the nano-meter length scale. Nanophysics and nanotechnology are interdisciplinary fields involving materials whose components and structures, due to their nanoscale size, have surprising or enhanced properties. The processing and manipulation of such materials on the nanoscale as well as the fabrication of devices with new sustainable approaches are of paramount importance in view of potential technology based on these materials.

Studies within this area are focused on understanding their properties in order to devise new technologies and, ultimately, to commercialize new devices. Potential applications include: smaller electronic components [1], compact memory [2], more sensitive sensors [3], and energy efficient and faster computers [4].

Study of materials at the nanoscale requires imaging and manipulation tools to achieve the goal. In 1986 Binning *et al.*[5] invented Atomic Force Microscopy (AFM) as an extremely versatile tool for imaging of conducting and non-conducting sample topography. AFM detects piconewton local forces with nanometre lateral high resolution [6, 7]. In this technique the sample surface is scanned by a sharp tip of nano-metric size fixed to a cantilever. During scanning, different forces (van der Waals, magnetic, capillary, electrostatic) disturb the probe's equilibrium condition. The tip - sample interaction forces is measured by monitoring the deflection of the cantilever. The cantilever deflection is in turn usually measured by an optical lever technique [8, 9] in which a laser beam is focused close to the end of the cantilever Figure 1.1. The reflected beam is detected by a quadrant photodiode which produce a voltage difference between two halves of the photodiode, where the voltage on each half is proportional to the light intensity illuminating it. In principle, the sample image could be obtained by

plotting the cantilever deflection versus its position on the surface. In practice it is much more straightforward to maintain a fixed force between tip and sample by adjusting and recording the height position of the translation stage with a feedback loop.

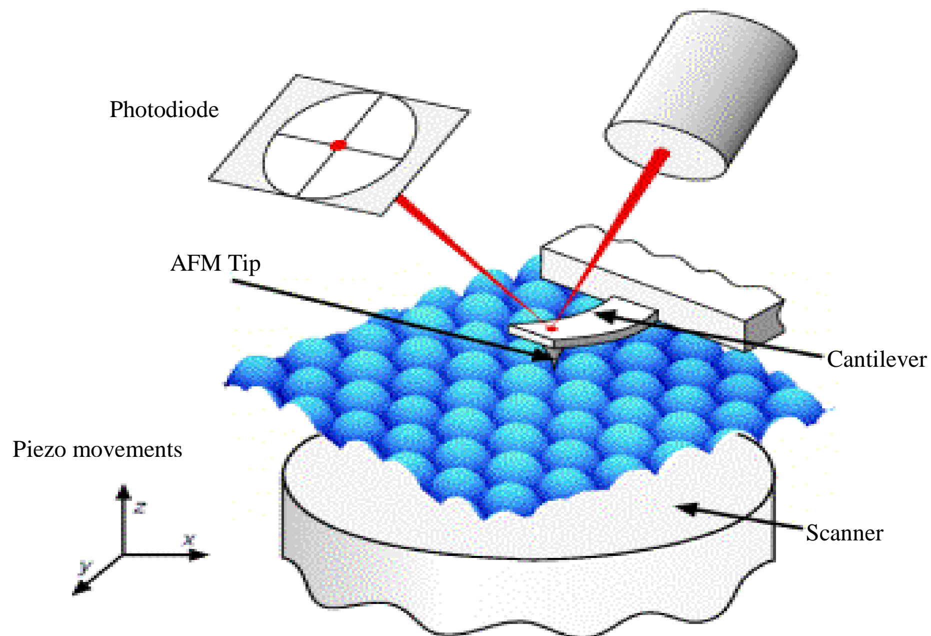


Figure1.1: Schematic Atomic Force Microscopy operation. The tip is attached to the cantilever. Tip-sample interaction leads to cantilever deflection which is monitored by Photodiode sensitive to the reflected beam at the tip back side.

Generally, two modes of scanning in AFM measurements are used; the contact and the non-contact mode. In the contact mode, the tip is kept in physical contact with the surface and operates in the region where the resultant tip-sample interaction is repulsive with a mean value of order of 10^{-9} N. The major drawback of this mode is the possibility of distorting the sample surface and damaging the tip as the cantilever drags along the surface Figure 1.2 illustrates tip- sample interaction as a function of surface separations.

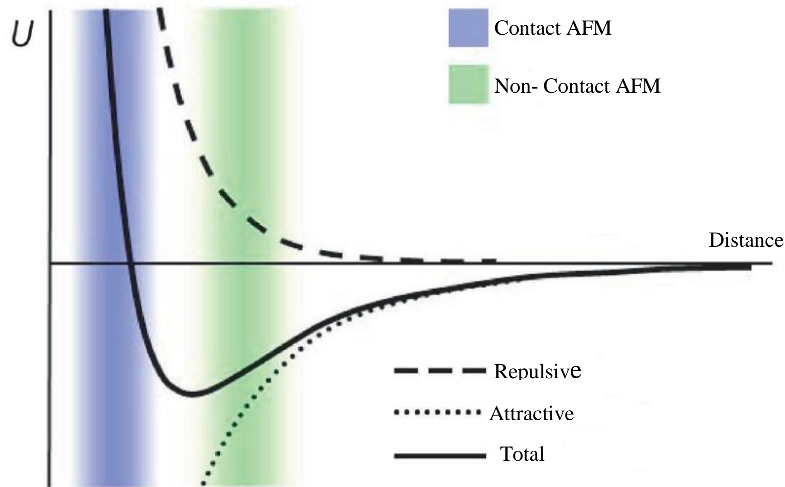


Figure 1.2: The tip-sample interaction as a function of the distance. The minimum potential occurs at a typical distance of about 1-2 nm.

The non-contact mode operates in the region where the resultant tip-sample interaction is predominated by the force of attraction. If the tip is scanned at a constant height, there would be a risk that the tip may collide with the surface causing crushing to both the tip and the material under consideration; hence, in most equipment a feedback mechanism is employed to adjust the tip-to-sample surface distance to maintain a constant force between the tip and the sample. Normally, the monitored sample is mounted on a piezoelectric tube is adjusted vertically (the z-direction) to maintain a constant force, while scanning the sample laterally in the x and y directions.

Intermittent-contact mode, or tapping mode, is another potent technique to probe sample topography with high resolution. In this mode, the cantilever oscillates at or close to its resonant frequency, with the oscillation amplitude being proportional to the amplitude of the AC signal from quadrant photodiode. During scanning in x and y, the feedback loop adjusts z to maintain a constant amplitude (as a fraction of amplitude when the tip is retracted from the surface). Since the tip does not remain in constant contact with the surface, this mode is less destructive to the surface.

The most critical component in AFM is the cantilever spring constant. To achieve excellent sensitivity, a large deflection for a given force is desirable, requiring a soft cantilever (small spring constant). On the other hand, high resonance frequency is best to minimize sensitivity to mechanical vibration and to allow a reasonable high scan speed. A third condition for enhancement of AFM images is the tip sharpness, which is highly recommended for good spatial resolution.

In this thesis, we consider transistor materials which are alternatives to crystalline silicon. Of these, amorphous silicon (a-Si) is the predominant semiconductor used for transistor manufacturing, coming second behind single crystal silicon for use in industry. Amorphous silicon is superior to the polycrystalline form from the viewpoints of processing temperature and device uniformity. However, the carrier mobility in amorphous silicon a-Si:H is of order of 1 $cm^2 V^{-1}s^{-1}$ which is lower than crystalline silicon by about one or two orders of magnitude. The limited mobility in a-Si:H arise from the hopping nature of carrier transport between localized states and band conduction is not achieved [10]. Also, its high photo-induced instability remain the key issues that limiting its applicability[11]. Furthermore, silicon based device are less interesting for transparent electronics because of its rather small band gap and lack of transparency [12].

Among the most interesting materials, organic semiconductors (OS) have been intensively studied and considered as potential candidates to replace amorphous silicon thin film transistors (TFTs). A primary interest for organic materials in thin film transistors is their compatibility for low cost and low temperature processing. Offering possibility of wide use in electronic devices. Kelley *et al.* [13] reported that, with considerable purification, well controlled dielectric, and optimized conditions, TFT mobilities from 0.5 $cm^2 V^{-1}s^{-1}$ to near single crystal values ~ 3 $cm^2 V^{-1}s^{-1}$ could be attained. Pentacene as a small organic molecule has exhibited the highest mobility [14] , better on-off ratio, and better reliability then most other OS [15]. Hence, it is a possible candidate to complement and replace the amorphous silicon technology in many electronics applications. Since then, a new hope has been opened in use of organic small molecule (OSM) as a popular material into electronic device fabrication. However, the major drawback of pentacene is that it is insoluble in organic solvents at room temperature.

In 2001, Anthony *et al.* [16] reported that adding of functional groups to the positions at 6 and 13 on the pentacene ring has an effect on solid state ordering and the electronic properties of the resulting crystal. Moreover, the resulting molecule should has solubility in the majority of organic solvents and the substituents induce ability for pi-stacking array to enhance intermolecular orbital overlap. The soluble pentacene derivative, 6, 13-bis(triisopropylsilylethynel)(TIPS) pentacene (TIPS-PEN) can grow crystalline thin films from solution and composed of large crystal domain suitable for organic FET fabrications [17]. Figure 1.3 shows the molecular structure of TIPS-PEN.

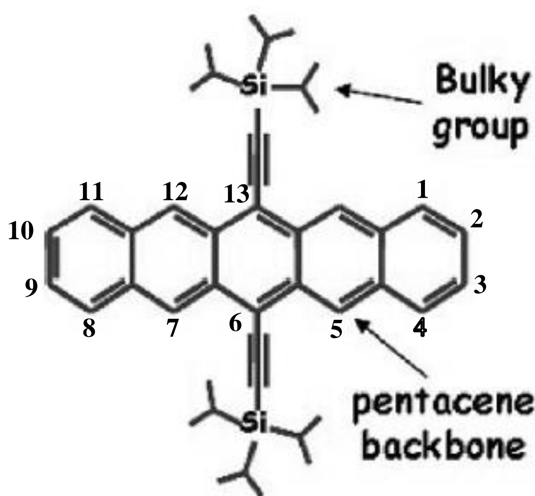


Figure 1.3: The molecular structure of 6,13-bis(triisopropyl-siylethynyl) pentacene (TIPS-PEN)

The performance of organic electronic material is quickly enhanced especially with improved device mobility and controlling thin film surface topography. Solution processable blends of highly crystalline (TIPS-PEN) with insulating polymer is a promising approach to provide, large crystals, high mobility, good film uniformity [18], and small device to device variation of organic field effect transistor (OFET).

On the other hand, metal–oxide semiconductors (MOS) have attracted significant interest [19, 20] because it is a unique class of materials which are transparent and have good conductivity[21, 22].

A growing requirement for transparent semiconducting active materials leads to raised attention on the MOS for new sets of electronic devices, because of their high field-effect mobility, environment stability and optical transparency [23].

This interest is driven by a constantly growing requirement for high performance device using cheap processing methods, compatible with temperature sensitive substrates. One metal oxide semiconductor that gained significance is the wide band gap indium oxide In_2O_3. Indium oxide can be processed by inexpensive and high throughput solution-based deposition such as spin coating and inkjet printing[24]. Moreover, solution–based deposition of MO semiconductors constitutes a simple, high fabrication, low temperature, procedure suitable for large–area electronics. Hwang *et al.* [25] prepared solution based indium oxide TFT by spin coating method. The obtained In_2O_3 device exhibits good uniformity, mobility of order of 2.6 $cm^2\ V^{-1}s^{-1}$, and turn on voltage V_{on} around 0V. Kim *el al.* [26] reported mobility around 2.3 $cm^2\ V^{-1}s^{-1}$ and I_{on}/I_{off} (on/off current) ratio of 10^4 for In_2O_3 precursor (at 300 ^oC) for TFT of 300 nm SiO_2 gate dielectric and 30 nm Al source and drain. Han *et al.* [27] fabricated solution processed In_2O_3 TFT by spin coating method. The synthesized thin film of indium oxide was annealed at different temperature ranging from 200 to 600 ^oC in air or in an O_2/O_3 atmospheric environment. For TFT at 500 ^oC the device showed 55.26 $cm^2\ V^{-1}s^{-1}$ and I_{on}/I_{off} ratio about of 10^7. However, In_2O_3 TFT exhibited mobility between 0.8 to 22.14 $cm^2\ V^{-1}s^{-1}$ and I_{on}/I_{off} 10^5-10^6 for 200 – 300 ^oC under O_2/O_3 . Also, they noted that the annealing atmosphere of O_2/O_3 can yield TFTs with higher performance at low processing temperature. Vygranenko *et al.* [28] applied long term gate bias stress on indium oxide TFT of mobility 3.3 $cm^2\ V^{-1}s^{-1}$ and I_{on}/I_{off} ~10^6. The results showed fast recovery of threshold voltage of threshold voltage of a relaxed device.

This thesis is structured into six main chapters as follow:

Chapter two presents an introduction to TFTs and several electrical measurements including the threshold voltage, field effect mobility, and I_{on}/I_{off}, and so on. Likewise, we discuss the related mathematical formulas of operating device based on linear and saturation regions. Also, we introduce some important topical information about organic and metal oxide semiconductors.

In chapter three we discuss strategies for controlling the morphology and crystalline microstructure of soluble (TIPS-PEN) as an organic small molecule OSM of interest in fabrication of OFET. The first part of the chapter concentrates on the effect of evaporation-induced flow on the drop cast dried film by controlling binary solvent composition. The effect on surface topography, roughness, and device mobility of the minor solvent (decane) composition will be discussed. The effect of adding insulating polystyrene to the blend for the TFT active layer is discussed in the second part of the chapter. The effect on crystal micro-structure, nano-scale surface topography, roughness, and device mobility as a function of polystyrene and solvent concentration is also presented. Also, we compare large scale optical microscopy images, nano-scale AFM images, and device mobility on both SiO_2 and poly (4-vinyl phenol) PVP surfaces.

Chapter four of the thesis concentrates on In_2O_3 as a metal oxide semiconductor TFTs. We present the main electrical and morphological properties of top contact (TC), bottom gate (BG) configuration of solution based indium oxide TFT (single and double spin coating). The primary aims of this study are three fold:

1. The study of device performance under gate bias stress and its effect on electrical properties of working transistor.
2. The use of Scanning Kelvin Probe Microscopy (SKPM) to map the local surface potential in In_2O_3 metal oxide semiconductor TFTs. We provide direct evidence for the diffusion of Al from drain electrode into the channel, which could prove to be a useful non-destructive probe of metal diffusion at electrodes. We also demonstrate the use of SKPM to detect trapped charge at the interface between the dielectric and the channel.
3. We discuss a new simple approach to detect metal diffusion at electrodes using conventional AFM with biased electrodes. This is backed up by modelling performed by colleagues at Swansea University.

In chapter five, we start with the fundamental principles of electrostatic force microscopy EFM and discuss its extension to a mode developed at Cardiff which involves measurements of the phase difference between the cantilever response and the driving signal as a function of applied tip bias.

The power of this approach has been considerably enhanced by the use of simple model in the analysis to correct for experimental time delay related to electrostatic charging. This has been the topic of a recently submitted patent application. An outline of the software developed for this is presented.

Finally in chapter six, the thesis ends with a summary of content and of the main conclusions, together with suggestions for future works in the field.

Chapter Two

Theoretical background

2.1 Introduction

Field effect transistors (FET) and circuits based on semiconductors other than silicon have experienced impressive developments in both performance and reliability. As present research moves toward areas like cheap manufacturing techniques and their application in large-volume, inexpensive disposable electronics. Solution deposition of organic and metal oxide semiconducting [29-31] materials as active layers in FET attract interest as a potential alternative of traditional silicon based technology. The main benefit is that layers of these materials can be deposited and patterned at low/room temperature by solution processing [32, 33], making them very suitable for low cost, easily produced, large area electronics and for inexpensive disposable electronics.

The semiconductor layer is not the only factor that determines the device performance. Device architecture, processing, and choice of electrodes are important as well. Moreover, the role of the gate dielectric and the charge trapping mechanism are also important.

In this chapter we will give some descriptions on the working principles of thin film transistors and the use of output and transfer characteristics to extract device parameters. Moreover, we will give a brief discussion on organic semiconductor (OS) and the process of charge transfer. Also, the factors that affect the charge transfer such as the HOMO and LUMO levels, impurities, and temperature are also mentioned. Finally, we conclude the chapter with a short discussion of the metal oxide semiconductor device.

2.2 Thin film transistors

Thin film transistors (TFT) are field effect transistor which can be made by deposition of a metallic electrode and thin film of semiconducting materials as well as dielectric layer on a supporting substrate. The deposited film which forms a conducting and active material can be a polymers[34-36], organic small molecules[37, 38], organic materials[39, 40], and metal oxide semiconductor[41, 42]. Many researchers have used different kinds of thin film (TF) deposition methods such as drop casting, spin coating, and inject print. Conventionally, the most common application of TFTs is in liquid crystal displays (LCD) -in television sets, mobile phones and computer monitors- to improve the image contrast and quality.

Recently, demands in the flat panel industry for high resolution, low power consumption, and large size flat panel displays necessitate using new semiconductor materials such as metal oxides. Metal oxides have high mobility, good homogeneity and are easily fabricated at room temperature. Crucial factors for improving device performance and stability include the quality and stability of the gate dielectric, suitable metallic electrodes, and control over threshold voltage changes. In this thesis we focused on two types of semiconductors as a thin film layer in field effect transistors (FET) devices. TIPS-PEN, a model small molecule organic semiconductor and indium oxide as a metal oxide semiconductor.

2.3 Thin film transistor structure

A variety of TFT structures can be prepared, with different configurations of the gate, source and drain electrodes. Each architecture is selected to optimise device performance for the target application. Figure 2.1 shows two such structures, with the top contact bottom gate (TC/BG) and with the bottom contact bottom gate (BC/BG) geometries. This choice affects the approach to deposition of the semiconductor layer. In the top contact structure the source (S) and drain (D) are deposited on top of the semiconductor layer (staggered structure).

However, for the bottom contact design, the source and drain electrodes are first deposited onto the gate (G) dielectric, followed by deposition of the semiconductor

film. This design are described as a coplanar structure because the source and drain are in contact with the dielectric material, being coplanar with the conducting channel. The staggered configuration provides a larger area for charge injection into the semiconductor than for the coplanar geometry, resulting in lower contact resistance and better device performance[43] as the charge injection process to the interface probably occurs across the whole contact surface area rather than the edge of contact as in the coplanar geometry.

Figure 2.1: Basic structures for thin film transistor presenting top contact bottom gate (left hand side) and bottom gate bottom contact (right hand side).

The bottom gate geometry is generally easier to construct. However, the semiconductor film remains open to the ambient atmosphere and is susceptible to the negative impact of the atmospheric factors such as humidity, oxygen and contamination. Therefore, this configuration often needs a passivation layer to avoid ambient damage effect and ensure long term stability. In the bottom gate coplanar configuration the effect of increased contact resistance is present due to less than optimal electrode/semiconductor interface and the parasitic capacitance between electrodes and gate which slow down TFTs. In contrast, the staggered bottom gate has the advantage of better quality of electrode/semiconductor interface which in turn leads to enhanced charge injection.

In this work, a top-contact (TC/BG) configuration was employed in all devices due to its lower contact resistance compared to that with a bottom-contact design. As outlined above, the lower contact resistance in this configuration is associated with the increased effective contact area [43, 44] as the charge injection to the interface may happen along the whole surface area of the contact rather than solely at the edge of the contact as with the coplanar configuration. Furthermore, since carriers accumulate at the insulator interface, there is a little charge injection / extraction at the top of the source contact Figure 2.2

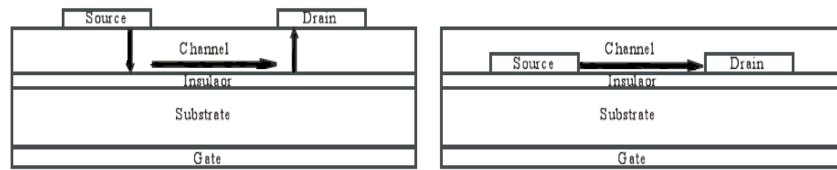


Figure 2.2: The arrows in the diagrams refers to the flow direction of current from the source to the drain.

On the other hand, evaporation of the top contact can lead to poor electrode-active layer interface quality between the metal and the semiconductor causing significant degradation of electrical of electrical performance [45]. This is a particular problem for organic semiconductor devices.

2.4 Basic operation of TFT

TFTs require the three basic components (S/D and G) as mentioned above. The charge injecting electrode source is usually grounded and the potential applied to both drain and gate. The semiconducting channel between the source and drain electrode is isolated from the gate electrode by a high quality dielectric material. Applying a voltage to the gate terminal generates a polarization of the dielectric, leading to a charge distribution of the same polarity as the gate potential on the dielectric surface and thin layer of mobile charge of opposite polarity within the semiconducting layer at the interface between semiconductor and insulator. This thin layer of mobile charge is the accumulation layer.

The amount of mobile charge in the accumulation layer depends on the value of gate voltage and on the capacitance of gate dielectric [46]. This mobile charge in the accumulation layer could be either electrons or holes depending on the gate bias polarity, their relative concentration and the majority carrier. Moreover, not all induced charges are mobile because the deep traps have to be filled first before additionally produced charges become mobile. These trapped charges are the origin of the threshold voltage (V_{th}). In other words, the mobile charges which contribute to the S-D current are produced after applying the effective gate bias ($V_{eff} = V_g - V_{th}$).

Figure 2.3(a) shows a top contact-bottom gate TFT with n-type semiconductor and the corresponding band diagram with different gate biasing conditions. The device will be in an equilibrium state with no gate bias Figure 2.3b. The next figure 2.3c on the right hand side presents a band diagram with a negative gate bias. Negative gate bias causes depletion of electrons in the channel region. The creation of such a depletion regions reduce the channel conductance. In contrast, when the positive bias applied to the gate terminal the mobile electrons accumulate at the interface of SC/dielectric which results in an accumulation region. In this case the device has a high conductivity and low resistance which results in a noticeable current between source and drain.

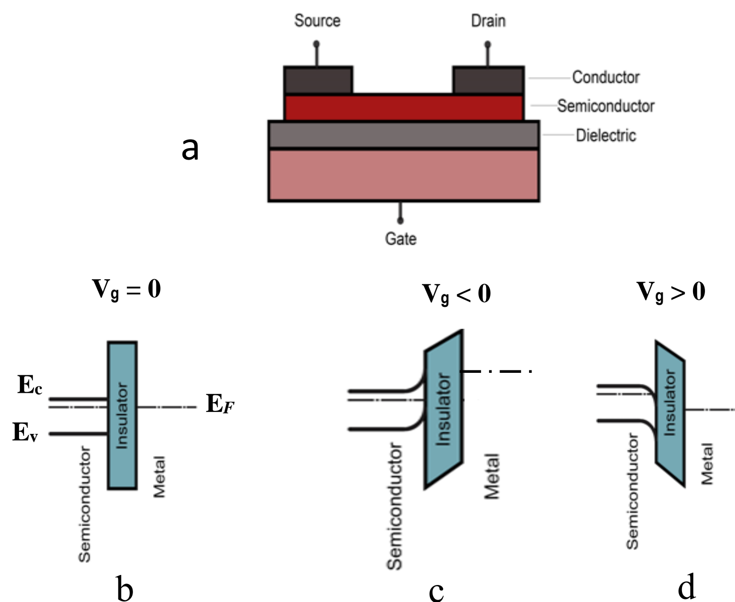


Figure 2.3: (a) TFT structure and corresponding gate biasing conditions. (b) The equilibrium condition. (c) $V_g < 0$V. (d) $V_g > 0$V

When no S-D bias is applied the charge concentration at the channel region is homogenous and uniform. When the a small bias is applied across S-D ($V_d << V_g$) a linear gradient of charge density is established in the channel region and the drain current is linearly proportional with drain potential V(x) from the injecting source (at x =0) to the extracting drain ($x = L$), demonstrating Ohmic behaviour.

As the source-drain bias is increased, a point is reached, approximately at $V_d = V_g - V_{th}$, at which there is depletion of carrier in the region close to the drain electrode. At this ***pinch off*** point the drain current stop increasing with increased V_d, usually referred to as the onset of saturation region. Further increasing of the source-drain bias leads to an expansion of the depletion region, shortening of the effective channel length and no current increase, referred to as the saturation region of the transistor.

If the channel is p-type material, as in the majority of organic semiconductors, then we need to apply a negative bias to the gate terminal. An electric field is generated across the insulator and OS close to the interface, which leads to the departure from equilibrium state. This departure from equilibrium by electric field is compensated for by a realignment of Fermi levels for both organic semiconductor and gate, and a resultant energy band bending near the interface. The band bending allows creation of accumulation layer of holes injected from source Figure 2.4.

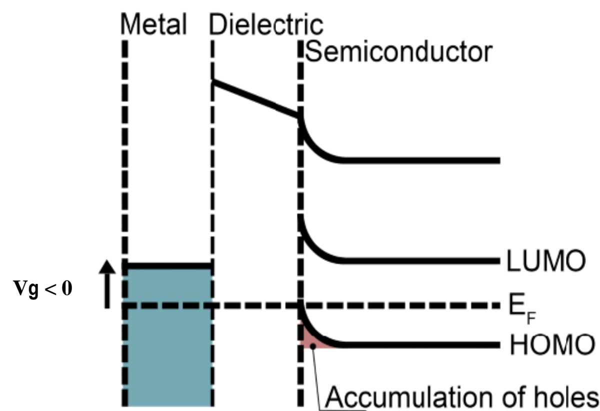


Figure 2.4: Application of a negative gate bias on p-type OS. The E_F of metal raises by gate bias (arrow) and leads to OS band to bend as they re-equilibrate [adopted from [47]].

2.5 Basic theory of TFT characteristics

The gradual channel model is the most commonly applied model to describe different regimes of the current-voltage characteristic of a TFT. In the gradual channel approximation, the electric field between source-gate (perpendicular to the current flow)

must be much larger than the field between source-drain (lateral field). Hence, all charges are transported on the semiconductor/dielectric interface and one dimensional potential distribution in the channel region can be applied [48]. According to this ideal condition, the accumulated charge density in the interface at a spatial position *x* follows the potential profile along the channel.

When the gate bias is higher than the threshold voltage, the transferred charge per unit area at the source electrode from the gate is

$$c_i\left(V_g - V_{th}\right) \tag{2.1}$$

where c_i is the capacitance per unit area. But the induced charge density q_{mob} depends on the position along the channel. Therefore, the above equation is modified to

$$q_{mob} = c_i \left(V_g - V_{th} - V(x)\right) \tag{2.2}$$

The drain current I_d is given by [46]

$$I_d = \mu W q_{mob} E_x$$

where *W*, *μ*, and E_x are the channel width, carrier mobility and electric field respectively. By substituting $\frac{dV}{dx}$ for E_x and substituting into equation (2.2), the drain current becomes

$$I_d\, dx = \mu W\, C_i \left(V_g - V_{th} - V(x)\right) dV \tag{2.3}$$

By integrating the last equation from *x* = 0 (source position) to *x* =*L* (drain) and corresponding values for potential:

$$\int_0^L I_d\, dx = \int_0^{V_d} \mu W\, C_i \left(V_g - V_{th} - V(x)\right) dV \tag{2.4}$$

$$I_d = \frac{\mu W\, C_i}{L}\left[\left(V_g - V_{th}\right)V_d - \frac{1}{2}\, V_d^2\right] \tag{2.5}$$

Equation (2.5) shows that for certain values of gate bias the current increases with V_d , and it reaches its maximum value at $V_d = V_g - V_{th}$

If the voltage applied between source and drain is much smaller than the difference between gate and threshold voltage, the above equation can be simplified to

$$I_d = \frac{\mu W C_i}{L}\left[\left(V_g - V_{th}\right)V_d\right] \tag{2.6}$$

As we see, the drain current is directly proportional to the drain voltage and therefore describes the linear regime of the output characteristic. However, when the applied bias between source and drain is greater than $\left(V_g - V_{th}\right)$, equation (2.5) defines the saturation regime with

$$I_d = \frac{\mu W C_i}{2L}\left[\left(V_g - V_{th}\right)^2\right] \tag{2.7}$$

According to the equations (2.6) and (2.7) the carrier mobility μ is an important parameter because it defines the drift velocity of the carriers in an electric field or how fast the carriers move across semiconductor depending on applied voltage.

2.6 The main components of a TFT

In this section we discuss briefly the role of the main components forming TFT which helps to get an optimum electrical performance of the device.

2.6.1 The substrate/ gate: A wafer of highly n- doped Si is the most common substrate for TC/BG or BC/BG thin film transistors. Highly-doped Si can be used as a conducting gate using the oxide as a dielectric. In this way the step of adding a conducting gate above the substrate can be avoided. The low resistivity of this gate electrode is very important for high speed and low power consumption as it minimize the capacitance (RC) time constant.

2.6.2 Dielectric layer :The performance of a TFT device depends to a great extent on the nature of the insulator that separates the semiconductor from the gate. The surface properties (morphology) of the dielectric determine the distribution and

crystallization of the semiconductor film deposited onto it. Silicon dioxide (SiO_2) has been used for a long time as a dielectric material in TFT device fabrication but because of size reduction, the demands of minimizing leakage current has become more challenging. An increase of the leakage current leads to higher power consumption. Therefore, materials with large values of the dielectric constant are preferable [49] . The dielectric capacitance is:

$$c_i = \frac{\varepsilon_o k}{d} A \tag{2.8}$$

where c_i, ε_o, k , and d are insulator capacitance, vacuum permittivity, dielectric constant and thickness respectively. Although the dielectric constant is directly proportional to capacitance and the charge density in the channel, high dielectric constant materials generally have a lower band gaps and high electron affinities (high affinity leads to smaller conduction band discontinuity and smaller carrier injection barrier), causing low break down voltage [49] . Therefore, when high dielectric insulators are used, low gate voltages must be employed. Figure 2.5 shows the change of band gap as a function of *k* for the gate oxide. Since the band gap is roughly inversely proportional to *k*, gate oxides with relatively low *k*- value must be considered[50].

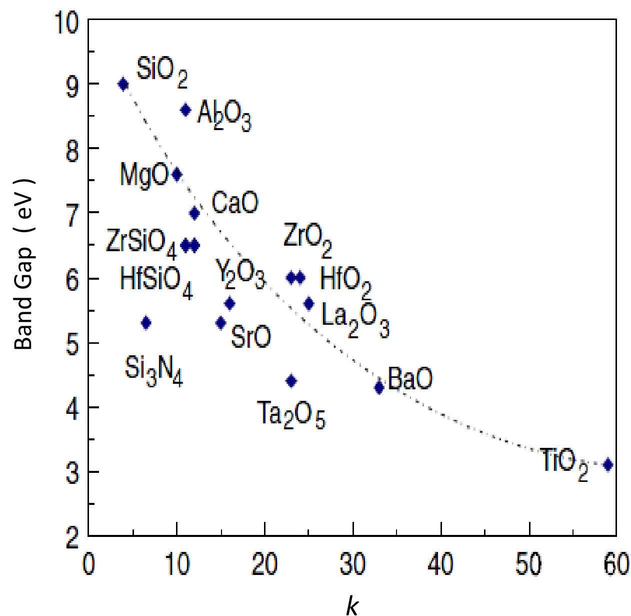


Figure 2.5: Dielectric constant versus band gap of some gate oxides [50]

The roughness of the dielectric also has a profound effect, because the accumulation layer occupies only a few nm thickness at the SC/dielectric interface, so the smoothness of this interface is very important. As the rough surface causes more charge traps, the interface must be well defined to avoid worsening of charge transport along the channel and limiting device performance.

2.6.3 Source and drain electrode: The deposition of metallic electrodes (above or below the semiconductor) depends on the nature of the electrode material. Vacuum deposition through shadow masks is a common technique of deposition of insoluble metallic contacts like gold or aluminium. The length and width of the channel is also specified at this electrode deposition stage. The source and drain are in direct contact with the semiconductor, so they play an important role in device operation. The reduction of contact resistance, minimizing of metal oxidation and diffusion of metallic particles beyond contacts during the deposition process all have a crucial effect in improving device performance. Furthermore, metallic contacts should be selected in such way that gives a good energy level alignment between the semiconductor and the Fermi level of the S/D electrodes, which relates to the work function.

The work function of metal is the minimum energy required to remove an electron from its surface. In a metal the work function and ionization energy are same [51]. We can estimate the contact suitability by comparing the metal/semiconductor work functions. Table1.1 lists the work functions for some metals.

In p-type organic semiconductors, a metal like gold with high work function (5.3 eV) is favoured for hole injection. However, for metal oxide semiconductors like indium oxide, aluminium (4.08 eV) is a good contact for electron injection.

Metal	Work function (eV)
Au	5.3
Al	4.08
Cd	4.07
Cu	4.7
Pt	5.37
Co	5.0
C	4.6

Table 1.1: The work functions for some metallic elements.

2.7 Electrical characterization of TFTs

Two standard electrical measurements are commonly used to characterize the device performance, transfer and output characteristics.

2.7.1 Transfer characteristic

The transfer scan is obtained by scanning the gate bias from off to the on region whilst keeping the drain voltage constant. The manner of transfer curve plotting depends on the parameter one wishes to extract from it. If the device mobility is needed the square root of drain current should be plotted against gate bias.

In addition to the channel mobility many device metrics also can be extracted from transfer characteristic. These include the threshold voltage (V_{th}), drain current on/off ratio, turn on voltage (V_{on}), and sub-threshold swing (*S.S.* The threshold voltage which is indicative of drain current onset [52, 53] can be extracted from transfer curve in the saturation region on $I_d^{1/2}$ vs V_g (Figure 4.4d) characteristic plot by extrapolating

the linear portion down to the V_g axis. The semi-log plot of drain current can emphasise the turn on point, where the current start to increase dramatically.

The sub-threshold swing ($S.S$) and current I_{on}/I_{off} ratio are estimated also from a semi-log plot of transfer curve (Figure 2.6) at high V_d ($V_d >> V_g$). The inverse of maximum slope of semi-log curve of drain current is determines the value of sub-threshold swing ($S.S$) :

$$S.S = \left(\frac{\partial \log I_d}{\partial V_g}\right)^{-1} \tag{2.9}$$

Typically the value of $S.S$ is less than 1 V/decade and representing how efficiently the device turn on. A small value of S.S is desirable because it shows the fast transition from an off to an on state. The I_{on}/I_{off} is calculated by measuring the ratio of the highest or maximum ("on" current) and lowest or minimum ("off" current) drain current values.

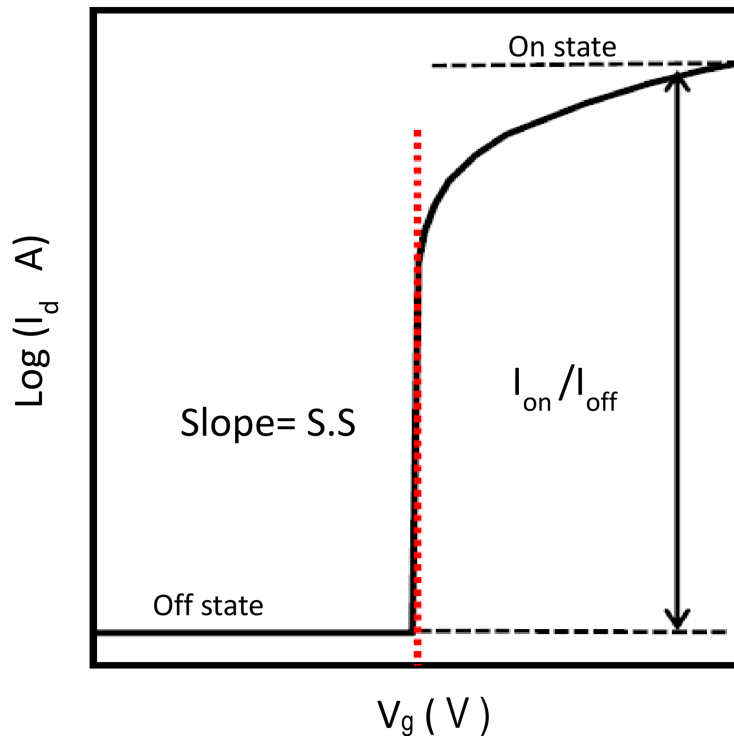


Figure 2.6: Schematic diagram for definition of subthreshold slope and drain current I_{on}/I_{off}

2.7.2 Output characteristic

The device output curve is obtained when the drain current is measured as a function of the drain voltage for a discrete gate bias. An applied gate voltage V_g changes the drain current Id versus V_d curve shifts according to Equation (2.5). Accordingly, the family of curves for different values of V_g can be generated.

Some analytical models [48, 54, 55] have been proposed to describe the current – voltage characteristics. However, the gradual channel approximation is the common model which describes TFT operation in different regimes.

The relative value of V_d compared to V_g describes the device working regime whether in linear or saturation. Practically, the output curves can be obtained by measuring the drain current as a function of drain voltage for different gate biases. Figure 2.7 shows typical output characteristic for n-type transistor.

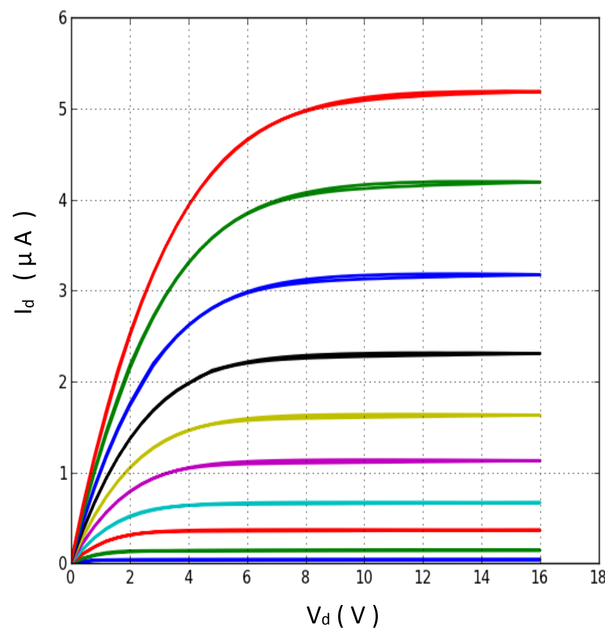


Figure 2.7: Typical output curves for metal oxide TFT with V_g = 1 to 10 (step 1V).

When the drain voltage is sufficiently small relative to V_g the TFT can be considered to be working in the linear regime as in Equation 2.6. The transistor channel acts like resistor. Such behaviour expressed as:

$$I_d = g\, V_d \tag{2.10}$$

where g is the channel conductance given by

$$g = \frac{W\,\mu}{L}\, Q \tag{2.11}$$

Q is the sheet of charge density in accumulation layer and depends on the gate voltage. In the linear regime we can also extract the transconductance g_m from the differentiation of Equation 2.6 with respect to V_g

$$g_m = \frac{\partial I_d}{\partial V_g} = \frac{W\,\mu\,k\,\varepsilon_o}{L\,d}\, V_d \tag{2.12}$$

where ε_o, k are the permittivity of free space and the relative permittivity of the gate insulator respectively. Likewise, it is obvious from Figure 2.7 and at the knee (onset of drain current saturation) $V_d = (V_g - V_{th})$ the drain current become substantially constant and no longer depends on drain voltage. The transconductance g_m at saturation regime and by using Equation 2.7 is

$$g_m = \frac{\partial I_d}{\partial V_g} = \frac{W\,\mu\,k\,\varepsilon_o}{L\,d}\,(V_g - V_{th}) \tag{2.13}$$

2.8 Contact resistance (CR)

In TFTs, in addition to the channel resistance (R_{ch}), the contact resistance (Figure 2.8) often has equally role on limiting the device performance especially in OTFT where the CR is large. The contribution of the contact resistance to the total device resistance become larger as the device channel spacing becomes shorter. In the other words, the device performance in a short channel length is degraded because the increasing effect of the metal/semiconductor interface[43, 56].

The potential drops due to the CR at the edge of S/D contacts are not negligible compared to the drops across the channel. Kelvin probe measurements are very useful

technique for confirming potential drops and study the potential profiles across the channel[57].

Figure 2.8: Schematic diagram for Top contact bottom gate TFT describing channel and interface resistance (left arrow).

The transmission line method (TLM) is a common way used for the evaluation of CR in organic thin film transistors. Unfortunately, because of large parameter variations (such as mobility and threshold voltage) in organic thin film transistor (OTFT) which limits uses of TLM to some extent. This issues leads to deviation of extracted contact resistance especially at low gate voltage[58].

The transistor channel in the linear regime could be regarded as a uniform resistance controlled by gate voltage[59], then from (6) the channel resistance is:

$$R_{ch} = \frac{L}{\mu\, W(V_g - V_{th})C_i} \tag{2.14}$$

Due to contact resistance R_c located between contacts and the channel the total resistance in the linear region becomes

$$R_{tot} = R_{ch} + R_c = \frac{L}{\mu\, W(V_g - V_{th})C_i} + R_c \tag{2.15}$$

2.9 Organic semiconductor

The discovery of electrical conduction in organic materials goes back to a century ago with the observation of photo conductivity in anthracene crystal[60]. Chiang *et al.* [61] in their work on polyacytylene invented a new class of highly conducting polymers and they won a Noble prize in chemistry in 2000. This important invention opened up a new road toward organic electronics, and a wide range of studies on conducting and semiconducting properties in organic materials. The majority of early OFETs was fabricated by the deposition of polymer films via drop casting or spin coating methods with rather low carrier mobility $10^{-5} – 10^{-4}$ cm^2 V^{-1}s^{-1}. On the other hand, the remarkable observation on using of organic small molecules α-sexithiophene instead of polymers in OFET led to higher carrier mobility of about 10^{-3} cm^2 V^{-1}s^{-1} and on/off current ratio about 10^5 [62]. Another positive side to using small molecules is that the charge transport process can be controlled by modifying the molecular parameters and deposition conditions. OFETs based on pentacene with mobilities larger than 0.5 cm^2 V^{-1}s^{-1} were reported almost two decades ago [14] . Later, a pentacene based devices was reported to have higher mobility [63] but the majority of other groups could only obtain mobilities of order of 1 cm^2 V^{-1}s^{-1}.

Generally, the polymeric organic semiconductors have good film formation properties and processing. But the measured mobility is rather small or requires high temperature to reach a suitable value. Poly(3-hexylthiophene) P3HT and poly(p-phenylenevinylene) PPV are two well-known examples of polymer semiconductors. In contrast, small organic molecules have better mobilities but poor film formation properties. Pentacene is a classic example of organic small molecule OSM.

Unlike the conduction properties of inorganic semiconductor where charge transport occurs by excitation between bands, conduction in organic materials occur by charge hopping between the delocalized π molecular orbitals. The common characteristic of these compounds is a series of alternating single and double bonds, either as closed benzene rings or as a linear chain. Carbon atom with the ground state configuration $1s^2\ 2\ s^1\ 2p_x^1\ 2p_y^1\ 2p_z^1$ can form two types of bonds between each others. The first one is σ strong bond and the second one is π weak bond. The strong σ bond is formed by the overlap of hybridized sp^2 orbitals, and the π bond forms by overlapping of

unhybridized $2p_z$ orbitals. The tightly bound electrons in σ bond always remain between carbon atoms, unlike the delocalized π electrons which have some degrees of freedom to move between adjacent molecules and define the electronic capabilities of organic semiconductor OS. For a benzene ring where σ bonds give the mutual position of atoms and its planar ring shape , and overlapped p-orbitals create delocalized π electron clouds Figure 2.9 (above and below the plan of benzene). The formation of delocalized molecular orbitals defines the boundaries of molecular electronic levels i.e the highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO). These two levels determine the electrical and optical properties of OS.

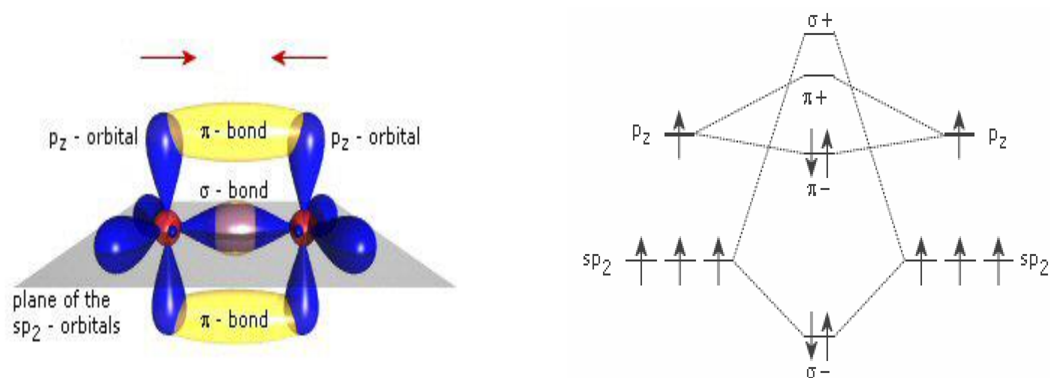


Figure 2.9: Two connected carbon atom with its orbitals (left), and energy levels of occupied and unoccupied levels for σ and π levels [64].

The states of π–electron clouds provides the probability for charge transport either by hoping mechanism, or by more band like transport if there is a significant overlapping of π - bonds between neighbouring molecules, in a manner closer to a crystalline inorganic semiconductor.

Depending on the molecular structure, the HOMO and LUMO separation of OS is roughly about 2-5 eV which is significantly larger than typical bandgaps in their inorganic counterparts. Therefore the number of thermally excited electrons (holes) is extremely low and the conduction process requires the addition of some mobile charges. This can be done by charge injection from metallic electrodes or by optical excitation.

2.10 Charge transfer in OS

Although, a comprehensive theory of charge transport in OS has not been attained, one can distinguish between disordered OS like amorphous polymers and highly ordered organic single crystals. In the first category charge hops between well-defined states. In highly ordered organic materials (crystalline) such as tetracene and pentacene the experimental data points to band-like transport between delocalized states[46, 65].

The energy bands of crystalline solids can be established from the energy levels of a single atom. When two atoms are brought close together the energy levels splits as a result of overlapping of molecular orbitals. Then by adding more and more atoms to a regular lattice leads to further splits of energy levels into two continuous bands separated by an energy gap. The lower band is a valence band where the electrons bound to atom, whilst the upper band is a conduction band where the electrons are free to move. The magnitude of the energy gap, the position of the Fermi level (E_F), and the electron distribution in these bands determine the electrical properties of metal, semiconductor, and insulators. In a metal, there is no energy gap and the Fermi level is in the conduction band which means availability of free electrons to carry current when a bias is applied. However, in a semiconductor E_F is within the energy gap so that an electron must be given more energy to reach the conduction band and move freely under bias.

In conducting organic materials the situation is closely related to that described above. All conjugated molecules have regions of overlapping p-orbitals allowing partial delocalization of π-electrons. Accordingly, all these molecules have occupied bonding orbitals and unoccupied antibonding orbitals. The highest occupied molecular orbital (HOMO) and lowest unoccupied molecular orbital (LUMO) is separated by the energy gap which depends on conjugation length (the number of coplanar rings determines the conjugation length - the longer the conjugation length, the lower the separation between adjacent energy levels, and the longer the absorption wavelength). Increasing conjugation length leads to increased electrons delocalization, broadening of the bands and reduction of the energy gap. Figure 2.10 shows the experimentally determined energy gap with the number of benzene rings for naphthalene (2- bonded benzene rings) which is 4.35 eV to pentacene (5- bonded benzene rings) which is 1.9 eV. The reduction

of energy gap with conjugation length certainly has some limit but the explanation of this situation is beyond the scope of this thesis.

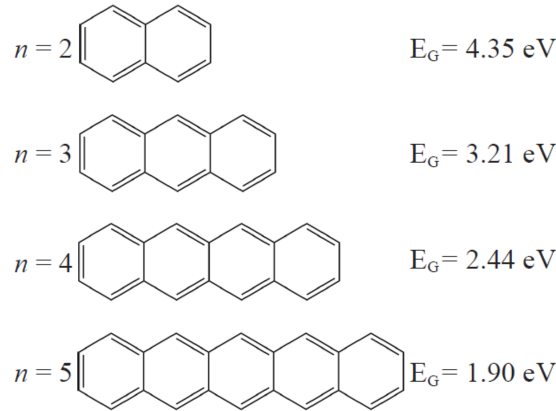


Figure 2.10: Energy gap dependence on conjugation length[66].

In the band model the mobility is controlled by either phonon or impurity scattering. The scattering cross section increases with temperature-so the mobility can be express by:

$$\mu \propto T^{-n} \tag{2.16}$$

For pentacene, n is of the order of 0.27 to 0.32 [67].

In the hoping model, the electrical conductivity is described by phonon assisted charge transport tunnelling from site to site over a potential barrier which separates two molecular or ionic sites. Likewise, the charge carriers are highly localized and the carriers mean free path is less than the separation between two adjacent neighbour molecules. For the hopping process with highly localized carriers the mobility is temperature T and activation energy E dependent according to:

$$\mu \propto \nu \exp\left(-E/k_B T\right) \tag{2.17}$$

where ν, k_B are the lattice phonon frequency and Boltzmann's constant respectively. The term $\nu \exp\left(-E/k_B T\right)$ represents the hopping probability from an initial to the final site. The above equation shows mobility increases with temperature, as the probability of overcoming the activation energy barrier increase.

2.11 Factors affecting charge transport in OS

Efficient transport of charges requires charge transfer from molecule to molecule and not be trapped or scattered [68]. Many factors influenced charge transport in OS including HOMO and LUMO level relative to the metal work function, molecular structure and packing, presence of impurity, temperature. It would be formidable task to try to discuss the detailed effects of all factors on charge transport. Therefore, we try to focus on some of them.

2.11.1 HOMO and LUMO level

The relative position of HOMO and LUMO levels with respect to the electrodes work function Fermi energy is very important because it determines energy barriers to charge injection into the semiconductor. The hole injection barrier is the difference between the electrode work function and the ionization energy of organic material, and the electron injection barrier is the difference between the metal work function and electron affinity of the organic film[69].

Selection of OS with proper HOMO and LUMO level relative to electrode can minimize the resulting e resistance. High work function material such as gold are used for efficient hole injection and lower work function metals like aluminium for electron injection. Figure 2.11 shows charge injection into the conduction channel. In p-type organic thin film transistor OTFT, the holes are injected into the HOMO level while in n-type OTFT the electron are injected into the LUMO. Figure 2.12 illustrates a comparison between metal work functions and the HOMO and LUMO position for different organic materials.

Considering a grounded source and applying a positive bias to the gate in pentacene OTFT, accumulation of electrons at the semiconductor/dielectric (at semiconductor side) interface occur. Since the Fermi level of Au is far from the LUMO of pentacene a large barrier produced, so the probability of electron injection is very small. In contrast, applying a negative gate bias leads to accumulation of holes at the semiconductor/ insulator and the holes are easily injected to the HOMO because the Fermi level of gold is very close to that level as indicated in the figure. Therefore, a significant hole current will pass through transistor channel if a bias applied between S/D.

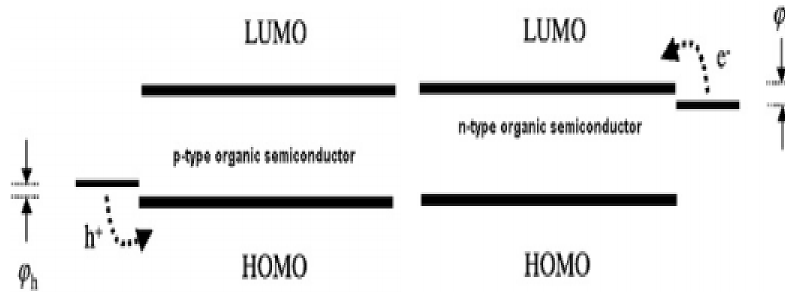


Figure 2.11: Energy level diagram of charge injection process in OS [70].

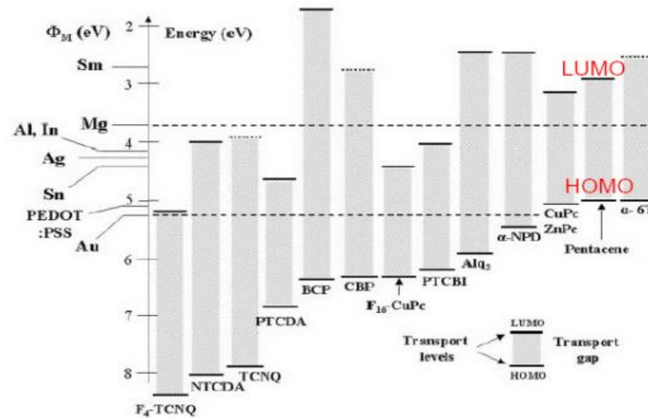


Figure 2.12: Metal work functions relative to HOMO and LUMO for different organic material[69].In the ideal device, the source Fermi level should be very close to the HOMO level of the semiconductor. If the difference between metal work function and HOMO level φ - $E_{HOMO} \leq 0.3$ then, the charges can move freely toward SC channel with minimum resistance. This kind of contact is known as an Ohmic contact.

2.11.2 Molecular structure and packing

The molecular structure is regarded as one of the most important factors for considering device performance. Highly crystalline OS which maximize π-orbital overlap have increased mobility. Since the degree of overlap is thus dependent on the crystal packing, charge transfer rates can depend on the molecular structure [68]. In the majority of the cases, π -conjugated crystalline molecules arrange themselves into a layered herringbone pattern. Such packing gives 2D transport within the stacked organic layers

[71]. The 2D transport behaviour of most organic single crystals (and thin films) has an important implication in OFET because it requires π-stacking direction to be in the plane of the source and drain in order to enhance the current flow through the conducting channel. Highly ordered with high degree of crystallization of organic semiconductor (such as TIPS-PEN where it has 2D brickwork configuration) should be aimed to guarantee device of good performance (Figure 2.13).

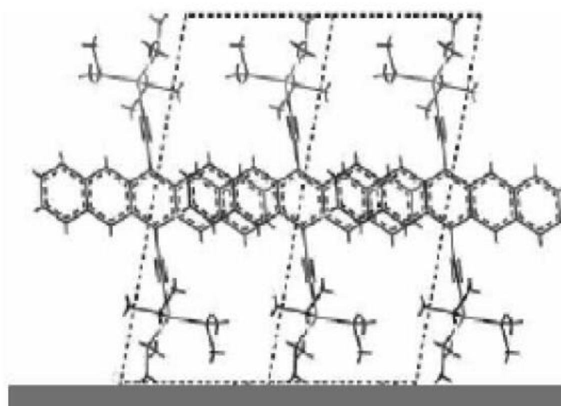


Figure 2.13: Highly ordered TIPS-PEN molecules on SiO_2 substrate. Well distributed molecules and close packing of π- orbitals in conducting pentacene are favoured for desired device.

2.11.3 Material impurities

The existence of impurities leads to disruption of crystal structure and degrades performance. Impurities could be compounds that have slightly different chemical structure which appear at low concentration in the host material. Jurchescu *et al.* [72] reported that the main impurities in pentacene single crystal is the pentacene –quinone molecules (Figure 2.14) are presented at concentration around 0.7%. Purification steps reduce this concentration to 0.07% , reducing the number of traps and improving the hole mobility from 35 $cm^2\ V^{-1}s^{-1}$ at room temperature to 58 $cm^2\ V^{-1}s^{-1}$ at 227 K. Jurchescu and co-worker found 6,13 pentacene –quinone is a dominant chemical impurities in pentacene crystal and the reduction of impurities by factor of five caused decreasing of number of traps by two order of magnitude. Traps occur when the existing impurities have lower conduction than the host semiconductor.

An important effect of traps is shifting of threshold voltage toward higher voltage. This shifting of V_{th} leads to an increase of required voltage to turn on the device and consequently larger power consumption.

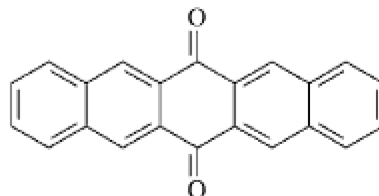


Figure 2.14: Chemical structure of impurities found in pentacene [72].

2.12 Semiconductor Materials investigated

We now introduce the two material systems studied in this thesis: the small molecule semiconductor TIPS-PEN and metal oxide In_2O_3 .

2.12.1 Organic small molecules

Pentacene, is a p-type organic small molecule consisting of five fused benzene rings as illustrated in Figure 2.10. It showed some of highest mobility detected in organic semiconductor [73]. Despite its promising electrical properties, pentacene has an edge to face herringbone structure that limits efficient charge transport because π-π stacking does not occur in this structure. The position 6 and 13 of pentacene molecule (Figure 1.3) are more reactive and pentacene is not soluble in most organic solvents. When pentacene is exposed to both oxygen and ultraviolet light the photo stimulated electron can transfer to oxygen and incubates formation of oxidized pentacene[74]. This impurity causes defects in the molecular crystal and states of traps in TFT which reduces charge transport as mentioned before. The deposition rate has also strong effects on pentacene film morphology. AFM of pentacene film showed more ordered crystalline grains when lower deposition rate and higher substrate temperature (30-90 ^{o}C) are used, the deposition rate 0.4A^{o}/s showed high performance pentacene device.

However, very low deposition rate (< 0.1 A°/s) not indicated better device performance but often the opposite[75].

The addition of solubilising groups to the pentacene core can make this material solution processable and maintains the electronic properties of mother pentacene. One notable example of substituent pentacene with good air stability is 6,13 bis (triisopropylsilylethynel)pentacene TIPS-Pentacene (TIPS-PEN) which is soluble in common organic solvents. The substituents in position 6 and 13 of pentacene have an effect of supporting the most sensitive and reactive part of the molecule [74]. Figure 1.3 shows the molecular structure of TIPS-PEN.

The second observed effect of added side-group is the molecular packing which leads to improvements in the electronic properties. In this functionalized material, the bulky group substitution on the central aromatic ring disrupts edge to face interaction and prevents the adoption of typical herringbone crystalline packing motif in crystal [63, 76].

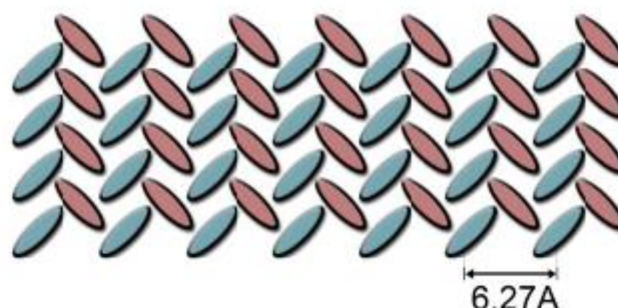


Figure 2.15: Edge to face herringbone structure

The strong triple carbon –carbon bond serves to hold the substituents away from the benzene planes allowing neighbouring molecules to stack in face to face orientation which results a striking improvements in stability, solubility, and electrical properties [16, 77]. Furthermore, because of these cofacial face to face arrangements, the interplanar spacing of aromatic rings reduced to 3.43 A° compared with 6.27 A° (Figure 2.15) for unsubstituent pentacene. TIPS-PEN packs in the two dimensional ***Brickwork arrangements*** that favour π-π stacking and increases carrier mobility by allowing transport to take place in more than one direction Figure 2.16.

Moreover, any tiny changes of molecular structure of the constituents in bulky side groups leads to dramatic changes in the molecular stacking and intermolecular interactions in solid state [78].

Figure 2.16: Two dimensional Brickwork arrangements. The arrow refers to the direction of charge transport which can take place.

Hence, depending on the size of R_o (the bulky group - Figure 1.3) the molecular packing takes different arrangements. In the case when R_o is smaller than half of the pentacene core the molecules packs as a 1D ***Slip stack*** form.

Figure 2.17: Face to face 1D ***slipped stack*** arrangements. Again the arrow refers to the charge transport which can take place only in one direction.

On the other hand, when R_o is close to the half of pentacene core the molecular configuration is brickwork arrangements where the molecules can pack in such a way that the charge transport takes two different directions in the solid. The molecular brickwork packing is the preferred configuration because the carriers can transport in the conducting channel of TFT more easily and independently on the direction of crystal growth. Finally for bigger R_o the observed molecular configuration is the herringbone which is not the favoured molecular arrangements.

In addition to the previously noted effects, adding the side group to the pentacene has a positive role on the HOMO and LUMO position in its molecular orbital diagram [79].

The adding of TIPS to the side 6 and 13 of pentacene core leads to lower the HOMO level from 4.96 to 5.11 eV. The last effect is a factor of major importance because as we mentioned in section 2.11.1 the position of HOMO level with respect to the metallic work function in pentacene organic semiconductor has an advantage in charge injection process. Assuming gold electrode with work function 5.1-5.3 eV the injection of hole from source to the conducting TIPS-PEN channel is favoured because the injected carrier require minimum energetic barrier.

In summary, the addition of side group to the position 6, 13 of pentacene core not only improves solubility and stability but also the π-stacking, molecular ordering and energy band lineup. The impact of these effects appear as a positive side in electrical properties as well till TIPS-PEN today is regarded as a model organic small molecule semiconductor. These reasons made us to consider TIPS-PEN as a reference starting material of the thesis.

2.12.2 Metal oxide semiconductor

Transparent oxide semiconductors are classified into two groups: polycrystalline and amorphous oxide semiconductors. Generally these materials have large bandgaps and wide controllability of carrier concentrations that make them promising candidate for transparent TFT applications. Polycrystalline thin film transistors show relatively high field-effect mobilities but the polycrystalline grain boundaries deteriorate the reproducibility and uniformity of the device characteristics [80]. However, amorphous oxide semiconductor TFTs have good uniformity and reasonably high field-effect mobilities even when deposited at room temperature on plastic substrates [10].

The electronic properties of metal oxide materials are highly dependent on their band structure and metal-oxide orbital interactions strongly influence electron and hole conduction for a given species. In the classic covalent band material picture of group IV semiconductor such as Si the conduction band minimum (CBM) and valence band maximum (VBM) are made from anti-bonding state sp^3 σ^* and bonding sp^3 σ states of hybridized Si orbital, its band gap being the splitting between the σ^* and σ levels [32, 81]. However, the metal oxide semiconductors such as In_2O_3 and ZnO are generally valence compounds with a high degree of ionicity in their chemical bonding. Such

ionicity produce an electronic structure that differs from that of purely covalent structure[32]. In such representative wide- band gap materials the VBM and CBM are produced from metal ns and oxide *2p* orbitals contributions[82] leading to a dispersive CBM and a localized VBM. This can explain the small electronic effective mass, large electron mobility and the predominant n-type conductivity found in the majority of metal-oxide semiconductors.

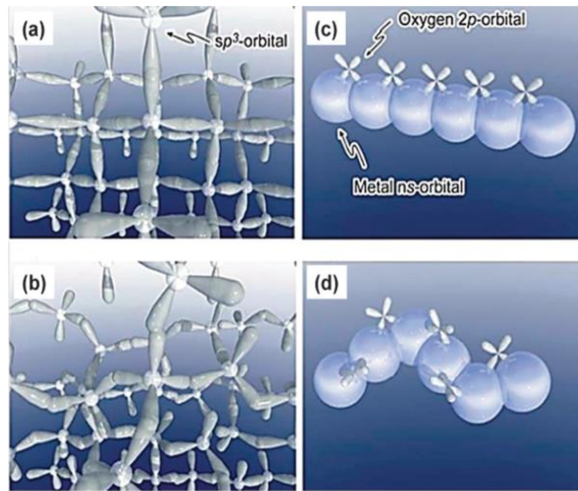


Figure 2.18: Electron transport and conduction path in [a] crystalline Silicon [b] amorphous Silicon [c] crystalline metal oxide [d] amorphous metal oxide [10].

Figure 2.18 depicts the disordered nature of amorphous silicon, which results in much poorer charge transport properties than in its crystalline form. This disordered structure in amorphous Si also leads to localized trap like states below CBM and above the VBM, leading to low mobility of charge carriers. In contrast, the large metal ns states in oxide materials (c and d) remain energetically close to each other in ordered and amorphous cases allowing effective electron transport and large carrier mobilities.

Since the large band gap of metal –oxide materials prevents the thermal generation of carriers, a significant dopant concentration is required to improve the conductivity. In metal oxides, dopant arise from their non-stochiometry-: for instance, the conductivity of In_2O_3 and ZnO can be increased if the materials are grown under metal rich and oxygen deficient conditions.

Chapter Three

Morphology control strategies for solution processed TIPS-PEN thin filmS

3.1 Introduction

Pentacene is a high performance organic small molecule composed of five fused benzene rings. This compound is unstable in air and has limited solubility. The solubility of pentacene was got over by adding 6,13 silyl group making this molecule soluble in the common organic solvents. Anthony *et al.* [16] have reported that 6,13-bis(triisopropylsilylethynyl) (TIPS) pentacene (TIPS-PEN) is soluble in majority organic solvents. In this functionalized material, the silyl group in the central aromatic ring disrupts the herringbone structure of pentacene and enhances the face to face motif that leads to enhancement of pi electron overlap or coupling and potentially increasing device performance. TIPS-PEN can be grown in crystalline thin films from solution producing large crystals and demonstrating very good semiconducting behaviour [63, 83].

The hole mobility in TIPS-PEN correlates with crystal direction and properties such as thickness, size and availability of cracks [17, 84]. Moreover, the film morphology, molecular ordering and its structure are key factors which determine the mobility and device performance. These parameters are affected by the choice of solvent or solvents composition ratios (in the case of binary solvents), concentration and the deposition method. Chen *et al.* [85] suggest a direct correlation between how good solvent is and the quality of the dried film after solvent evaporation.

Up to now, small molecules provide the highest field effect mobilites [40, 63] but the device to device variation arising from morphological anisotropies sometime make it difficult for large area printing [86]. On the other hand, polymers give good device uniformity [87] and their solution rheology make them prime candidates for large area

printing. But the limited mobility of polymers makes the devices fabrication unsuitable for commercial use. Blending small molecules TIPS-PEN with polymers providing good rheology and device uniformity from the solution phase, constitutes fascinating and viable approach toward enhancing device performance [39]. TIPS-PEN reveals different morphologies on a single substrate by tiny changes of solvent composition making thin films made from this material suitable for studying the effect of crystal quality and molecular ordering on device performance.

In this chapter we discuss strategies for controlling the morphology and crystalline microstructure of soluble (TIPS-PEN) as the organic semiconductor of interest in fabrication of organic field effect transistor OFETs. The motivation to study TIPS-PEN is not to chase performance figures only but to investigate how the solution deposited film topography can be controlled by varying the solvent composition and the insulating polymer binder concentration. The first part of this chapter discusses the impact of evaporation-induced flow on drop cast dried films by controlling solvent exchange composition, involving changes to the minor solvent decane concentration relative to that of the anisole bulk solvent. The resulting film morphology is significantly improved from a grainy and featureless thin film for pure anisole solvent to long ordered molecules terraces through this control of the minor solvent ratio. We also focus on the resulting film roughness and grain density statistics from captured AFM images. Finally, we discuss the performance of transistors in term of maximum, minimum and average mobility for 9 fabricated devices. The blend of insulating polymer and small molecule TIPS-PEN is discussed in the second part of the chapter. It was found that addition of polystyrene has a significant effect on improving both macroscopic crystal properties and film surface morphology. It was observed improvements in the surface coverage, unity of orientation, long range molecular orders and average field-effect mobility. We compare large scale optical microscopy images and nano-scale AFM images on both SiO_2 and poly (4-vinyl phenol) PVP surfaces. The influence of insulating polymer composition in blend on crystal size, film morphology, molecular ordering, and device performance is discussed in detail. Finally, we summarise the conclusions and suggest future works. This study was performed in collaboration with Professor Stephen Yeates and He Lan from the School of Chemistry, University of Manchester, UK.

3.2 Solvent blend casting

In the process of solvent casting of blends three possible stages are expected: 1) vitrification, 2) phase separation, 3) crystallization and nucleation.

3.2.1 Vitrification

Vitrification is the transformation of a substance into a glassy state. In inorganic materials, it is induced usually on rapid cooling through a glass transition temperature T_g that is characteristic of a material. Below T_g amorphous materials are glassy whereas above T_g they are molten. The exact value of T_g depends on the thermal history and rate of cooling – and on the timescale of the measurement of its physical properties. Vitrification occurs when bonding between material particles such as atoms or molecules becomes higher than a certain threshold value [88] : it is a process that changes the solution or liquid into a glass-like solid when its temperature is under glass transition temperature [89]. Many polymer systems lack a well-defined crystalline state and easily form glasses, even upon very slow cooling.

3.2.2 Phase separation

Phase separation is a complex process that can occur when solvent evaporates from a solution of two or more components or solutes. The segregation of phases in a binary polymer system depends on several factors such as molecular parameters (miscibility, solvent, and concentration), thermodynamic conditions (temperature, pressure) and the film formation method (such as spin coating, doctor blading, or drop casting). For such systems, during solvent evaporation the blend will separate from one mixed phase to two individual phases, depending on the free energy of the system [90]. The Gibbs free energy of mixing $\Delta G_m = G_{mixed} - G_{segr}$, the difference between the Gibbs free energy of the mixed and segregated states, at temperature T is

$$\Delta G_m = \Delta H_m - T\Delta S_m \tag{3.1}$$

where ΔH_m , ΔS_m are the corresponding enthalpy and entropy of mixing respectively. At high temperature the entropy become the controlling factor on the blend

and a single mixed phase is favoured. However as the temperature is decreased, the enthalpic interaction dominates resulting in two segregated phase [91].

Phase separation will always occurs when $\Delta G_m > 0$. However, phase separation can not occur for $\Delta G_m < 0$ [92]. Figure 3.1 shows the free energy of mixing ΔG_m as a function of composition, the line connecting these two minima (at which $\partial G/\partial c = 0$) determines the binodal curve for various temperature. The binodal curve represents the condition for binary distinct phases may coexist or it's the thermo -dynamical limit between mixed phase system and separate phases. Furthermore, the two inflection points where $\partial^2 G/\partial c^2 = 0$ specify the spinodal curve for different temperatures. The spinodal curve is the frontier of absolute instability of solution to decomposition into two phases. Inside the spinodal curve any small changes in composition leads to phase separation via spinodal decomposition which is a fast mechanism to segregate solution from one thermodynamic phase into two coexisting phases. Furthermore, the maximum point for both curves in temperature coincides and is known as critical point.

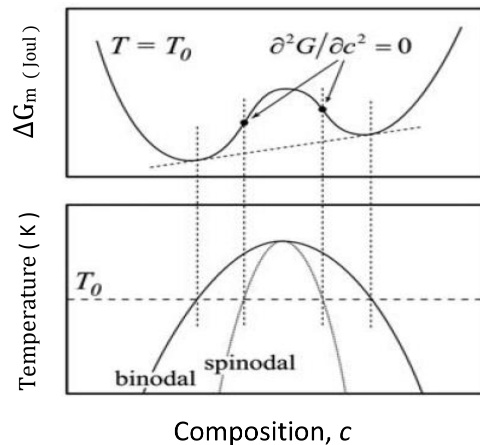


Figure 3.1: Free energy as a function of composition change and spinodal, binodal curves at various temperatures.

For a blend system consisting of a small molecule and a polymer, such as TIPS-PEN/and poly(α-methyl styrene)(PαMS), as used by Ohe *et al.* [93], TIPS-PEN is regarded as a first component and PαMS as a second one. The calculation of ΔG_m values of the TIPS-PEN/PαMS system was performed for different PαMS molecular weights. For low molecular weight of PαMS ΔG_m showed a negative value consistent

with a homogenous film. However, with high polymer molecular weight the changes of Gibbs free energy of the mixed phase showed a positive value which would be expected to lead to a phase separated structure.

3.2.3 Crystal nucleation

The process of nucleation and crystal growth happens within binodal and spinodal curves which are in a metastable region. Nucleation is very sensitive to the system impurities and therefore it is important to distinguish between homogeneous and heterogeneous nucleation. In homogeneous nucleation the nuclei develops in supersaturated solution in the absence of any foreign surface. In contrast, heterogeneous nucleation occurs when foreign particles exist in the solution so the nuclei are formed around the alien or odd particles such as dust or impurities. The self-seeding nucleation is the third type, which is produced by self-induction of small crystals of the same materials.

The general stages of growth from homogeneous nucleation are illustrated in Figure 3.2 aggregation follows nucleation and leads finally to lumps or agglomerate growth.

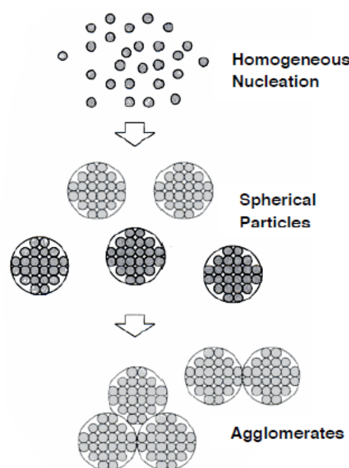


Figure 3.2: Homogeneous nucleation mechanism [94]

As regards to self-seeding nucleation, the crystallization starts from seed crystals which are very tiny clusters or sub-microscopic crystals. The small crystals combine to form larger crystals in size.

Seed crystal can nucleate new crystals leading to larger size of crystals then they grew to compose a final growth and total crystallization, as illustrated schematically in Figure 3.3.

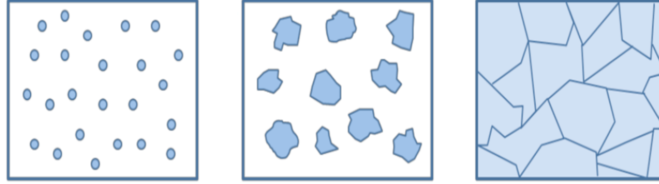


Figure 3.3: Crystallization starts from seed crystal followed by crystal nucleation and formation of large crystal.

3.3 Solubility parameter and TIPS-pentacene solubility

The Hildebrand solubility parameter δ is defined as the root mean square value of the cohesive energy density of solvent:

$$\delta = (CED)^{1/2} \tag{3.2}$$

It is a numerical value [expressed in $(MPa)^{1/2}$] which characterises the relative solvency of a solvent [95]. Cohesive energy relates to the heat of vaporization divided by molar volume cm^3/mol

$$CED = \frac{\Delta H - RT}{V_m} \tag{3.3}$$

where $\Delta H,\ R,\ T$ are the heat of vaporization, gas constant and temperature respectively.

Therefore, CED is a numerical value representing the heat of vaporization in units of calories per cubic centimetre of solvent. By substituting the last equation in 3.3 we get.

$$\delta = \left(\frac{\Delta H - RT}{V_m}\right)^{1/2}$$

or $$\delta = \left(\frac{\Delta E_i^V}{V_i}\right)^{1/2} \qquad i\text{=1, solvent; } i\text{=2, solute}$$

where E_i^V is the energy of vaporization for a solvent or solute

The numerical value of cohesive energy correlates with the van der Waals force which holds molecules together. For a material to dissolve in a solvent, the same interaction needs to be overcome as molecules separate from each other and surrounded by solvent. In other words, this correlation between Van der Waals force and vaporization translate to a correlation between vaporization and solubility behaviour.

As regards to material like TIPS-PEN which has a good solubility in the majority of organic solvents we can explain the situation as below:

Generally, the dissolving process becomes easier when the Gibbs free energy of mixing is as negative as possible. The Gibbs free energy relates with enthalpy and entropy of mixing according to the equation 3.1 [85]. Furthermore, the enthalpy of mixing relates to the solubility parameters, fractional volume φ and volume of mixture V according to [96].

$$\Delta H_m = (\delta_1 - \delta_2)^2 \varphi_1 \varphi_2 \mathrm{V} \tag{3.4}$$

where δ_1, δ_2, φ_1, φ_2 are solubility parameters and volume fractions for solvent and solute respectively.

As seen from equation 3.4 the values of the solubility parameter must be as close as possible in order for $(\delta_1 - \delta_2)^2$ to be close to zero which in turn makes the Gibbs free energy of mixing as negative as possible to give good solubility. The estimated solubility parameter for TIPS-PEN is 18- 19 $(\mathrm{MPa})^{1/2}$ [97]. The value of the solubility parameter is an important criterion for the choice of solvent: a good solvent is one where its solubility parameter highly matches with that of the solute in order to get a suitable solution processible organic semiconductor. Hence, the solubility parameter and boiling point are regarded as important characteristics in optimizing solution processing conditions.

3.4 Experimental details

In this section we try to review the main experimental techniques used in this chapter for the fabrication, characterisation, and measurements of TIPS-PEN thin films and devices.

1. A silicon wafer was firstly cleaved under ambient condition and cut into roughly equal size of typical dimension 6 mm x 6 mm. The cleaved wafer was then cleaned by ultrasonic bath for 5 minutes with a sequence of methanol, acetone and isopropanol followed 30 minutes ozone treatment in order to remove organic molecules from the surfaces.

2. TIPS-PEN powder, purchased from Aldrich was used to form the semiconductor solution of 2 wt% of TIPS-PEN with various composition of anisole and decane ratio R_{1-x} where x= 0, 0.05, 0.09, 0.1, 0.15, 0.2.

3. After selection of a single binary solvent with x=0.09 (Anisole/decane = 91/9). TIPS-PEN and polystyrene solution were blended with different ratio TIPS-PEN / Ps (M_w= 900 kDa) = R_{1-y} where y = 0, 0.05, 0.1, 0.15, 0.2. This means the TIPS-PEN blend ratio varied from 1, 0.95, 0.9, 0.85, 0.8 for 2 wt% blend.

4. The solution was drop cast in air onto a surface of silicon wafer comprising 300 nm thermally grown gate oxide layer with, tilted at a 5° angle at 30 °C .

5. To secure complete film drying, the substrate was left in ambient for at least three hours to make sure that all the solvent evaporated. Figure 3.4 shows the drop casting process in our clean room.

Figure 3.4: Drop casting Tips-PEN solution with different composition of anisole and decane on Si wafer.

6. The source and drain electrode were finally deposited through a shadow mask by thermal evaporation of gold to form the contact electrodes of thickness about 80-100nm on the top of organic semiconductor under 1-2.5×10^{-7} Pa with a

deposition current 4.2 A (Figure 3.5). The procedures 6, 7, 8 were conducted in Manchester University.

7. **Poly(vinyl-phenol) surface treatment**: To prepare the organic gate dielectric, a fresh coating solution consist of 3.4 wt% PVP and a cross linking agent 1.1 wt% of poly(melamine-co-formaldehyde) in PGMEA (Propylene glycol monomethyl ether acetate) solvent was stirred for 2hours. The solution then used to spin coating onto substrates with spin speed of 2000 rpm in vacuum room and for duration of 30 seconds. Substrates were then dried on a hot plate for 2 minutes at 120 ºC under normal atmosphere to evaporate the solution then heated at 160 ºC for 30 minutes to complete the cross linking process.

Figure 3.5: Specialized glove box for gold evaporation and deposition of contacts through shadow mask.

8. Electrical characterization (*I-V* characteristics) of organic field effect transistors was carried out at room temperature under ambient conditions using an Agilent B1500A semiconductor parameter analyser.

Figure 3.6: Image of microprobe station and semiconductor device analyser (at the School of Chemistry)

3.5 Film casting and evaporation

As we mentioned in the previous chapter, there are different techniques for film deposition from solution. Drop casting is popular because of its simple processing and low cost. In this work this method was selected for depositing TIPS-PEN thin films. The drop casting method includes three main stages starting from depositing a small volume of prepared solution onto the substrate surface using a micropipette. Solution spreading over the substrate is strongly dependent on the nature of surface. Solvent evaporation and complete film drying comes as a third and final stage. The dried films can reveal different morphology and microstructure depending on the solvent evaporation rate. The evaporation rate in turn correlates with different factors such as: temperature, vapour pressure and the amount of air current flow over the surface. The amount of mass loss per unit area at temperature T is defined as the evaporation rate [98]:

$$E = K_m \ (P_{sat} \ - \ P_w) \ \frac{M_w}{RT} \tag{3.5}$$

where K_m is a mass transfer coefficient, P_{sat} , P_w , M_w, R are the saturated vapour pressure, partial pressure of water, molar mass of the evaporating molecules and the gas constant respectively.

In this work we used a system of binary solvents or solvent exchange method consisting of anisole $CH_3OC_6H_5$ of boiling point BP=155°C, density 0.953 g/cm^3, and surface tension 29.313 dyne/cm as a major solvent and decane $C_{10}H_{22}$ with boiling point BP 174 °C, density 0.73 g/cm^3, and surface tension 23.8 dyne/cm as a minor or secondary solvent.

Figure 3.7 shows the chemical structures of anisole and decane respectively.

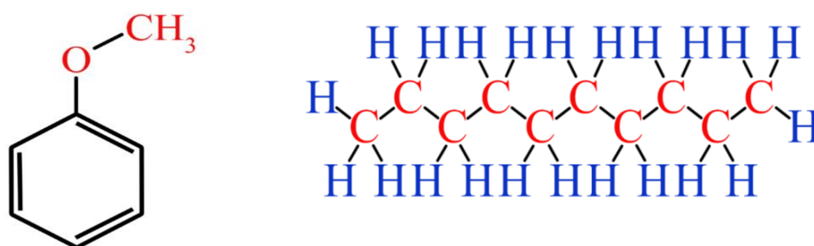


Figure 3.7: Anisole (left) and decane (right) chemical structure.

The device active layer morphologies and its crystalline microstructures are sensitive to processing nature such as solvent evaporation rate [63] and solubility of the molecules [99]. During solution processing we noticed that the drying behaviour has an essential influence on self-organization of organic molecules. Likewise, controlling of evaporation – induced flow during the solvent drying process plays a crucial role in organic small molecules crystallization and thin film morphology because the solute easily moves by solvent flow. The formation of molecular self- organizations and crystalline grains within the thin film, and device channel might be beneficial as good π – orbital overlap and better transistor performance.

We will explain later the effect of evaporation induced flow on the morphology and microcrystalline structure of dried film by controlling the solvent ratio. The continuous circulation of flow in drop casted droplet induced by Maragoni flow (driven by surface tension gradient) and opposite to the convective flow successfully produces TIPS-PEN crystals. In turn, the quality of these crystals and the way they are produced will specify the device performance to a large extent. Decane has high boiling point and low surface tension compared to the main solvent anisole which has a higher surface tension and continuously recirculation of solvent flow can be achieved. Accordingly, nucleation starts from contact line and crystal formation fill up or replenish from edge toward droplet inside. The change of solvent composition and monitoring the surface topography and film drying process leads to optimized mixed solvents which can be used to control thin film morphology and molecular ordering.

Part 1

3.6 TIPS-PEN crystalline thin film growth

In this section we will discuss the morphology of drop-cast 2 wt-% TIPS-PEN films as a function of the solvent composition employed during film deposition. Optical microscopy of magnification (20x) was used to monitor the large-scale morphology and AFM the nm scale morphology for anisole/decane ratios from 100/0 to 80/20 (vol/vol).

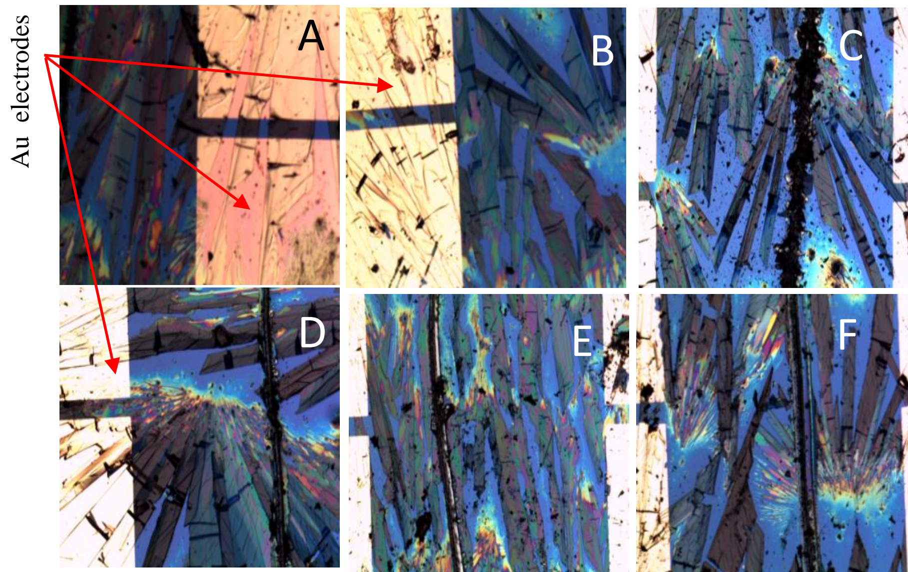


Figure 3.8: Optical microscope (OM) images (scale 800 μm x 800 μm) of TIPS-PEN droplet with various solvent compositions. A) pure anisole, B) mixed solvents containing anisole and 5% decane, C) anisole and 9% decane, D) anisole with 10% decane, E) 15% decane, and F) anisole and 20% decane. The golden areas on optical images are vacuum-deposited Au electrodes, the gap between electrodes is the active channel of length 60μm.

In Figure 3.8, we compare the micron-scale optical images with different ratios of anisole and decane as solvent mixture on SiO_2 surfaces. The optical micrographs for each solvent composition appear similar, showing asymmetric crystallites. It can be observed from these optical images that TIPS-PEN do not cover the entire surface, regardless of the ratio between anisole and decane. The crystal width ranges from 50 μm to several hundreds of microns, which leave void regions between these crystals several hundreds of microns wide. Moreover, TIPS-PEN crystals tend to appear feather

or spike-like, which means that, even within the same channel area, orthogonal crystals can be observed. Void regions causes effective channel width variation and are likely to lead to more grain boundary traps. TIPS-PEN crystals with varied orientation lead to coexisting fast charge carrier-moving path and slow charge carrier moving paths in the same channel region. This co-existence is likely to cause unwanted device-to-device variation. The micrograph images show Au source –drain electrodes as golden bars covering some area of crystalline thin film with channel length 60 µm. Detected grown crystals of TIPS-PEN shows changes in crystal shapes toward rod or elongated patterns at 15% of decane. For 20% we obtained various thin needles like crystals showing sharp facet angle close to the sample centre. In contrast, more disordered crystals are located near the sample edges.

Although the ratio between anisole and decane does not strongly affect the crystal growth pattern observed in optical micrographs, it does have a strong influence on the nano-scale surface morphology monitored with AFM. For TIPS-PEN dried film from pure anisole (single solvent), AFM images acquired from the edge Figure 3.9 and from the centre Figure 3.10 of the substrate showed no distinguishable structure such as terraces or dendrites, it revealed instead featureless or granular (grainy) structure with no evidence of clear molecular ordering.

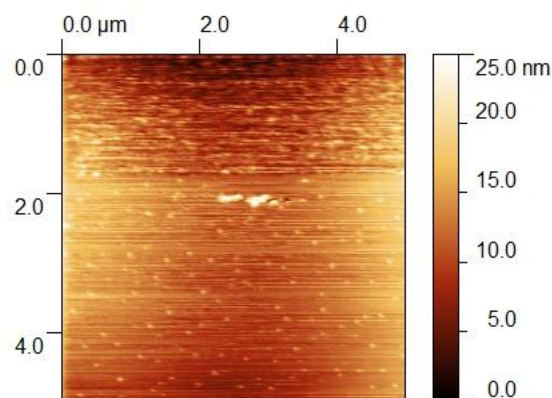


Figure 3.9: Scanned AFM image in tapping mode of a crystalline domain taken from edge of droplet.

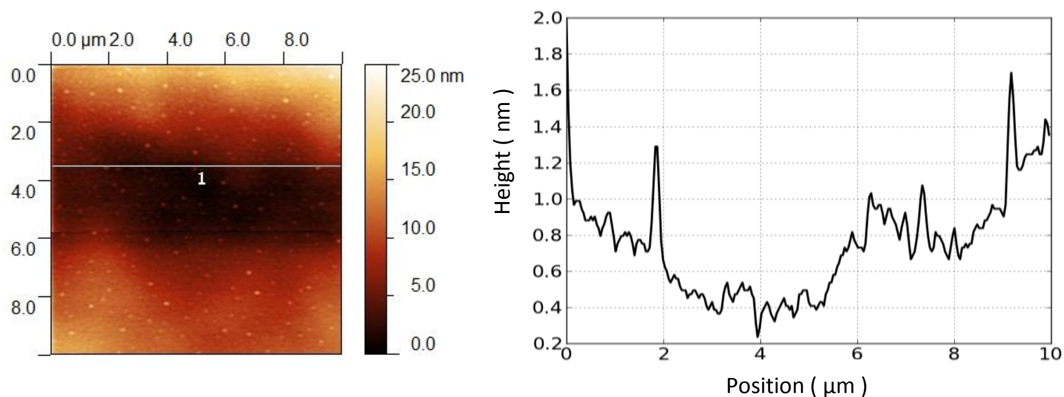


Figure 3.10: AFM image taken from centre of droplet and corresponding profile across drown line. The line profile reveals some peaks when the line crossing grains.

These grains (appearing as white dots in these images) were distributed randomly over AFM images with no tendency to accumulate in specific regions. The detected grains showed a small fluctuation in size with calculated mean diameter of order of 32 ± 2 nm. Furthermore, TIPS-PEN film printed from pure anisole had relatively high surface roughness (rms) 6.3 ± 2.2 nm.

The introduction of decane with higher boiling point and lower surface tension induces significant changes in the nano-scale morphology. Addition of 5% decane results in strong improvements in molecular ordering. Direct comparison of AFM images showed that the addition of decane in the solution results in a significant changes from granular structure to a more ordered appearance, featuring well-defined steps between terraces. Additionally, AFM captured images revealed a reduction of film surface roughness to 4.3±1.9 nm for 5 % decane binary solvents. Figure 3.11 shows the morphology for an anisole: decane ratio of 95:5 (v/v) which is dominated by stepped terraces indicative of step-flow crystalline growth. The molecular terraces show step-heights of approximately 1.5 - 1.65 nm examined by image cross section (line profile) Figure 3.11. This height corresponds to the length of c-axis (length of the lattice constant in z-direction) of TIPS-PEN molecule [100, 101], hence, this indicates that the long axis of molecules is almost perpendicular to the substrate surface. These results indicate that the solution deposited TIPS-PEN film is highly ordered with the molecules oriented close to the normal to the surface.

The commonly observed (001) projection of small molecule TIPS-PEN film demonstrate that the molecules tend to align its acene unit edge on the substrate and touch it by their bulky side (Figure 2.13)

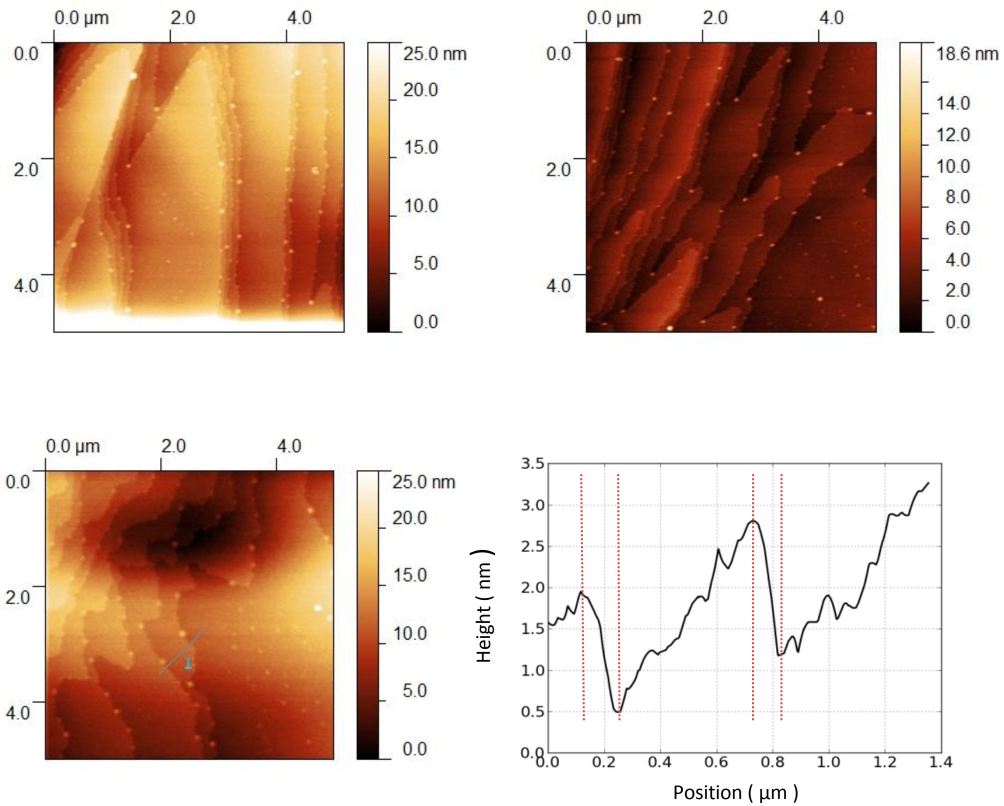


Figure 3.11: AFM images in tapping mode of TIPS-PEN drop-cast from anisol:decane 95:5 vol/vol with total vertical range 25nm. Line profile across terraces shows step height of 1.53± 0.09 and 1.61±0.11 nm respectively.

The obtained AFM images in intermittent contact mode of drop casted TIPS-PEN from 5% decane demonstrate wide directional lateral large plat like terraces or dendrite like smaller terraces. Small grains (white dots) or islands [86] were again observed, here predominantly along step edges between terraces with small number of grains formed on the top of large terraces. Narrow dendrite-like terraces appeared free from grains on their upper surface. Moreover, the steps occurred as a wavy feature rather than straight and decorated with larger grains of around 46 ± 5 nm.

The surface roughness deduced from the AFM scans confirmed the improvement in molecular ordering. The surface roughness deduced from overall image reduced to 4.3±1.9 nm. The surface roughness of flat terraces also was lower than those observed for films of deposited from pure anisole.

Similar behaviour was found for 9 and 10% decane concentration with roughly same terraces style and circular grains (islands) accumulation at the step edges (Figures 3.12a, 3.12c, 3.12d). The occurrence of grains (seen as white dots) at the step edge have been previously reported for TIPS-PEN films deposited from chloroform [102]. The appearance of the particles at the edges probably indicates that these comprise impurities expelled by the growing step. As the solvents evaporate, the grains concentration become larger with time and these particles deported or expelled by growing crystals accumulate at the step edges. Step heights deduced from cross sectional line profiles are 1.6 nm and 3.5 nm (±0.1 nm) corresponding to single and double layers molecules and well consistent with the c-axis (length of lattice constant in z-direction) spacing of 1.54 nm in the triclinic unit cell of TIPS-PEN. Smaller step heights of around 1.4nm were also observed, which may correspond to a tilted molecular orientation as shown in Figures 3.12a,b.

The step height measurements allow as to deduce molecular tilt angle ~1.4±0.6 nm corresponding to the measured step height on the assumption that the step correspond to the [001] spacing for TIPS-PEN. A step height of ~ 1.4nm corresponding to this rather crude approach to a molecular tilt angle of about 30° – 40° for 9 – 10 % decane composition. The molecular tilt angle was also noticed by other workers using AFM [14, 63]. In addition to molecular tilt angle the measured surface roughness for overall images offer the lowest value 2.7±1.0 nm and, 1.7±0.8 nm for 9 and 10% decane concentration respectively.

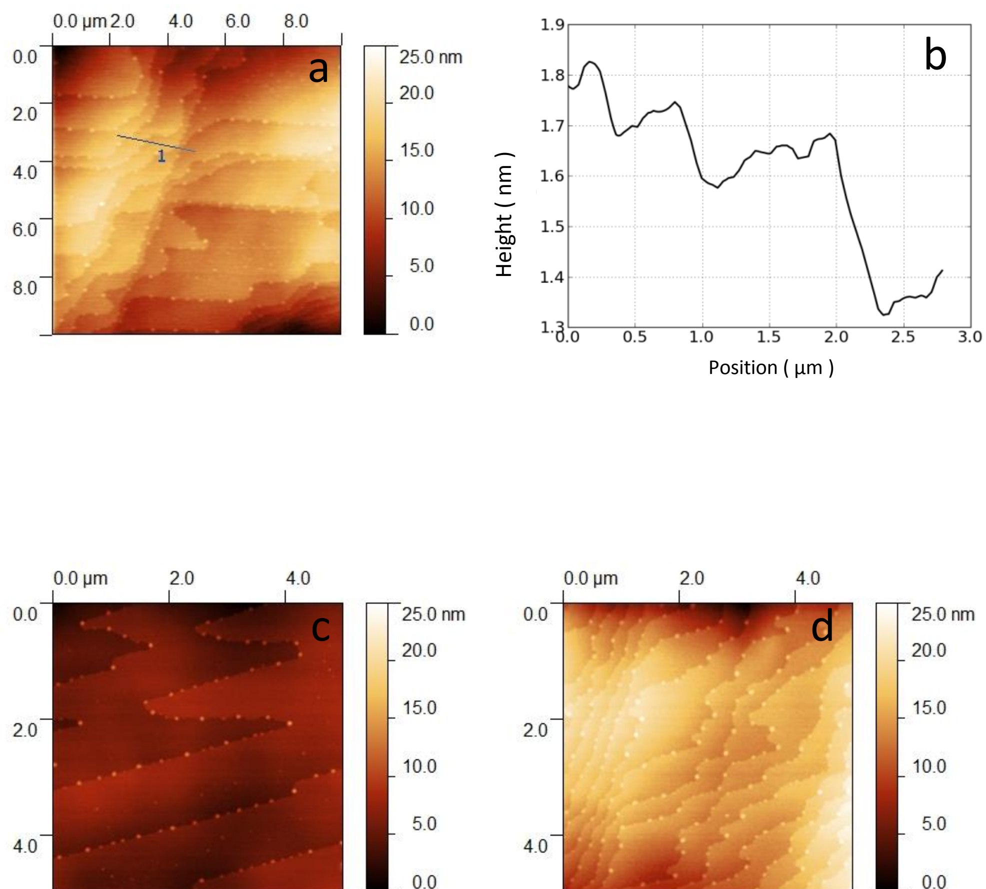


Figure 3.12: a) AFM image of 9% decane concentration. b) The profile presenting cross sectional line of (a) and shows step heights (1.41, 1.60 and 3.5nm respectively). c and, d) are AFM images for 10% decane which shows more straight steps in some cases like b.

On further increasing the decane concentration to 15 and 20%, terraces steps were not so well-defined nor straight or wavy. Instead molecular steps become unclear and AFM images revealed grainy and very poor molecular ordering especially for 20 percent decane, as in Figure 3.13. Furthermore, the overall surface roughness increased again by 4 times compared to 10%.

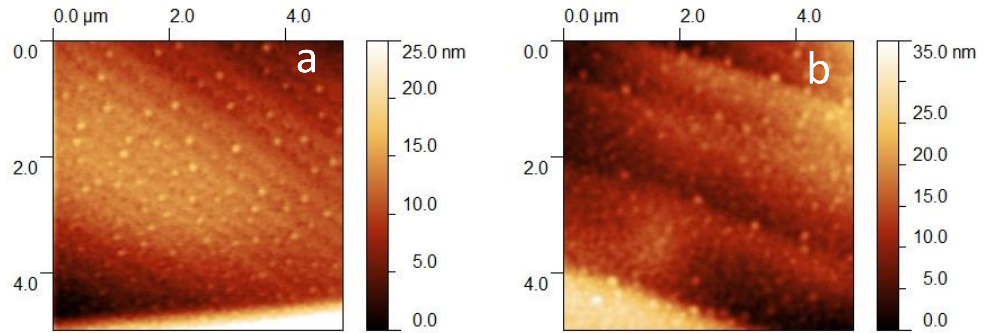


Figure 3.13: Tapping mode AFM images of, a) 15% decane, b) 20 percent of decane. We notice that the steps become unclear or undefined.

Table 3.1 lists the roughness (root mean square) values for full AFM images (5µm x 5µm) as a function of decane concentration in anisole/ decane blends. It is clear that at 10% of decane the surface roughness is at its lowest value.

Anisole:decane (v/v)	Roughness(rms)/nm
100:0	6.3 ±2.0
95 :5	4.3±1.0
91:9	2.7 ±1.0
90:10	1.7 ±0.8
85:15	6.50 ± 1.8
80:20	6.06 ± 2.0

Table 3.1: The value of roughness (rms) of captured overall AFM images according to decane concentration in blend.

Further investigations of decane impact on surface roughness were done by measuring the roughness of flat terraces between the steps. We noticed it depend sensitively on solvent concentration, being 1.04±0.35, 0.61±0.23, 0.59±0.13, 1.15±0.13, and 1.67± 0.17 nm for anisole:decane ratios of 95:5, 91:9, 90:10, 85:15 and 80:20 (v/v) respectively. In other words, the roughness of the flat terraces between the steps is lower and is sensitive to solvent ratio, showing a clear minimum at 9-10 anisole/decane (v/v) as shown in Figure 3.14 below.

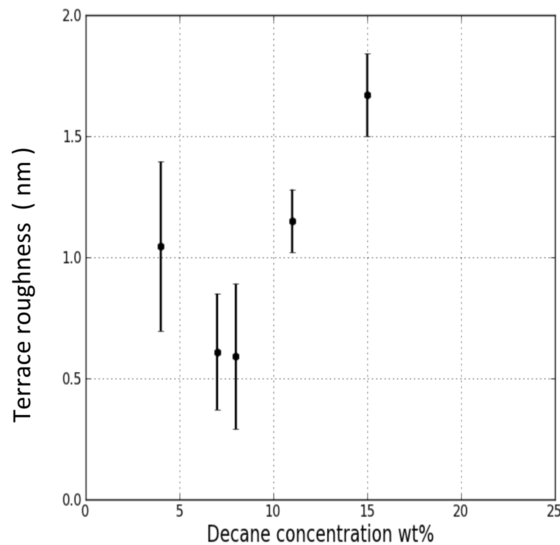


Figure 3.14: Change of roughness of a terrace with decane concentration

3.7 Evaporation dynamic and crystal growth

The nature of the evaporation process plays an important role in the resulting morphology and device performance as it governs solute material distribution in the drop cast film. The drying starts from the periphery and proceeds towards the centre of the drop which related to the outward convection flow and pinned contact line. If the contact line is pinned during the drying process, a fixed drop area will lead to a capillary flaw of liquid from the centre towards the contact line occur in order to substitute for the loss by evaporation. This type of flow limits the device performance because undesirably uneven distribution of materials across the deposit[103].

On the other hand, depinning of the contact line is depends on choice of solvents and its boiling point which identified as a key factor that determined the shape of deposit [104]. For instance, the use of high boiling solvents with low evaporation rate increases the homogeneity of deposition. The solvent evaporation rate is also likely to relate to the time scale for depinning of the contact line [104].

All drop casting process in this study were performed on substrate tilted 5° from the horizon where the lower drop line diffuse downward and upper contact line remain pinned[103, 105, 106]. During the drying process the drying speed or evaporation rate close to the upper contact line is faster than near lower drop line so the solution migrates toward the upper part of the substrate (because of hydrodynamic flow of solvent) to compensate for loss due to evaporation. The crystal seeds start to nucleate from this upward contact line and TIPS-PEN molecules diffuse rapidly toward this interface carried in the above hydrodynamic flow of solvent leading to crystal growth down the tilted surface as shown in Figure 3.15. As the solvent evaporate close to the edge of the substrate and the contact line recedes, homogeneous and continuous stacking of TIPS-PEN molecules occurs resulting from silyl group stacking on the substrate[106] and crystal seeds start to nucleate and crystallites in the direction of stacking axis down to slide [107].

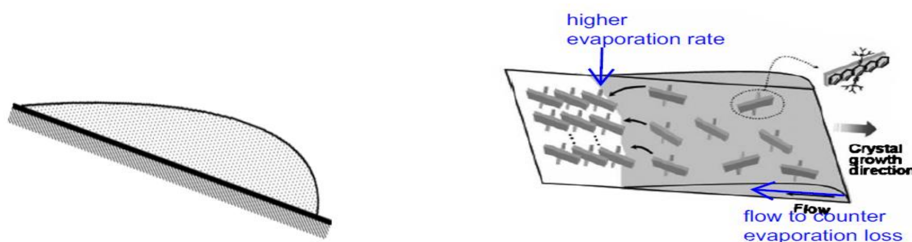


Figure 3.15: A droplet of TIPS-PEN solution on tilted substrate and the possible growth mechanism [106].

One approach to increase the homogeneity of particle distribution and morphology is to use a mixed solvent system. In this system the suspended materials that accumulate at the contact line are counterbalanced or enhanced by Maragoni flow which is induced by surface tension gradient due to solvent composition variation [108]. In other words, the solute that is transported to the contact line by convective flow is counterbalanced by the rate of Maragoni flow, which depends on the solvent composition. This Maragoni flow is induced by surface tension gradient between the periphery and the centre of the

droplet causing current flow from regions of low surface tension in the direction of increasing surface tension. High boiling point solvents generally have lower surface tension than those with lower boiling points. For a composite system which contains a mixture of solvents, if the minor component has the higher boiling point and lower surface tension, then the Maragoni flow is induced in the direction counter to that of convective flow as illustrated in Figure 3.16 below. However, if the minor solvent has a lower boiling point and higher surface tension, then the Maragoni flow can enhance convective flow.

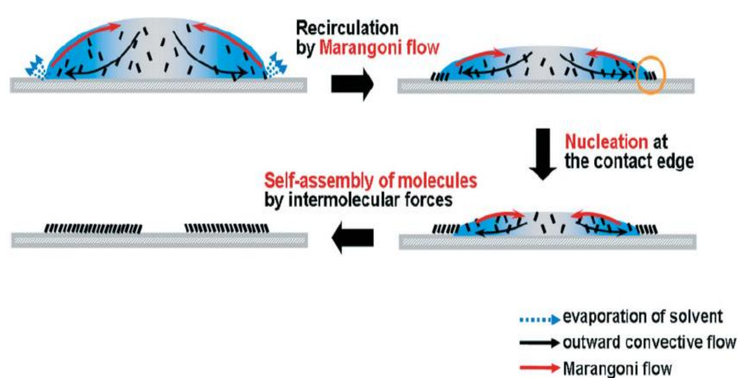


Figure 3.16: Schematic presentation of film drying by using binary solvents system the dark blue shows solvent with high boiling point[[103]].

Based on the above discussion we proposed the following explanation for crystal growth and molecular ordering in drop casted TIPS-PEN dried film. As we mentioned before, the evaporation behaviour during film drying play a key factor in controlling morphology and solute material distribution. As the molecular ordering of TIPS-PEN is highly depending on the nature of droplet [109], we tested the influence of solvent composition on microcrystalline structure and film morphology by changing the minor solvent ratio in the blend. In the case of single solvent anisole, the outward convection flow occurs from the droplet centre towards the contact line to compensate evaporation loss at the droplet edge, and this flow pushes solute material to the droplet periphery. This effect causes unwanted uneven distribution of solute across the deposit which appeared as grainy, featureless captured AFM images with no molecular terracing. Adding lower surface tension solvent decane to the main solvent anisole introduces several effects to the drying of the droplet. These include the outward convection flow and inward Maragoni flow due to surface tension gradient between minor and major

solvents making evaporation-induced flow possible. Maragoni flow starts from edge of the droplet toward its centre, inducing a smooth circulation of solvent as shown in Figure 3.16. Thus the solution gradually become more concentrated at the droplet edge and molecules self-assemble onto the surface in an ordered 'step-flow' fashion. According to the above idea, the evaporation induced flow can be controlled by varying the solvent composition. Our data is consistent with the outward convection flow being dominant for pure anisole, with the Maragoni flow rate increasing for 5% decane. The two flows are optimally balanced at 9-10% decane and the Maragoni flow is dominant at higher decane concentrations, causing more turbulent flow. While this is a reasonable explanation, consistent with our data, we cannot prove experimentally that this is indeed the true mechanism.

Furthermore, UV-vis analysis of anisole/decane mixture, showed a blue shift (Figure 3.17) by increasing decane composition that support H-aggregate formation (H-aggregate exhibit a blue shifted absorption band which support face-face motif of molecular ordering) [110].

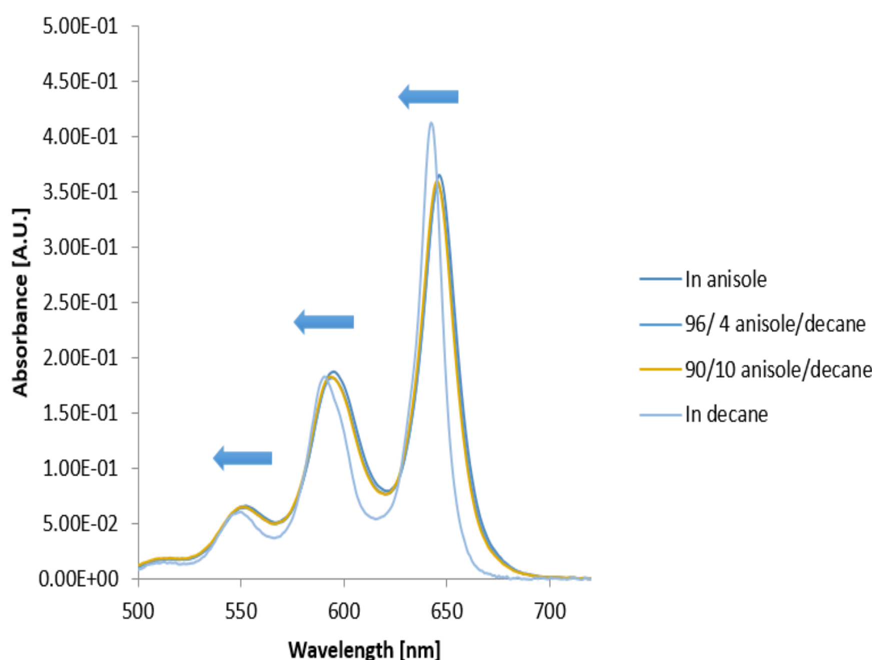


Figure 3.17: UV/Vis absorption spectra of TIPS-PEN dissolved in different anisole/decane solvent mixtures at a constant 1 x 10^{-5} M. Arrows illustrate the blue shift with increasing decane content [This experiment was performed by our colleague collaborator in Manchester University].

3.8 Performance of pure TIPS-PEN transistor

The measured average field effect mobilities obtained for the various anisole: decane compositions of the drop-casted TIPS-PEN are listed in Table 3.2 below. The average mobility for each composition is obtained over 9 devices. Table 3.2 also shows the summary of the maximum and the minimum mobility for each case.

Anisol:decane ratio (v/v)	Maximum mobility $cm^2 V^{-1} s^{-1}$	Minimum mobility $cm^2 V^{-1} s^{-1}$	Average mobility $cm^2 V^{-1} s^{-1}$
100:0	0.036	0.00025	0.0138
95:5	0.028	0.00094	0.011
91:9	0.058	0.00226	0.013
90:10	0.026	0.0017	0.0134
85:15	0.034	0.00035	0.0141
80:20	0.021	0.00004	0.0044

Table 3.2: Summarized maximum, minimum, and average mobility results obtained on transistors as a function of anisol:decane ratio.

For each reported condition, we obtained average value of nine different devices gathered with the minimum and maximum recorded mobility for each case. Whilst the average performance of the devices remains roughly around 0.013 $cm^2V^{-1}s^{-1}$ overall anisole:decane compositions we observe an improvement in device to device uniformity up to 10 vol-% decane, but beyond this limit we see a rapid fall off in device to device uniformity with increasing decane ratio. The minimum mobility range is between $2.2x10^{-3}$ $cm^2 V^{-1} s^{-1}$ for 9% decane to 3.5x 10^{-5} $cm^2 V^{-1} s^{-1}$ at 20% decane in the bulk. However, the maximum recorded mobility is between 0.058 and 0.021 $cm^2 V^{-1} s^{-1}$ for the same decane proportion.

3.9 Step edge grain statistics

We investigated the size and distribution of the accumulated grains (small balls which appear white in images such as Figure 3.12) at the step edges using Gwyddion software (Gwyddion is a modular program for SPM-scanning probe microscopy data visualization and analysis. It can be used for all data processing operations such as: analysis of height field obtained by AFM, STM, profile extraction, levelling and data correction, standard statistical characterization, filtering and grain marking function,…etc). Interestingly, the distance between grains along step edges appear to be similar, though not exactly equal. However, the observed number of grains was a function of step density and increased with number of steps. This result means random distribution of expelled white dots along step edge during crystal growth or formation. Figure 3.18 below shows masked grains statistics for 10 percent decane composition.

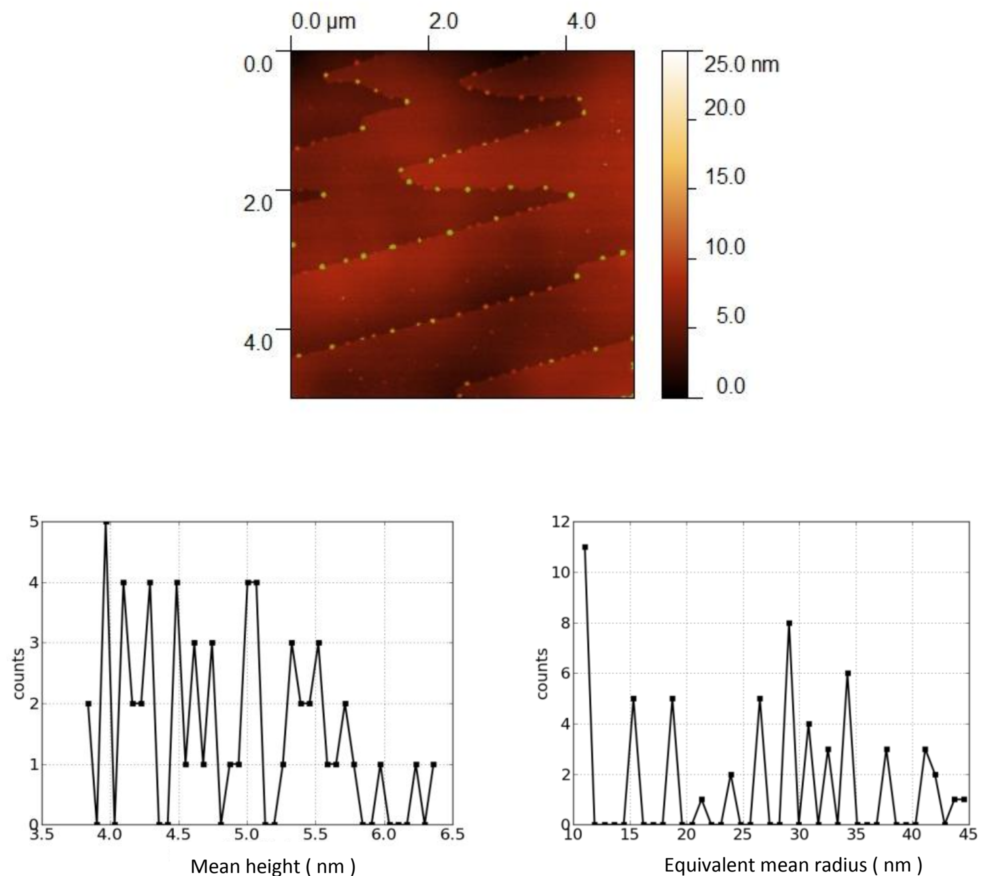


Figure 3.18: Grains (small balls) statistic according to their mean height and equivalent mean disc radius

Part 2

3.10 Influence of low concentration of polystyrene on crystal growth, surface roughness and OFET device performance of TIPS-PEN.

A second approach to controlling the morphology of the drop cast film, blend an organic small molecule semi-conductor with an atactic polymer binder. Many studies of solution blending of organic semiconductors with organic insulating polymers such as polystyrene have been recorded [111, 112]. This strategy has been used in an endeavour to enhance the organic device performance [40, 93]. In such devices, - fine tuning of an insulating polymer in the blend leads to regulation of phase separation, which in turn leads to a fine adjustments of hole movements in the transistor channel. On the other hand, the adding of insulating polymer to the semiconductor limits charge transport [113]. Therefore, the logical and straight forward method to tackle this problem is current pathway guarantee. However, to get such high level of current pathway, phase segregation and small molecule crystallization need to be closely controlled. Here we examine these two competing effects to optimise the blend concentration of amorphous atactic polystyrene (aPS) of molecular weight 900 kDa in TIPS-PEN drop-cast films.

The process of phase separation is complex and affected by factors such as the molecular weight of the polymer, solvent evaporation rate, degree of crystallization of blend components and the surface properties of the substrate [114].

Morphology, film roughness, and resulting mobility were examined as a function of aPS ratio in the blend with TIPS-PEN, on both hydrophilic and hydrophobic surfaces for the anisole: decane composition of 91:9 which gave the best TIPS-PEN film morphology, and long range molecular ordering. This solvent ratio gave well defined terraces, low film roughness and the most consistent mobility values. Therefore, in this part all blended TIPS-PEN/aPS films are studied at fixed anisole:decane ratio 91:9.

Figure 3.19 compares the optical micrograph images of drop casted TIPS-PEN and polystyrene blends crystal growth on SiO_2. The weight fraction of TIPS-PEN from A to E are 100, 95, 90, 85, and 80 percentage values in drop casted 2 wt % blend.

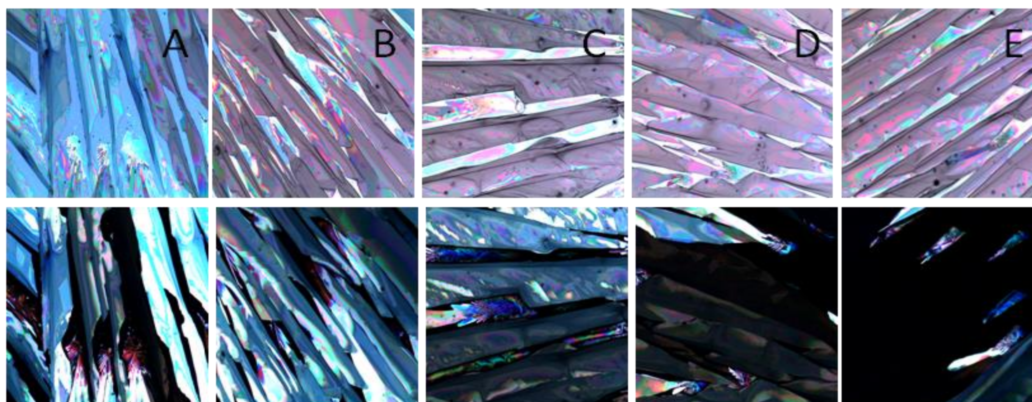


Figure 3.19: Polarized Optical micrographs of 800 μm x 800 μm (0º top upper and polarization rotated through 90º dawn lower) for pure TIPS-PEN film and four TIPS-PEN/aPS blends ratio at 30 ºC. A) 100:0, B) 95:5, C) 90:10, D)85:15, E) 80:20, on SiO_2 substrate. Solvent used is anisole:decane =91:9 (v/v).

It is clear that as the polystyrene content increases we observe that the plate-like crystals become more aligned and also the surface coverage improves with almost the entire surface covered at a 85:15 TIPS-PEN to polystyrene blend ratio. However, pure TIPS-PEN demonstrates the least crystal alignment and coverage under the same solution concentration condition. Furthermore, since TIPS-PEN absorbs polarized light most strongly when the light is aligned with the conjugated pentacene stack, the difference between brightness under polarized optical microscope indicates different degrees of long-range order of TIPS-PEN stacking. The brightness change becomes sharper and the regions of uniform colour become larger as the amount of polystyrene increases, indicating that the addition of aPS not only improves surface coverage but also promotes long-range order as well.

Atomic force microscopy is used to map the surface morphology of blend film which forms the conducting channel in OFET. On SiO_2 substrates, AFM images reveal step heights of 1.6 nm, which corresponds to the pentacene molecule length. This result demonstrates that the pentacene conjugated axis is close to perpendicular to the SiO_2 substrate surface. Similar stepped surfaces with flat terraces are observed across samples with different aPS compositions, but two differences are apparent: the step edges are much straighter than those for pristine TIPS-PEN and larger grains, of the order of 125 nm or more across, are observed on the terraces between steps.

Figure 3.20 and 3.21 show AFM images of TIPS-PEN blend with 5% Polystyrene film. It is clear that not only the step edge become straighter but also the terraces widen noticeably compared to those in pristine TIPS-PEN.

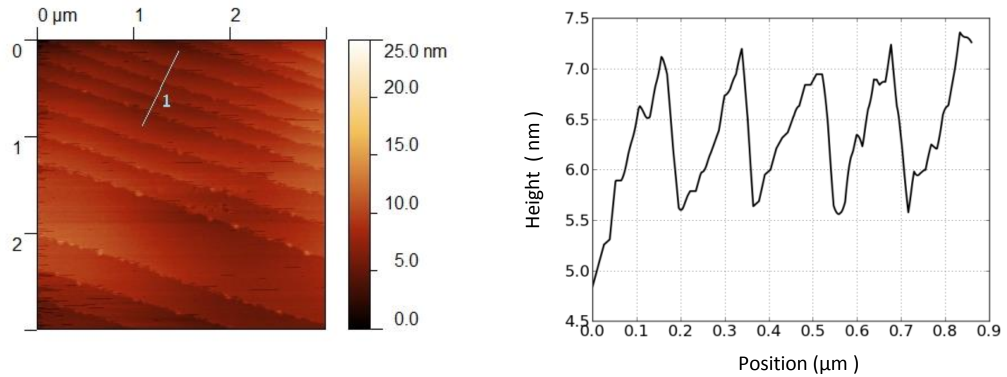


Figure 3.20: Tapping mode AFM image of 5% PS blends that show step height (1.62± 0.15) which consistent with previously measured step height for pure TIPS-PEN.

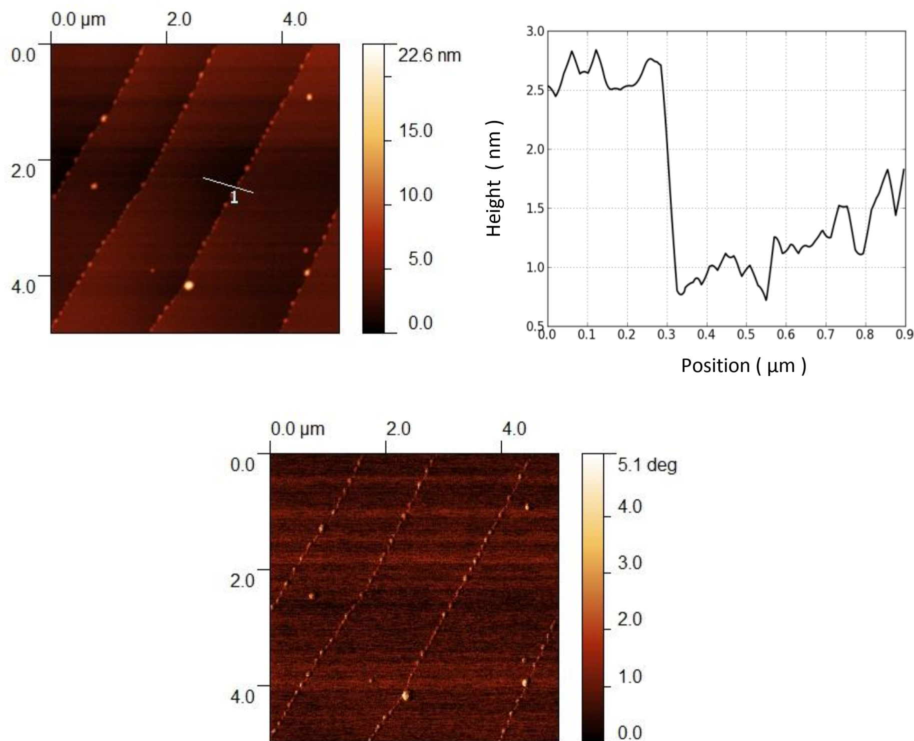
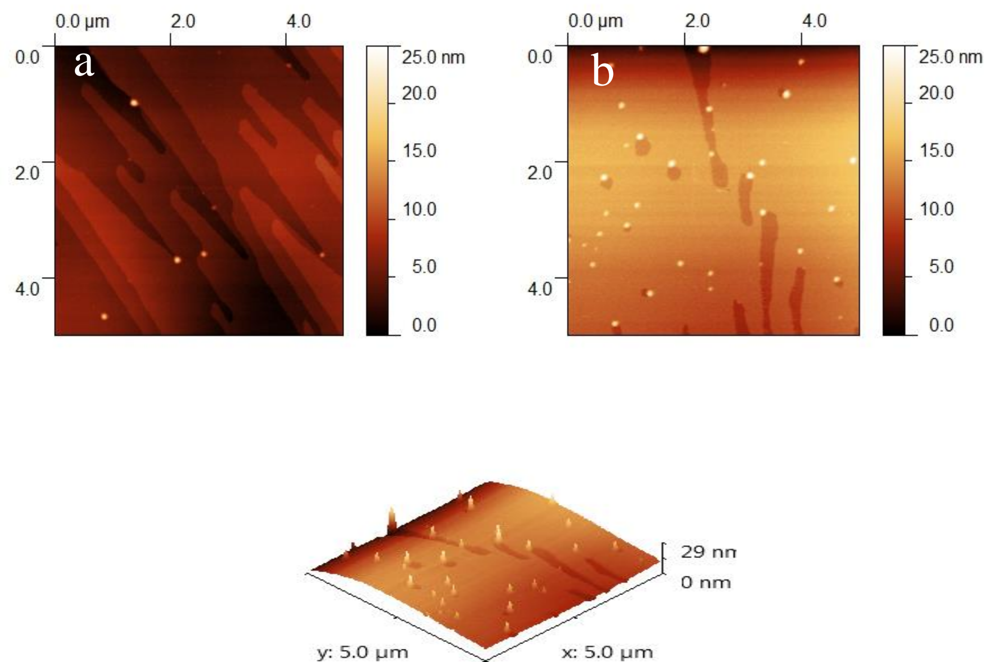


Figure 3.21: AFM height and phase images of 5% polystyrene blend with cross sectional line profile. The measured step height is (1.96±0.11) nm. The phase image shows the appearance of larger grain size suggesting polystyrene visage during phase segregation.

Moreover, the blend films revealed two types of nano- size surface morphology. The first one appeared with normal step heights 1.55-1.7 nm and with small size grains (30-50nm) across the step edges (Figure 3.20). While, the second one exhibited larger steps height of order of 1.8-2.0 nm and bigger grain size of about 125 nm or larger across and above the terraces Figure 3.21. Also the detected images revealed overall roughness of order of 2-2.5 nm.

On further increasing of the polystyrene ratio to 10% dendrite-like terraces appeared in some AFM images decorated with small numbers of large grains across step edges. On the other hand, other images revealed wide terraces with some cracks or opening on the top Figure 3.22. Surprisingly small shallow trenches, 1 molecule deep, lie next to the grains on flatter terraces (Figure 3.22b). No noticeable difference in electrical performance was detected for 5 and 10% polystyrene content in TIPS-PEN blends. The average recorded mobility for 5 and 10 percent polystyrene blends were 0.0027± 0.0016 and 0.0032 ± 0.0021 $cm^2 V^{-1} s^{-1}$ respectively. The overall film roughness was 3.4±1.1 nm for 10% composition.



+

Figure 3.22: 10% polystyrene blends AFM images with dendrite style (a) and wide terrace (b). The bottom picture is the three dimensional image of (b).

When the weight fraction of polystyrene was boosted to 15 percent the devices average mobility increased one order of magnitude to reach the value 0.034±0.0013 cm^2 V^{-1} s^{-1} and the overall film roughness (area averaged) went up to 5.7 ± 1.3 nm. Furthermore, the optical and polarized micrograph images revealed large, directional plate like crystals, and confirmed long range TIPS-PEN molecular stacking.

Active layer	Mean mobility cm^2 V^{-1} s^{-1}	Deviation
Neat TIPS-PEN	0.013	
5% poly. blend	0.0027	0.0016
10% poly. blend	0.0032	0.0021
15% poly. blend	0.034	0.0013
20%poly.blend	0.016	0.0058

Table 3.3: Electrical properties of drop casted TIPS-PEN and aPS blended OFET. The standard deviation was calculated for 9 devices.

Regarding the nano-size surface morphology, two categories of AFM images are seen in Figure 3.23. The crystal images from substrate edges revealed straight and narrow terraces with normal TIPS-PEN step height and steps of smaller heights of order of 1.3 ±0.2nm. Double layer step height of order of 2.8±0.2nm again comes to light.

However, the AFM images of crystals close to the centre of substrate demonstrate continually large lateral grown terraces with molecular steps.

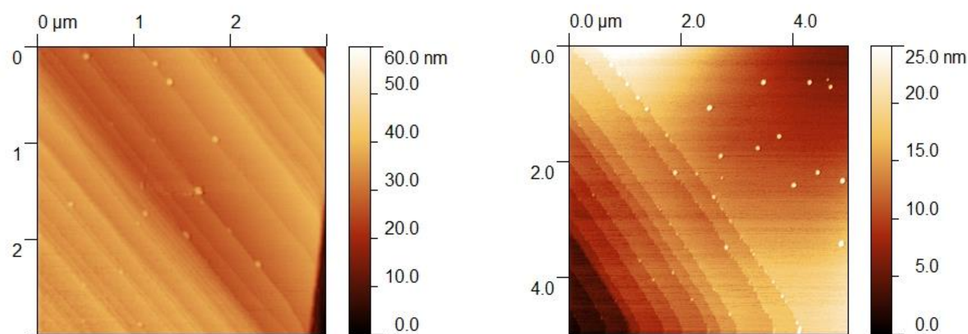


Figure 3-23: Atomic force microscopy images of drop cast film of TIPS-PEN:15% aPS 2%wt blends. The left image is from crystals at the substrate edge. The right image taken from crystal close to the centre of substrate.

Adding extra polystyrene to the blend to reach 20% (Figure 3.24) the overall film roughness reduce to 3.8±1.5 nm and the mobility to 0.016±0.006 $cm^2\,V^{-1}\,s^{-1}$.

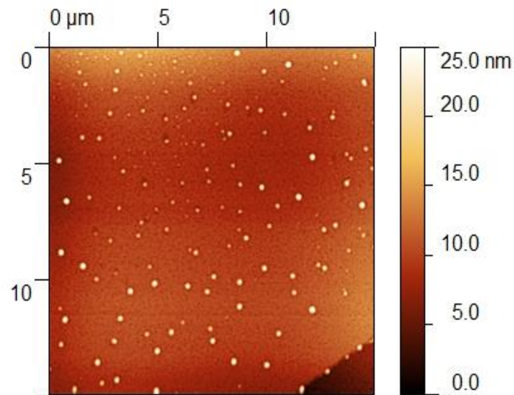


Figure 3.24: 20% polystyrene blend. The terraces again contain lots of holes or openings sharing only with one white ball (polystyrene).

The roughness of flat area between terraces for different aPS ratio on SiO_2 surface showed the values 0.67±0.34, 1.12±0.44, 0.80±0.16, 1.25±0.38 for 5, 10, 15, and 20% for aPS respectively. Figure 3.25 shows the change of roughness with aPS contents in the blends.

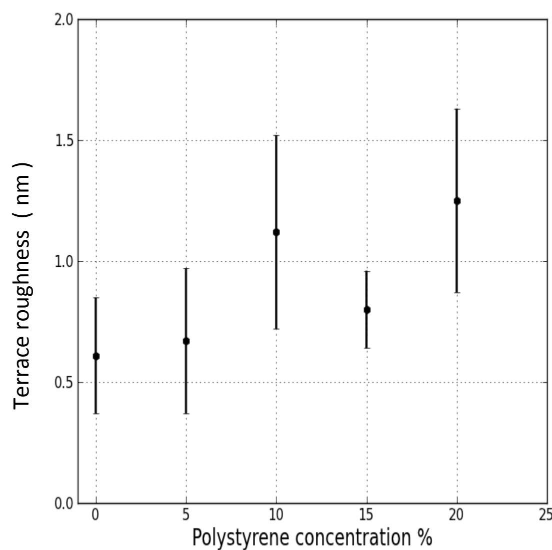


Figure 3.25: Flat area roughness variations with aPS composition in the blend on SiO_2.

Table 3.3 shows the mobility values for pure TIPS-PEN film and its blended films according to the weight fraction of polystyrene in the solution. From these results, we notice that the average mobility is decreased when TIPS-PEN was blended with insulator binder. This effect is might be due to the intrusion of insulating polystyrene into TIPS-PEN rich regions [115]. Also the strong interaction between small molecules and insulating binder probably prevents phase segregation towards active interfaces [111]. However, the improved film morphology, crystal quality, for 15% aPS reveal the best uniformity for polystyrene blended devices. Furthermore, the mobility is increased roughly about three times compared to the neat TIPS-PEN on SiO_2 to reach the value 0.0334 $cm^2 V^{-1} s^{-1}$ and the film uniformity is enhanced. These indications possibly due to the favoured phase separation between polystyrene and TIPS-PEN components for 15% of polystyrene.

Lee e*t al.* (2009) and Lee *et al.*(2014) suggested that when a soluble acene/ insulating polymer is deposited onto a hydrophilic substrate (like SiO_2) the organic small molecule semiconductor with low surface energy tends to preferentially segregate towards the air film interface and insulator polymer toward substrate film interface [90, 116]. This feature of phase segregation (organic semiconductor top/insulator polymer bottom) is also useful for fabrication of top contact and bottom gate field effect transistor [90].

The drop casting of small molecule TIPS-PEN/polystyrene on hydrophobic PVP treated SiO_2 substrate showed improved morphology and high mobility. The morphological improvements monitored by optical microscopy images and scanning probe microscopes by AFM in tapping mode are consistent with better device performance. The main problem during our analysis is to understand in full the structural basis behind these improvements.

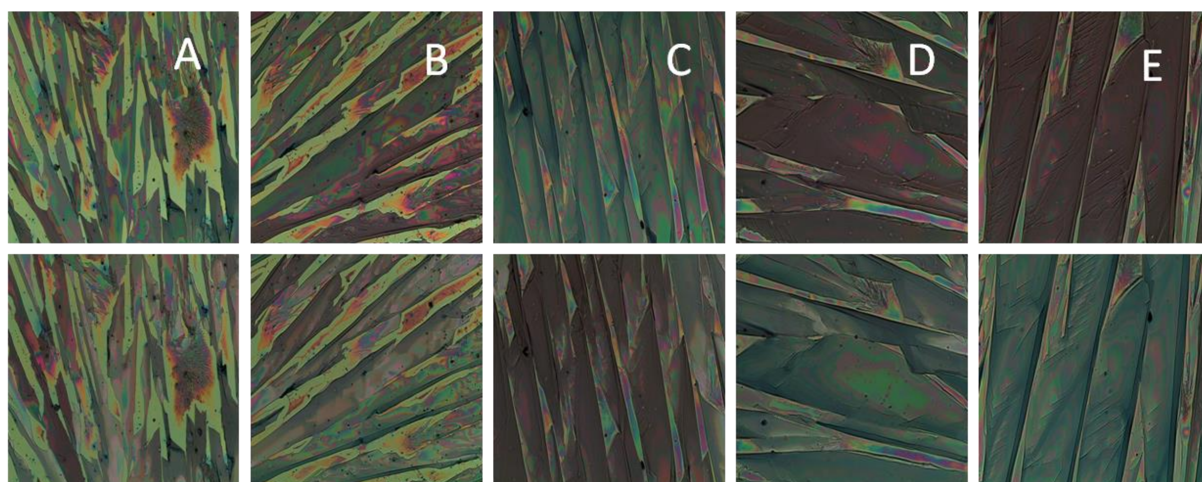


Figure 3.26: Polarized optical microscopy images of 800 µm x 800 µm (0º top upper and polarization rotated through 90º dawn lower) of pure TIPS-PEN and TIPS-PEN:Polystyrene blends according to Ps weight fraction. A) pure TIPS-PEN, B) TIPS-PEN:aPS =95:5, C) TIPS-PEN:aPS=90:10, D) Ps=15%, E) PS=20%.

It is well-known that the organic film formation and device performance are strictly influenced by the surface property of the substrate and its roughness [76, 117]. Researches demonstrate that by matching the surface free energy of the dielectric and the pentacene film, the OFET mobility is enhanced to above 2.0 $cm^2\ V^{-1}\ s^{-1}$ [117]. Since the triisopropylsilyl functionalized groups of TIPS-PEN are hydrophobic, the deposited film might be expected to grow well on PVP treated surface which has hydrophobic properties and low surface energy of about 34 $mJ\ m^{-2}$ [117, 118].

Figure 3.26 shows the optical microscope images for 2wt% pure TIPS-PEN and its blends with polystyrene on PVP surface. It is clear that the neat TIPS-PEN crystals shown in Figure 3.26A covered the substrate surface with few big voids between the crystals. Moreover, the structural properties and surface morphology characteristics

obtained from captured AFM images (Figure 3.27) explain the distribution of single and multi-layered TIPS-PEN islands grown directly on the surface. The series of isolated islands are arranged in roughly straight and parallel lines running diagonally in the image. These segregated islands seem to correspond to incomplete growth of TIPS-PEN terraces of height 1.60 to 1.75 nm which noticed for d(001) spacing. However, other crystals revealed well-ordered AFM images with defined terraces edge (Figure 3.27 bottom). The overall measured film roughness from AFM images is of order of 8.3±2.7 nm. The pure TIPS-PEN on PVP as an active layer of devices showed the values 0.158, 0.0120, and 0.0772 $cm^2\ V^{-1}\ s^{-1}$ for maximum, minimum, and average mobility respectively. Comparing the average mobility for pure TIPS-PEN on both PVP and SiO_2 surface we see that the device performance increased seven times in PVP surface compared to the hydrophilic dielectric surface.

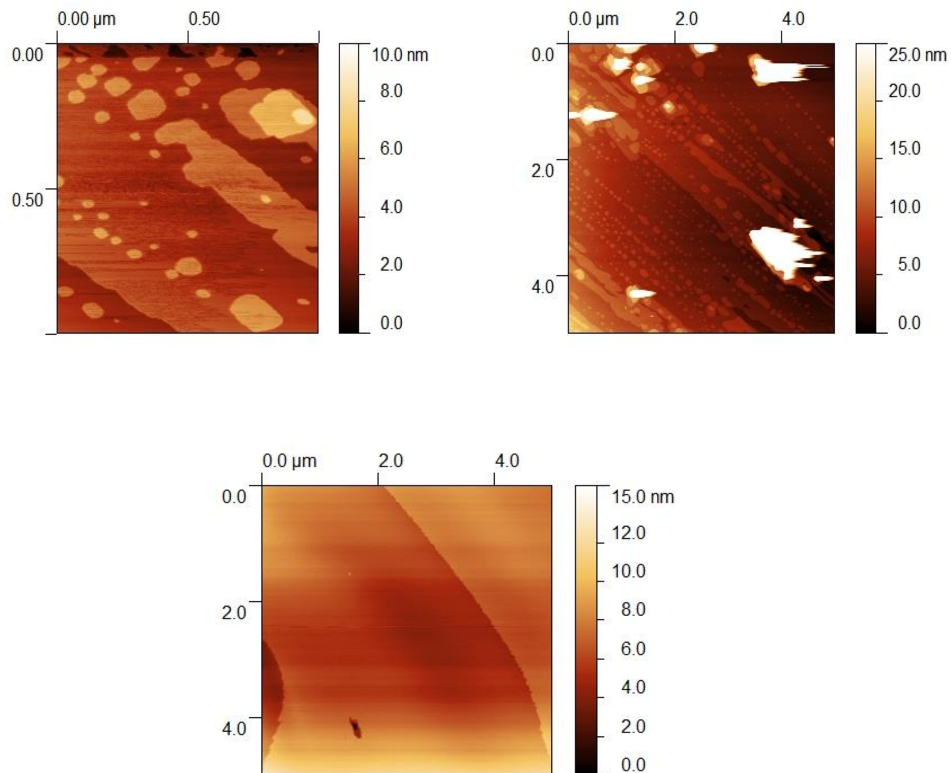


Figure 3.27: AFM images for pristine TIPS-PEN on PVP dielectric. The top images show TIPS-PEN islands distribution while the bottom image reveals well defined large terraces.

Adding polymer binder to the pure TIPS-PEN solution noticeably improves the film surface morphology and device mobility. The enhanced device mobility by aPS up to certain values of blending ratio explain that the presence of such binder dose not negatively affect the process of charge transport in the device channel [119].

Typical optical microscopy images in Figure 3.26 demonstrate the micro-size morphology evolution as a function of TIPS-PEN/aPS blend ratios ranging from 100/0 to 80/20 printed on hydrophobic PVP dielectric. Although pure TIPS-PEN gives large but still irregular shaped crystals leading to the restricted or finite coverage of devices channel. Addition of 5% aPS to the solution improves the crystal quality and shows more regular and larger crystals. Devices with such morphology have two times higher average mobility compared to neat TIPS-PEN at same experimental conditions. Likewise AFM displayed different style of images. In Figure 3.28, the scattered islands completely disappeared and replaced by well-defined ordered but wavy like terraces. Also the small and large grains on the step edges which appeared on hydrophilic substrate do not occur here and the overall surface roughness offered the value 4.0 ± 2 nm. The set of 9 devices showed the values 5.24 x $10^{-3}$and 0.48 cm^2 V^{-1} s^{-1} for minimum and maximum mobility respectively.

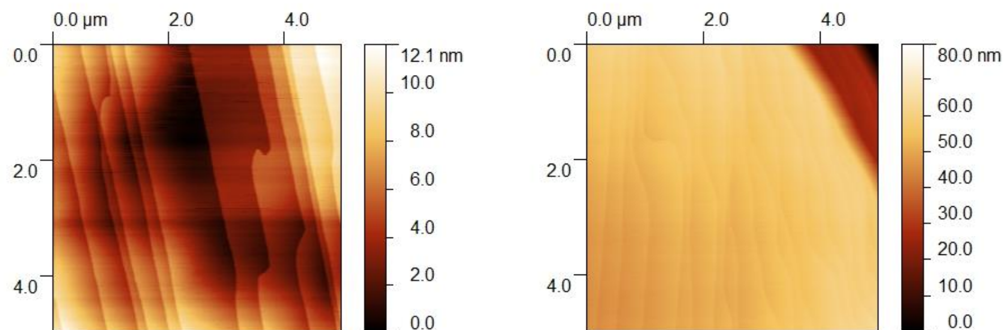


Figure 3.28: AFM images for 95:5 of TIPS-PEN/aPS blend. The wavy style of ordered film is clear and the terraces fluctuate between narrow and wide.

As the aPS concentration is increased to 10 percent, the crystal size is further enlarged and becomes more uniform, interconnected and regular. Furthermore, the brightness change become sharper in polarized optical microscope image and the regions of uniform colour become bigger, indicating that the addition of more polystyrene not

only enhance surface coverage but also promotes micro-scale long-range order of TIPS-PEN molecules. Next, we studied the AFM images of 10 percent insulating binder fabricated thin film in Figure 3.29. The surface of the drop cast film was fairly smooth, with root mean square (rms) value of roughness 1.1±0.4 nm. The terrace edges are straight, rather than wavy, again free of grains. Furthermore, the electrical (mobility) has an average value of $0.17\ cm^2\ V^{-1}\ s^{-1}$.

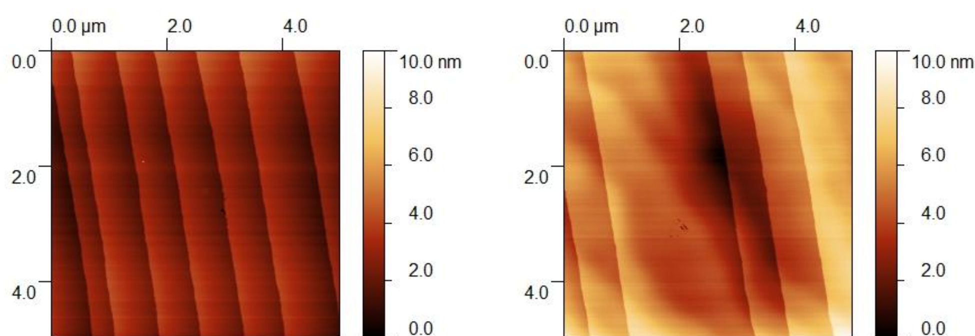


Figure 3.29: AFM images for 10 aPS percent ratio blend composition. The images exhibit straight line ordering and well defined film pattern.

TIPS-PEN/aPS blend of 85:15 on PVP surface shows organized molecular structure which indicates good molecular ordering as seen in AFM images Figure 3.30. However, the small terraces wavy style of ordering appeared again in contrast to the 10 percent of aPS and the surface roughness increased to 5.0 ± 3 nm. These features are more similar to the 5% PS blend than to the 10% PS. The mean saturated mobility was found to be $0.153\ cm^2\ V^{-1}\ s^{-1}$ and the best device showed mobility $0.454\ cm^2\ V^{-1}\ s^{-1}$ again similar to the 5 percent polystyrene concentration.

Further addition of aPS to the solution neither improved film morphology nor increased device performance. The AFM images showed either wavy style of ordering or large terraces with scattered white grains across steps and above terraces (Figure 3.31) similar to the films on hydrophilic SiO_2 substrate. The calculated device average mobility was $0.118\ cm^2\ V^{-1}s^{-1}$.

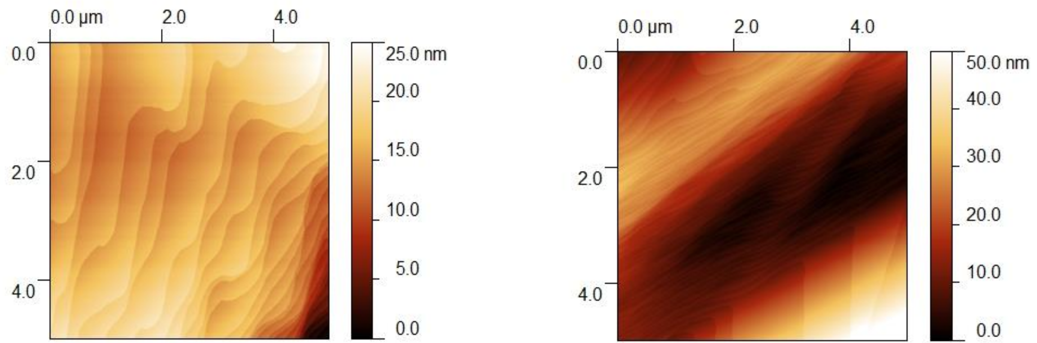


Figure 3.30: AFM images for TIPS-PEN:aPS of 85:15, the appearance of wavy style of molecular ordering again.

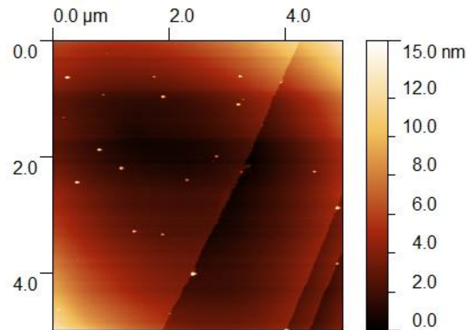


Figure 3.31: AFM images for 80/20 TIPS-PEN and PS ratio. Appearance of wide terraces with white grains again.

Additionally, the roughness of the flat terraces is marginally lower than for corresponding films grown directly onto the silicon surface and generally free from grains. The roughness of flat area between terraces for different aPS ratio on PVP showed the values 0.65±0.20, 0.38±0.13, 0.71±0.23, 0.87±0.28 nm for 5, 10, 15, and 20% for aPS respectively as depicted in Figure 3.32 below.

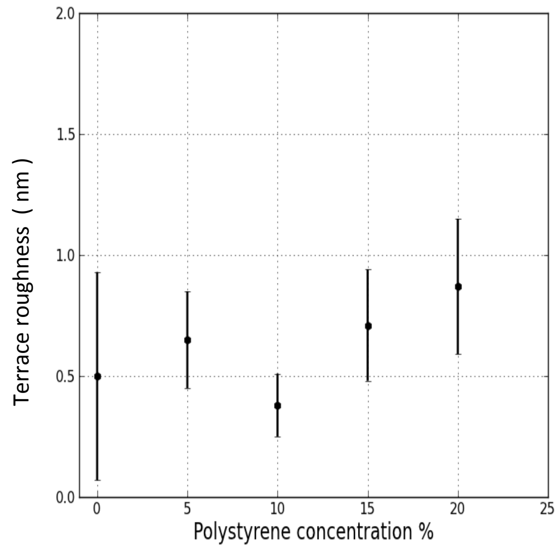


Figure 3.32: Flat area roughness of TIPS-PEN/aPS blends on PVP

A summary of mobility measurements is given in Table 3.4. For each reported conditions the average mobility was obtained for 9 devices prepared at same experimental conditions. By comparing the average mobilities for different blends we can see that these values are close to each other and around 0.15 $cm^2\ V^{-1}s^{-1}$ except for pure TIPS-PEN. The results explain that only a small amount of polystyrene, around 5-10% concentration, is sufficient to improve the device performance.

TIPS-PEN:Ps ratio	Maximum mobility $cm^2\ V^{-1}\ s^{-1}$	Minimum mobility $cm^2\ V^{-1}\ s^{-1}$	Average mobility $cm^2\ V^{-1}\ s^{-1}$	Standard deviation
100:0	0.158	0.012	0.0772	0.046
95:5	0.483	0.00052	0.142	0.147
90:10	0.252	0.043	0.17	0.081
85:15	0.454	0.0069	0.153	0.12
80:20	0.226	0.0493	0.118	0.051

Table 3.4: Summary of mobility measurements presents the average, minimum, and average mobility according to the blend composition. The average mobility was obtained for 9 devices.

Figure 3.33 shows the average, minimum, and maximum mobility for each reported blends also it presents the standard deviation for each case.

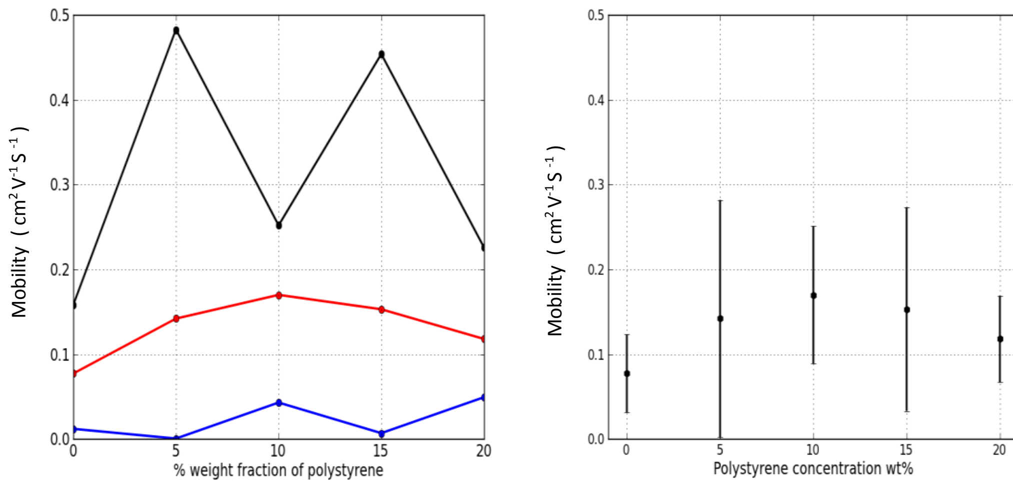


Figure 3.33: The mobility change according to TIPS-PEN/aPS blends ratio on PVP dielectric. Black curve refer to maximum mobility, red presents average mobility, and the blue is for minimum mobility. The second image (on the right) refers to the change of average mobility with standard deviations.

Table 3.5 gives the value of mean mobility of 9 symmetrical devices according to the blend composition on both PVP dielectric and SiO_2 surface and Figure 3.34 is plotted according to the mobility mean values on SiO_2 and PVP.

TIPS-PEN: aPS ratio	μ_{ave} on PVP cm^2 V^{-1} s^{-1}	SD	μ_{ave} on SiO_2 cm^2 V^{-1} s^{-1}	SD
100:0	0.0772	0.046	0.013	
95:5	0.142	0.147	0.0027	0.0016
90:10	0.17	0.081	0.0032	0.0021
85:15	0.153	0.12	0.034	0.0013
80:20	0.118	0.051	0.016	0.0058

Table 3.5: Comparison of mean saturated mobility of pure TIPS-PEN and its blend with polystyrene on PVP and SiO_2.

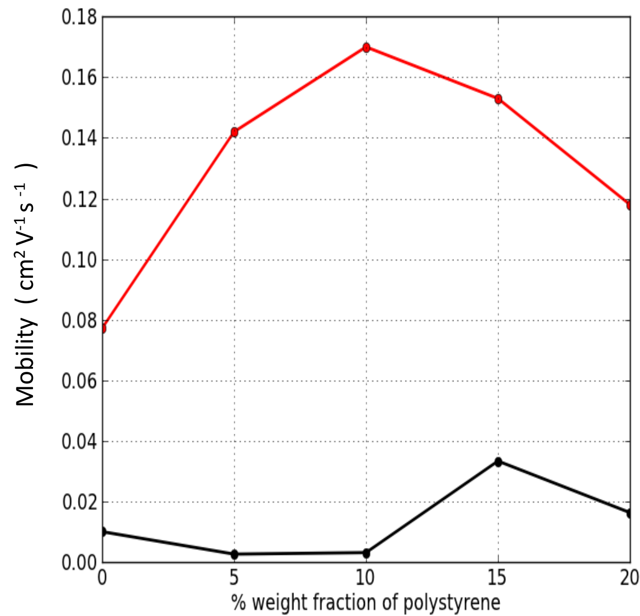


Figure 3.34: Average mobility changes of transistors according to the active layer composition of TIPS-PEN and its blends of polystyrene on PVP (red curve) and SiO_2 dielectric (black curve).

The surface properties of the substrate not only play a vital role in coating of deposited film, but also in crystalline morphology and resulting device performance. Particularly, PVP exhibits excellent compatibility with TIPS-PEN as its offer adequate surface for adhesion of the hydrophobic silyl groups of TIPS-PEN due to its low surface energy 34.6 mJ m^{-2} [117, 118]. This is consistent with polarized optical microscope images obtained from crystal growth on PVP and with surface nano-sized structure of AFM images. Table 3.5 and Figure 3.34 show the comparison of the average mobility values in both SiO_2 and PVP surfaces.

The mobility improvement on PVP is clear where its values are enhanced for both pure and blended devices compared to SiO_2 dielectric. Specifically, for neat TIPS-PEN the mobility was increased 7 times when PVP used as a dielectric surface. Also, only an addition of 5% Ps to the solution (fixing to 2 wt%) the mobility went up more than 50 times. On the other hand, when we compare AFM, OM images for pure TIPS-PEN and aPS blends on PVP we see a dramatic improvements in crystal size, orientation, and film morphology.

Furthermore, the increase of mobility after addition of aPS is very clear. For instance, the mobility enhanced two times only by the blending 10% aPS with the pristine TIPS-PEN solution.

In addition to the polymer device uniformity and solution rheology, Hamadani *et al* (2007) and Ohe *et al*.(2009) [87, 93] suggested that the addition of polymer binder leads to longer evaporation rate and slower drying process and consequently to a different TIPS-PEN morphology. Yoon et al. assumed that the polymer binder affected the film formation process and acts indirectly as purification method [120].

3.11 Conclusions

We have presented a systematic study of the influence of binary solvents on TIPS-PEN film formation and device performance. In this study, the effect of anisole:decane solvent mixtures as a function of volume ratio for drop-casted TIPS-pentacene thin film was investigated by OM, AFM and OFET measurements. It was found that the addition of up to 20% decane has no dramatic impacts on micro-scale crystal pattern but has a significant influence on nanoscale morphology. Moreover, addition of decane beyond 15% causes a decrease in field effect mobility. We found that the anisole:decane blend ratio 91:9 is the suitable blend composition for best film morphology and device performance were obtained.

Furthermore, the effect of the TIPS-PEN : polystyrene ratio from 100:0 to 80:20 for drop-cast thin film was similarly investigated. It was found that addition of polystyrene has a significant effect on both macroscopic crystal properties such as surface coverage, unity of orientation, long range orders and average field-effect mobility, and also changes the surface morphology and layer ordering on the nano-scale.

Finally, the effect of dielectric surface on the film formation and device mobility was investigated in detail. It was found that the surface properties of dielectric material play a vital role not only in coating of deposited film, but also in device mobility and crystalline morphology. The device mobility on PVP was dramatically improved where its values are enhanced for both pure and blended devices compared to SiO_2 dielectric. For pure TIPS-PEN the mobility was increased 7 times when PVP used as a dielectric surface. Likewise, only an addition of 5% Ps to the solution (fixing to 2 wt%) the mobility went up more than 50 times. Moreover, when we compare AFM, OM images for pure TIPS-PEN and aPS blends on PVP we see a dramatic improvements in crystal size, orientation, and film morphology. These results show that the hydrophobic surface PVP was more suitable and compatible for TIPS-PEN film and its blends when compared to the hydrophilic SiO_2 dielectric.
Our study provides a good method for controlling the film morphology and molecular structure of OSM semiconductors TIPS-PEN for the direct fabrication of high-performance organic electronics.

Chapter Four

In_2O_3 thin film transistors

4.1 Introduction

Metal oxide materials have been researched extensively in recent years, particularly with regard to the commercialization of oxide-based electronics for use in display technology and as an alternative material for transistor applications [27, 121, 122]. Oxide based thin film transistors have a performance advantage related to their high carrier mobility, low cost production and, easy processing at relatively low and ambient temperature. Furthermore, because of large band gaps and resultant optical transparency [32], their use in transparent electronics and optical displays becomes possible and of great interest [123].

A number of metal-oxide based TFTs such as indium oxide (In_2O_3), Indium zinc oxide(IZO), zinc oxide (ZnO), zinc tin oxide (ZTO), and indium gallium zinc oxide (IGZO) have demonstrated high mobility's and reasonable device performance at low or room temperature, using different device dimensions and various fabrication methods [124-133].

Indium oxide is a n-type oxide semiconductor of band gap (3.6eV) at room temperature and indium oxide thin films superior to other transparent oxide counterparts such as ZnO and SnO_2, particularly due to its high mobility of 10–75 cm^2 V^{-1} s^{-1} at a carrier density of 10^{19}–10^{20} cm^{-3}[134-136]. Furthermore, indium oxide has high optical transmittance in the visible region and its high electrical performance makes it a superior candidate for the oxide TFT active layer.

Jiao *et al.* [137] fabricated a bottom-gate TFT by using amorphous In_2O_3 as the n-channel device on SiO_2/Si substrates by direct current magnetron sputtering at room temperature. They noticed that, by controlling the sputtering time, In_2O_3 can be grown into the amorphous phase with better film uniformity, smoother surface, high performance and large on-off ratio. Kim *et al.* [131] found that In_2O_3 devices on SiO_2

gate dielectrics exhibit reasonable field effect of mobility of around 0.7 $cm^2 V^{-1} s^{-1}$ and on-off ratio 10^6 for operating voltages in the 0.0 - 100 V range. In contrast to the results for a SiO_2 dielectric, the In_2O_3-organic hybrid TFTs fabricated with the high- *k* organic (self-assembled nanodielectric –SAND) dielectrics exhibit excellent *I-V* characteristics and their analysis showed that the n+-Si/SAND/In_2O_3/Au TFT electrical performance reveals large saturation-regime field-effect nobilities, up to 43.7 $cm^2 V^{-1} s^{-1}$ with on-off ratio around 10^6.

Faber *et al.* [138] used ultrasonic spray pyrolysis to demonstrate the growth of polycrystalline, highly uniform indium oxide films at temperatures in the range of 200-300 °C in air. They noticed strong dependence of electron mobility on deposition temperature and found the fabricated transistor at 250 °C revealed good mobility in the range 15-20 $cm^2 V^{-1} s^{-1}$ and high on-off current ratio of order of 10^6. Furthermore, Han *et al.* [27] used spin coating to fabricate indium oxide TFT to study the effect of the annealing atmosphere on the In_2O_3 film's optical, morphological, chemical, and electrical properties as well as the TFT performance. The thin film annealed at 500 °C under air showed high field effect mobility around 55 $cm^2 V^{-1}s^{-1}$ and I_{on}/I_{off} ratio of 10^7. Indium oxide film annealed under O_2/O_3 at temperature between 200 - 300 °C exhibited mobilities 0.85 - 22 $cm^2 V^{-1} s^{-1}$ and $I_{on}/I_{off} \sim 10^5 – 10^6$.

Moreover, indium oxide TFT's show electrical performance that is dependent on the active layer thickness as reported by Noh *et al.* [128] which is attributed to the total number of carrier in the active layer in TFT. The performance dependence of indium oxide TFT on the film thickness such as the carrier mobility, threshold voltage, turn on voltage, on–off currents and consequently on-off ratio, which is also corroborate with other metal oxide TFT [127, 139-144].

However, some issues such as bias stress instability [28, 145-153], effect of surface roughness on device performance [154, 155], short channel length effects [130, 140, 156], and contact resistance effect [156, 157] have been explored or improved by then.

In this chapter we study the surface structure and morphology of indium oxide thin film using AFM in intermittent contact mode for both single and double spin coating film. The main objective of this study was to develop high performance n-type indium based metal oxide TFT transistors. The device output and transfer characteristics were used to extract out the transistor electric performance such as mobility, on-off ratio, threshold voltage (V_{th}), and turn on voltage. The impact of active layer thickness (single and double) on V_{th}, V_{on} , I_{on}, I_{off} and transistor mobility is discussed. Furthermore, in the second part we report the bias stress effect on the top contact bottom gate indium oxide device stability over prolonged bias stress and the impact of it on TFT transfer characteristics and drain current during the stressed state. The device recovery after stress release and the proposed mechanism behind bias stress and recovery is discussed in the context of our experimental data. EFM evidence about stress and recovery is also mentioned. The primary aim of this part is the study of the device stability when it is subjected to the long term bias stress. Our study showed that the investigated transistors return to their original state and the threshold voltage shifts recovered when the devices relaxed. This result suggested that the charge trapping at the interface or bulk dielectric is the main mechanism behind threshold voltage shifts.

The surface potential SP profiles provide a detailed picture of the local potential within working transistor channel, allowing for separation of device characteristics in both linear and saturation regime. The SP and 2D images obtained by SKPM (Scanning Kelvin Probe Microscopy) as a function of drain bias at fixed gate voltage will be discussed in detail. Moreover, the gate bias effect at constant drain voltage for linear and saturation regime will be mentioned in the third parts of this chapter. We observe a smooth film homogeneously covering the channel region between source and drain without any discontinuity, voids or cracks. We imaged the investigated devices at linear and saturation region, performing a complete profiles, showing a symmetrical and small drops at both contacts edges and confirming small contact resistance.

Finally, 2D drift-diffusion simulations of the In_2O_3 TFTs incorporating Al contact diffusion were employed to verify and support experimental results. An Al diffusion region of 6 μm was detected. Also, modelling of potential profiles for various drain bias is presented and we see good consistency between experimental data and simulation results. Likewise, we show that AFM topography measurements with a biased drain electrode also can be used to specify the contact diffusion.

4.2 Experimental details

Here we review the main experimental techniques used in this chapter regarding the fabrication, characterisation, bonding and measurements of Indium oxide thin films and devices. The deposition of film and transistor fabrication was carried out by the group of Prof. Thomas Anthopoulos. Imperial College, using spin coating.

4.2.1 Preparation procedure

For solution-processable indium oxide, the In_2O_3 precursor solution was prepared by dissolving anhydrous indium nitrate [$In(NO_3)_3$] (99% Indium Corporation) in deionized (DI) water at a concentration of 30 mg/mL. The solution was stirred at room temperature for 60 min before use.

For the fabrication of low-temperature aqeuous-based (water) In_2O_3 TFT, the semiconductor thin-film deposition was carried out by spin-casting the In_2O_3 precursor solution onto the Si substrates at 3000 rpm for 30 sec in ambient air, followed by a post-deposition thermal-annealing process for 30 min at 200 °C in ambient air. The thin-film deposition and formation cycle was carried out twice in order to accomplish a dense and continuous In_2O_3 layer. The In_2O_3 TFTs were finally completed by thermal evaporation of 40 nm thick Al top source and drain electrodes through a shadow mask. The sample size was 2 cm x 2 cm and each sample included 58 devices.

4.2.2 Device Characterization, bonding, and measurements

1. Before starting the experiments the size of specimen (2 cm x 2 cm which includes 98 transistors) was modified (about 8 mm x 8 mm) by cleaving it in our clean room and under ambient atmosphere.
2. Cares was taken during specimen cleaving to keep the specified sample as it was (using gloves, clean cleaving tools,..). Cleaving was used in preference to scribing to minimise the number of fine particles produced. Then the sample was exposed directly to N_2 flush to remove any remaining tiny particle residues from the surface.

3. Afterward the transistors were bonded with gold wire of diameter 0.06 mm via high quality silver paint under optical microscope. Figure 4.1 shows the transistor bonding.

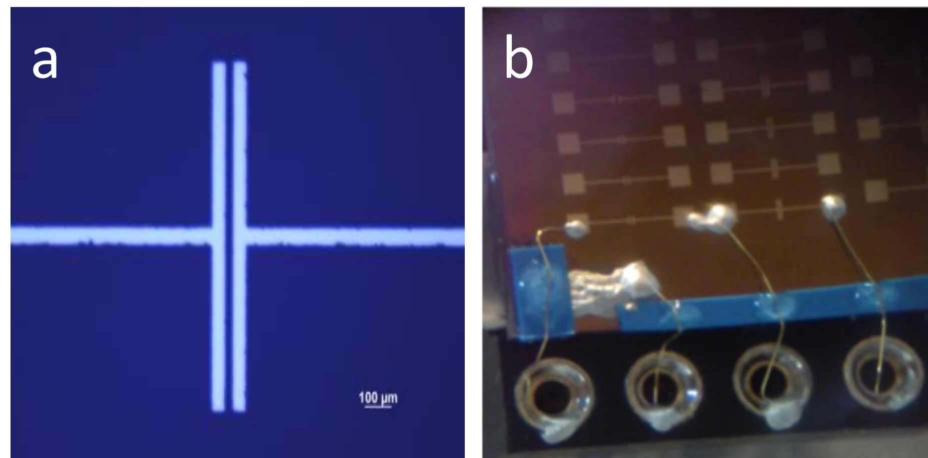


Figure 4.1: a) The specific transistor before bonding, b) after bonding with gold wire

4. Two devices were made for each case (Figure 4.1b), with each device of different W and L (different dimensions) in order to see how the device performance is correlates with transistor dimension.
5. Once the device bonding had been performed, the sample was stored under vacuum to prevent degradation via interaction with atmospheric gases or ambient humidity.

6. Device *I-V* data was monitored with a Keithley Picoammeter-6487- using a python program. Output and transfer characteristics of transistors were plotted using other programs.
7. A Veeco Nano Scope IIIa was employed for electrostatic force microscopy (EFM) measurements, during which the surface topography in intermittent contact mode AFM and its surface potential image captured at the same time.

4.3 Indium oxide surface morphology

The surface morphology has an important effect on the device electrical performance. The smooth and uniform surface morphology can give good interface between the source- drain electrodes and the channel layer [125, 141]. Rough interfaces can lead to trap states and defects that degrade contacts and the channel mobility so the material morphology and the influence of grain boundaries must be considered[32].

Grain boundaries act as potential barriers which hinder charge transport. Nano-particle based devices in general have performance issues which are directly correlated to the structure of deposited film and to the method of deposition. For instance, it is believed that the poor device performance may be attributed to the number of voids in the nano-particulate film and on the semiconductor/interface roughness [158] . The rough channel /dielectric interface decreases the drain current and device mobility because it inhibits transport of accumulated electrons [159]. Also the voids and an increase of roughness probably enhance the creation of charge trapping which in turn causes poor current flow through the transistor channel. Okamura *et al.* (2008) and Okamura *et al.* (2010) [155, 158] suggested that even very small nanometre changes in roughness can cause variation in device mobility up to an order of magnitude. They also noticed that an interface roughness smaller than the accumulation layer thickness leads to higher mobility. However, the device interface roughness equal or greater than accumulation layer thickness acts like a trap of carriers and significantly prevents induced carriers transport through the channel.

Figure 4.2 shows AFM images of indium oxide film captured between transistor electrodes. The root mean square (RMS) surface roughness from topographical AFM images can be taken as a rough an approximation to the interface roughness if we assume conformal behaviour [158]. The roughness of each film measured by taking 5x5 micron AFM images and calculated with using Gwyddion software.

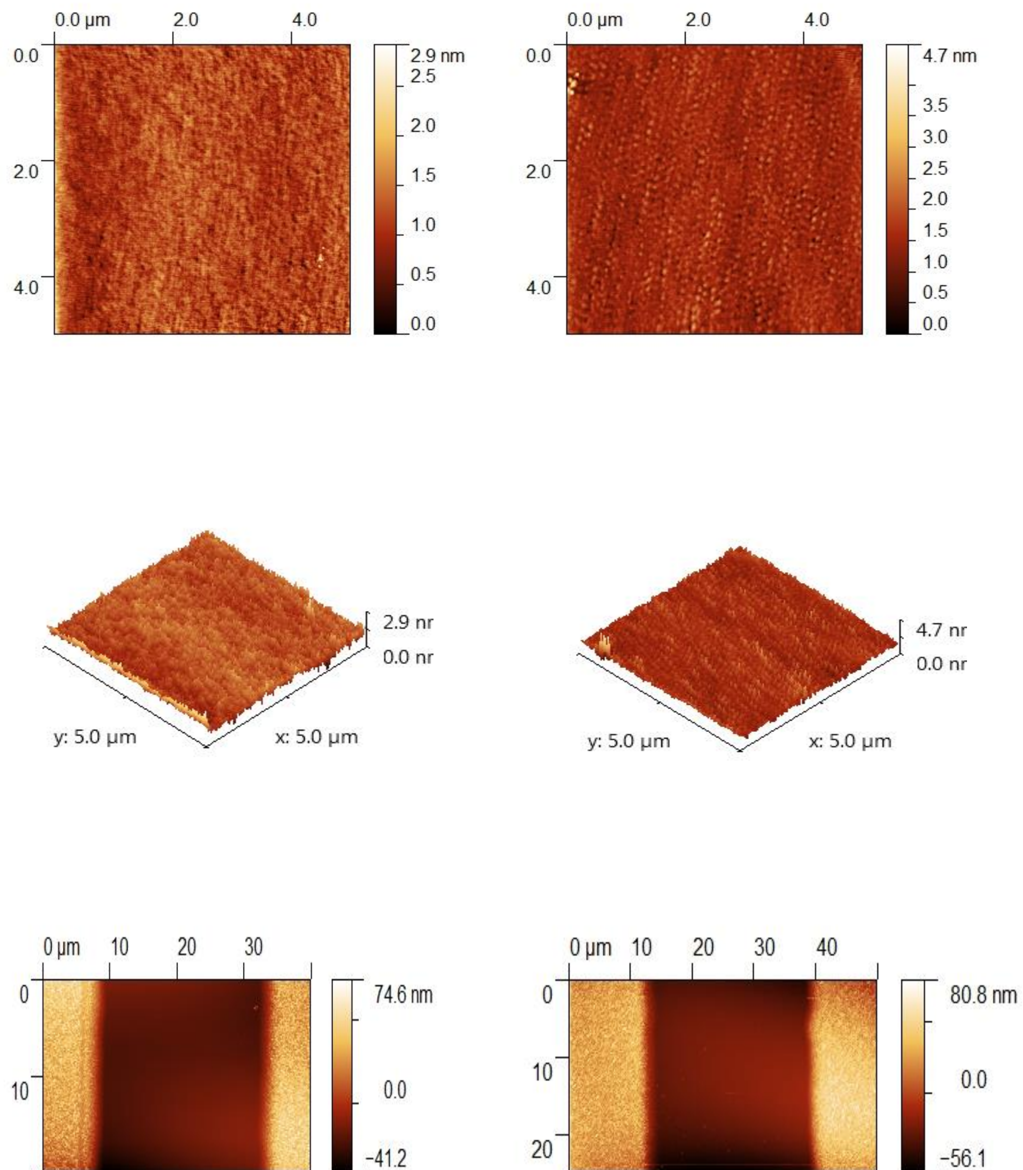


Figure 4.2: AFM images of single spin coating (top left) and double spin coating (top right) film of indium oxide. The middle images are the corresponding single and double spin in three dimensions. The bottom images are for corresponding devices with Al electrodes.

The surface properties of In_2O_3 film present a uniform, smooth, and highly textured well patterned morphology with average RMS value of 0.56±0.06 nm and 1.23±0.13 nm for single and double spin coating respectively. It appears that the 2D image of the thicker (double spin coating) film has more grain structure, while it disappears in the thinner one (single spin coating). Beena *et al.* [160] demonstrated that the conductivity of the film increases generally when the film become smoother, ordered and crystalline because the trapping and scattering of carriers become less. The quality of the active layer is crucial for suitable TFT performance which influenced by film morphology. Figure 4.2 also shows the surface topography of working devices during our experiments which depicts continuous and uniform films between source and drain with no voids or cracks in between.

Part 1

4.4 Electric characterization of In_2O_3 TFT

The common measurements used to describe the thin film transistor performance are: output characteristics, transfer characteristics and device mobility.

4.4.1 The output characteristic

The output characteristic is obtained when the drain current is measured as a function of drain voltage for different gate bias. As the applied gate voltage V_g changes the drain current I_d versus V_d curve shifts.

$$I_d = \left(\frac{W}{L}\right)\mu C_i \left[(V_g - V_{th})V_d - \frac{1}{2}V_d^2\right] \quad (4.1)$$

Accordingly, families of curves for discrete values of V_g can be generated. Figure 4.4B shows the output characteristic of single spin coating In_2O_3 based TFT of channel width W= 1000µm and length L= 30 µm denoted as W1000L30S, for which the gate bias was varied from 0 to 10V in 1V increments. The I-V curves clearly reveal the linear, pinch off and saturation region in good agreements with standard field effect transistor theory.

The device operates as an n-channel which is clear from the fact that only a very little drain current occurred at zero gate bias and a positive gate bias required to generate carriers and induced conducting channel with channel conductivity increased by positive gate bias[161, 162]. In addition, we observe a strong saturation at the post pinch off position evidenced by flatness of the slope for each curve at large V_d value. This means that the complete thickness of the channel layer is depleted from free electrons and the device exhibit a large resistance (reciprocal of *I-V* curve slope) [163, 164] that required for circuit applications since transistors exhibiting this property possess a large output impedance. Furthermore, the channel resistivity can be estimated from the linear slope of output characteristic at zero gate bias [136, 165]. However, other devices showed a slight decrease in saturation current at large gate and drain voltage as shown in Figure 4.3.

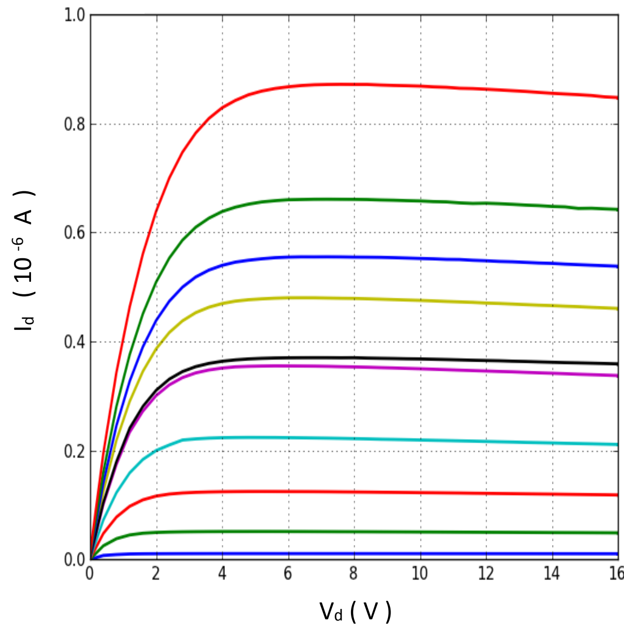


Figure 4.3: The output characteristic of single spin coating transistor of dimension W1500L40S. The gate bias V_g = 1, 2, ..10V step 1V.

Device self-heating at high bias probably is the main origin of this effect. Similar results were reported on other metal oxide transistor [122].

4.4.2 The transfer characteristics

Parameters used to describe the performance of a transistor can be extracted from its measured transfer characteristic. These include channel mobility μ, I_{on}/I_{off} ratio, threshold voltage V_{th}, turn on voltage V_{on}, and sub threshold voltage swing.

The transfer characteristic is obtained when the gate bias is swept at fixed drain voltage, selected to ensure that the device working in saturation region.
For saturation region ($V_d \geq V_g - V_{th}$), Equation 4.1 can be written as:

$$I_d = \frac{1}{2}\mu_{Sat}\, C_i\, \frac{W}{L}\left(V_g - V_{th}\right)^2 \qquad (4.2)$$

Figure 4.4D shows the square root dependence of drain current with gate voltage which governs by Equation 4.2. The device mobility can be extracted experimentally from slop of $\sqrt{I_d}$ versus V_g. However, the threshold voltage obtained by fitting the straight line of the square root of drain current versus gate voltages from the transfer plot.

The indicated device W1000L30S in Figure 4.4D showed saturation mobility μ_{Sat} = 0.24±0.069 $cm^2\ V^{-1}\ s^{-1}$ V_{th} = 2.524 V, I_{on}/I_{off} = 10^{4}, and V_{on}= 2.21 V. The device is working in enhancement mode which is preferable to depletion mode because it is not necessary to apply gate bias to switch off or turn off the transistor. Also the circuit design is easier and power dissipation is lower [124, 143, 166]. The low positive threshold voltage for this device infers low trap density, the contamination induced process is negligible and optimal carrier density in the channel layer [165, 167].

In addition, indium oxide exhibits n-channel properties because electrons are generated only at positive gate bias. The mobility alone does not explain the whole picture of the device performance. For a good transistor other parameters should be considered such as I_{on}/I_{off}, V_{on}, V_{th} . Table 4.1 shows the electrical performance for some single and double spin coating devices. Comparing W1000L30D and W1000L30S devices we see the better saturation mobility for double spin transistor which is 5 times greater than single spin coating device. The same situation is true with W1000L20 devices comparison.

W/L	μ_{sat} $cm^2 V^{-1} s^{-1}$	V_{th} Volt	V_{on} Volt	I_{on}/I_{off}	Devices
200µm/40µm Double spin	0.845±0.11	-0.20V	-4.45V	10^5	W200L40D
1000µm/30µm Double spin	1.143±0.13	-6.65V	-7.76V	10^4	W1000L30D
1000µm/20µm Double spin	1.25±0.081	-15.8V	> -19V	10^6	W1000L20D
1000µm/30µm Single spin	0.24±0.069	2.5V	2.12V	10^5	W1000L30S
1000µm /20µm Single spin	0.215±0.07	-4.75V	-5.75V	10^5	W1000L20S
1500µm /40µm Single spin	0.153±0.09	9.3V	8.6V	10^4	W1500L40S
1500µm/100µm Double spin	0.77±0.082	0.8V	-3.65V	10^5	W1500L100D

Table 4.1: The electric performance of In_2O_3 devices of 100nm thick SiO_2 dielectric according to the device dimension W and L and film thickness.

4.5 Gradual channel model for threshold voltage and mobility extraction

Once the TFT is electrically characterized, the device mobility and threshold voltage can be extracted to quantify the performance. It should be mentioned at this point that for every device in this thesis this is performed by the standard and accepted transconductance technique (such in Figure 4.4D). The reason behind this is that the extracted values may be used for comparison with other devices in this thesis or for other groups.

An alternative approach to obtain values for the saturation mobility and threshold voltage is to fit the Equation 4.2 for the gradual channel model to the experimental transfer curve. Figure 4.4F shows the fit obtained to the experimental data for indium oxide TFT described in Figure 4.4D. The red dots represent the fitting curve that confirms good agreement with the experimental obtained transfer curve (black line) for indicated W1000L30S device. The fit is good for $V_g > V_{on}$ but deviate for $V_g < V_{on}$.

The fitting of transfer curve according to the model gives a correct value of the real voltage that need to turn on the device as well because the channel in negative gate bias in this device is fully depleted. Hence, from fitting results we can estimate V_{on} value as a third parameter which improves the outcome of the needed parameters. The result of extracted fitting parameters for single spin coating device W1000L30S are V_{th} = 3 V and μ_{sat} = 0.22 cm^2 V^{-1} s^{-1} which is in good agreements to the obtained value mentioned above in Table.4.1.

4.6 Effects of active layer thickness.

The thickness of the conducting layer has an impact on device performance. However, using a solution deposition process to carry out a study on a full range of thickness-dependent performance is somewhat difficult. This is because:

1. Increasing precursor concentration to increase final thickness, also affects film quality.

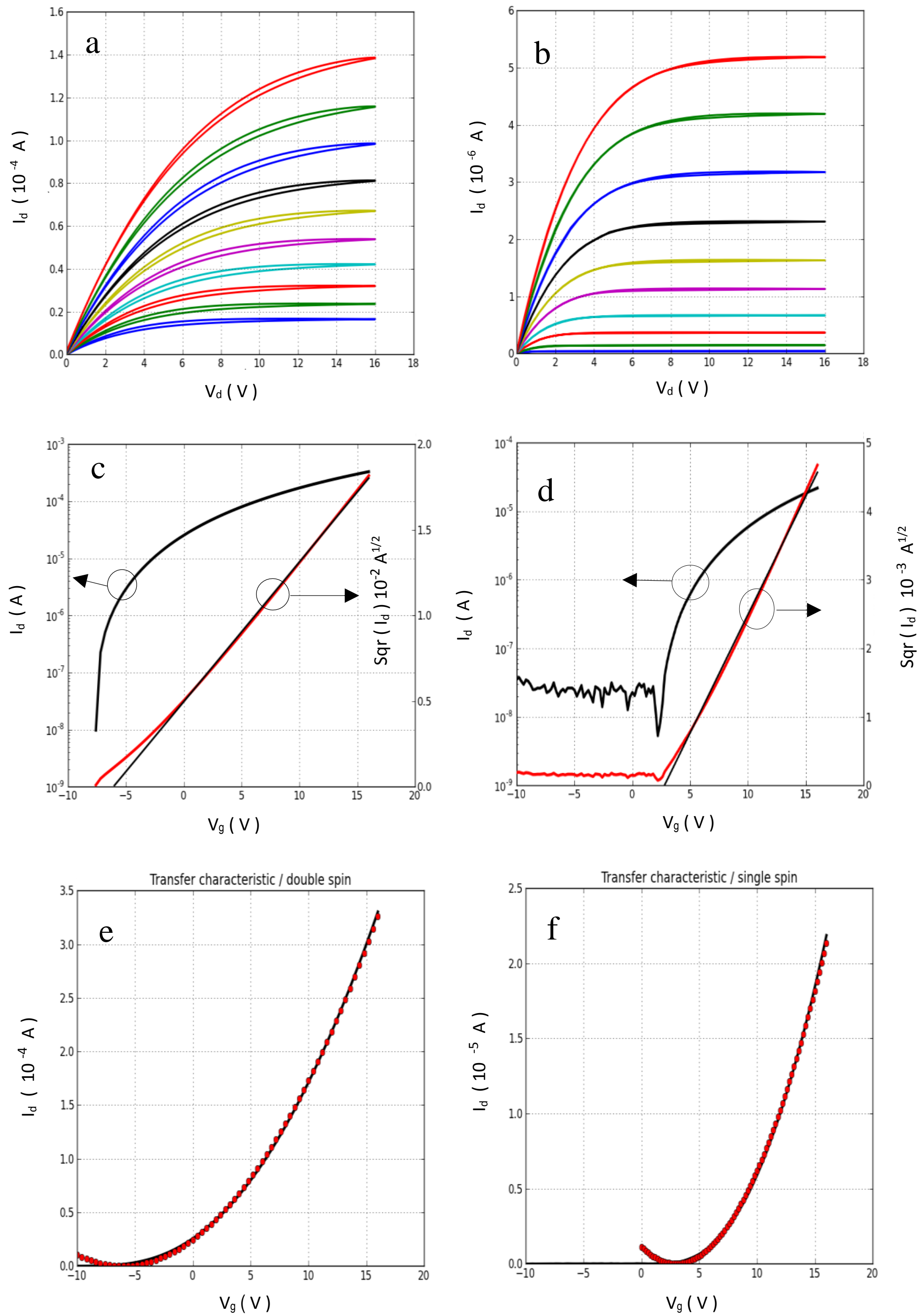


Figure 4.4: The output characteristic of: a), double spin coating W1000L30D, b), single spin coating W1000L30S. The gate bias V_g = 1, 2,3,…10V step 1V for both doable and single spin. c and d), the corresponding transfer characteristics at V_d =10V. The figures (e and f) represents the fitting of transfer characteristics according to equation 4.2 at saturation region. The obtained V_{th} and μ_{sat} values from fitting are -6.07V, 1.17 cm^2 V^{-1} s^{-1} and 3 V, 0.22 cm^2 V^{-1} s^{-1} for double and single spin respectively which is very close to table 4.1 corresponding values. The film thickness for double spin coating is about 7-8nm and around 4nm for single spin coating.

2. If carrying out more steps using a specific concentration, other parameters, such as thermal-annealing time, have influence on electrical performance. So the change in thickness won't be the only factor that needs to be considered.

The result for double spin-coating here, the value is close to the highest performance that can be obtained at 200 ^oC and the film thickness is around 7-8 nm (Lin, Yen-Hung, imperial college-London). The electrical performance of amorphous oxide based semiconductor thin film transistor is a strong function of semiconductor layer thickness [127, 168]. Figure 4.4 shows the comparison of output and transfer characteristics of single and double spin coating TFT (of dimension W1000L30 for both) which have different indium oxide thickness. The modulation of drain current according to gate bias is apparent which refer to clear field effect by gate and drain bias.

It is clear that the increasing the active layer thickness leads to the higher off current [131] and lower threshold voltage. We can expect larger number of free carriers in the bulk of a thicker film which is consistent with a higher off current in the double spin coating transistor. The variation of off current with thickness d_a is attributed to the decrease of active layer resistance (channel resistance) with increasing d_a which causes faster flow of electron from source to pass the drain terminal [143].

As the thickness of the In_2O_3 active layer (from single to double) is increased, for our limited data set, the mobility is increased, threshold voltage is shifted toward negative direction, off-drain current is increased, and on-drain current is less pronounced. These observations is consistent well with the other works in the metal oxide field [139, 169].

We have studied the effect of channel thickness on another couple of transistors of dimension W1000L20 as depicted on Figure 4.5. The trends after comparing thin and thicker devices reveal the same situation which is mentioned above, increase of drain currents, shift of threshold voltage toward negative direction, increase of off currents, small changes of on currents, and the increase of mobility from $\mu_{sat} = 0.215 \pm 0.07$ $cm^2\ V^{-1}\ s^{-1}$ to $\mu_{sat} = 1.25 \pm 0.081$ $cm^2\ V^{-1}\ s^{-1}$ for single and double spin coating respectively.

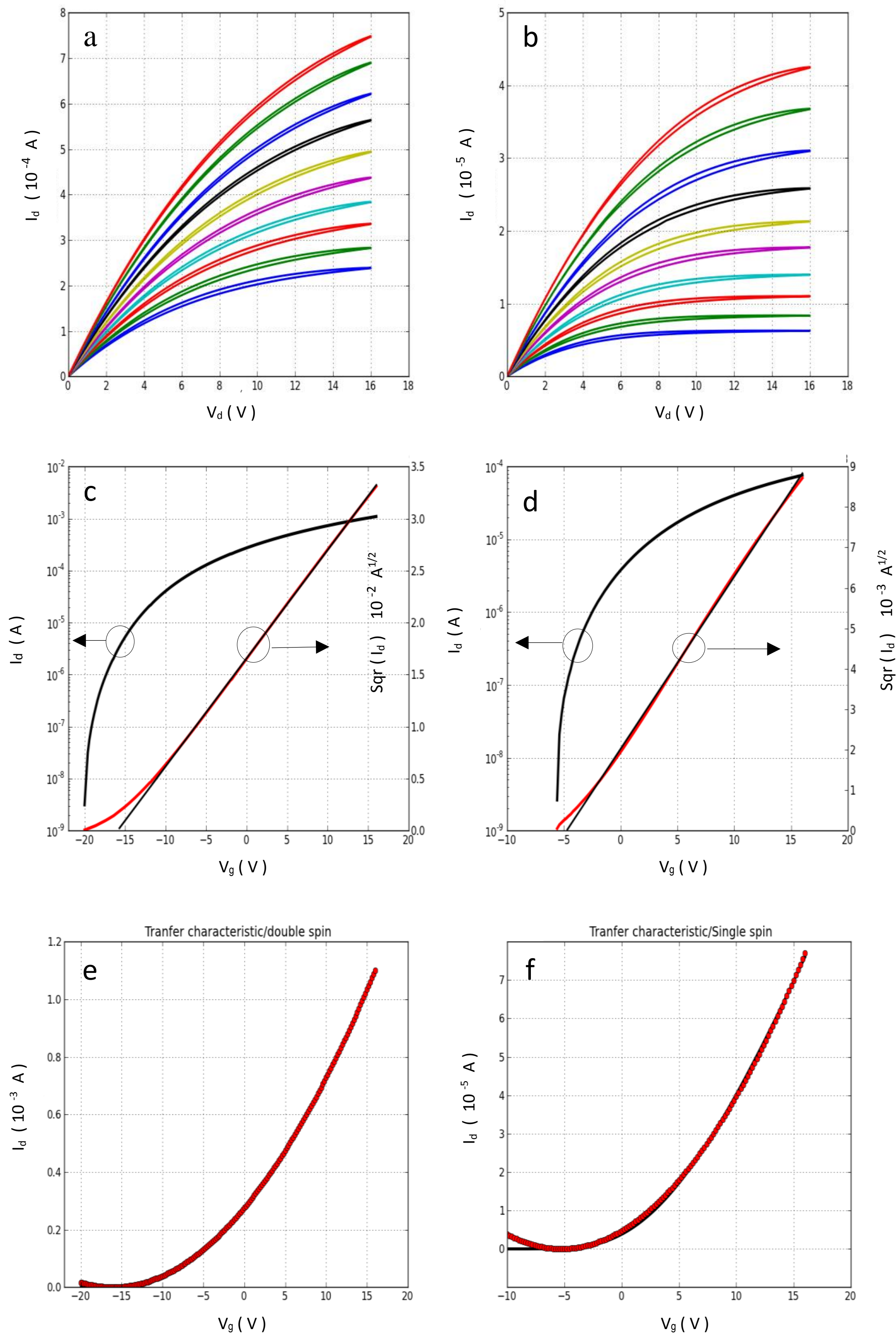


Figure 4.5: The output characteristic at V_g = 1, 2,3,…10 V step 1 V of double (a) and single (b) spin coating thin film transistor of dimension W1000L20. c and d), the corresponding transfer characteristics at V_d = 10V. The bottom figures (e and f) represent the fitting of transfer characteristics according to equation 4-2 at saturation region. The obtained Vth and μ_{sat} values from fitting are -16.04V, 1.19 cm^2 V^{-1} s^{-1} and -5.23V, 0.2 cm^2 V^{-1} s^{-1} for double and single spin coating respectively.

In this couple of devices we see the single spin device working slightly in depletion region with V_{on} = -5.75 V but the thicker one working at V_{on} = -20 V. The threshold voltages shifts from -4.75 to -15.8 V which obtained from linear fitting extrapolation down to x-axis table 4.1, again in good agreements with threshold voltage values -5.23, -16.04 V obtained from fitting parameters of Figure 4.5f and Figure 4.5e.

Also other devices showed same characteristics when we compared the thin (single spin) with a thicker one (double spin) for the same device dimensions.

Part 2:

4.7 Bias stress and device instability

In order for an indium oxide TFT to have practical value, it must be stable with respect to operating conditions, which means their figures of merit should change the least possible under device operation. One of the methods used for testing the stability of thin film device is to study the effect of varying positive/negative bias stress. Bias stress measurements probe the operational instability of TFT during application of prolonged gate bias and simulate the conditions for long term transistor operation.

The electrical stability of thin film transistors is important for active displays operation for stable display performance. Bias stress instability leads to the threshold voltage shift with time during application of gate voltage which in turn causes a decrease in drain current. Therefore, the generation and recovery of these instabilities over time may leads to time dependent operation of the device and finally disfunction. It is believed that the bias stress leads to some instabilities such as charge trapping, defects in the active channel layer, in the gate dielectric, and at the active layer/dielectric interface. Mechanisms for this degradation have been proposed. For instance, Nomura *et al*. [170] in the study of a-In-Ga-Zn-O suggested that the shallow traps are the origin of large threshold voltage shift (~ 10 V) and subthreshold deterioration observed in unannealed devices, while deep traps are responsible for small shifts (~ 1 V) and not removed by annealing. On the other hand, Lei *et al.*(2008) and Suresh *et al.*(2008) [146, 149] attributed degradation to charge trapping in the channel/dielectric interface and bulk semiconductor.

The purpose of this section is to explore the effect of bias stress on In_2O_3 devices as a n-type metal oxide material used for TFT fabrication. During our experiments and in order to test the electrical stability of indium oxide TFTs, the impact of prolonged positive gate bias on the drain current and threshold voltage was investigated after giving the sample enough time to reach equilibrium with the surrounding atmosphere. With the source electrode grounded and fixed drain bias, the applied gate bias was subjected to a given bias for chosen time period, then interrupted for very short time to record the transfer characteristics of the TFT under investigation.

The stressing time was varied from some seconds to hours with the sample kept dark and in enclosure at room temperature. Figure 4.6 shows a set of transfer curves of TFT transistor W1000L30S.

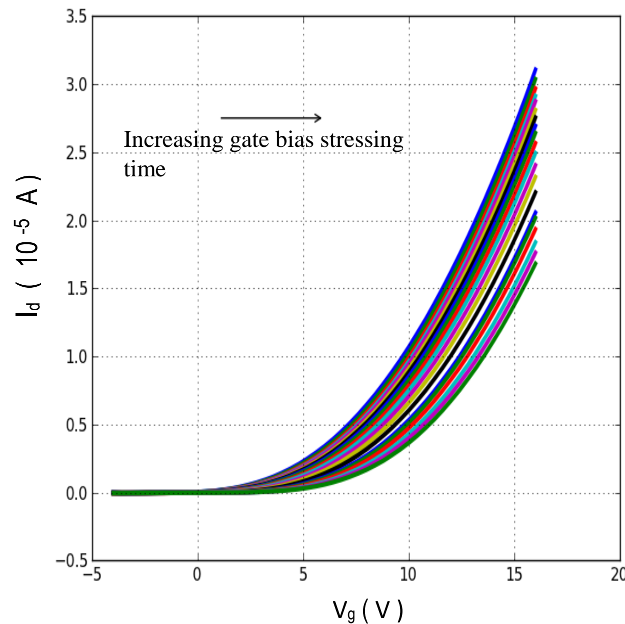


Figure 4.6: Transfer characteristic curves shift with stressing time of W = 1000µm and L = 30 µm. The drain bias was 10V and the stressing gate bias was mentioned at 10V with stressing times of 0, 15, 30, 90, 150, 240, 360, 540, 780, 1080, 1500, 2100, 2820, 3720, 4920, 6720, 7200, 8400, 1080, and 13200 seconds.

It is clear that the transfer curves for different stressing time reveal shifts toward larger threshold voltages. The positive shifts of threshold voltage with stress time could be due to electron trapping at the channel/dielectric interface or injected into the dielectric or creation of defect states at or close to the channel /insulator interface [28, 126, 132, 150]. Trapped electrons at the interface between active layer and oxide dielectric reduces the effective gate bias and consequently shifts the threshold voltage in the positive direction. The lower effective gate bias results in smaller drain current flow through device channel, therefore, larger gate bias is needed to switch on the device and reach saturation.

The shift of threshold voltage is given by:

$$\Delta V_{th} = V_{th}(t) - V_{th}(t = 0) \quad (4.3)$$

where $V_{th}(t)$ and $V_{th}(t = 0)$ are the threshold voltage at time t and at the start of bias stressing respectively.

Applying negative gate bias stress to the device resulted in no shift of threshold voltage with negative bias. This results is attributed to full depletion of the transistor channel with negative gate bias so that there is no mobile charge available for charge trapping.

It is well known for a Si TFT that there are two effects causing instability: defect creation in the channel and charge trapping in the dielectric material and at the channel/insulator interface [28]. In our case the bias stress dose not permanently deteriorate the device performance. This suggests that no additional defects appears during the stress. This also indicates that the formation of additional electron trapping states in the interface of active layer and dielectric layers by gate bias stressing is negligible and that the shifts of threshold voltage mainly results from the trapping of negative carriers at the interface or between the bulk dielectric layers. This behaviour is similar to that observed by Lei *et al.* [146] on a-In-Ga-Zn-O metal oxide transistor.

The charge trapping at the channel / dielectric interface and injection of charge onto the dielectric have the same impact on resultant electrical properties but with one exception. The major difference between the two is the amount of energy needed to remove the injected charge should be much higher than the energy required to release trapped charge at interface [171, 172]. If the charge injection is the dominant mechanism then some form of bias/ thermal annealing is required to recover the device back to its virgin state [173]. Also, thermal annealing is necessary to remove any defects created during bias stress[174]. Our device dielectric material was thermally grown silicon dioxide which has a low density of bulk trap states and the fact that the device return to its initial state quickly without annealing suggest that charge trapping is the major cause of In_2O_3 device instability and hence the charge injection is less probable.

The process of charge trapping starts with the quick shifts of threshold voltage which appeared shortly after applying stress, suggesting that the charge is trapped instantaneously at readily available states at the interface or in channel region.

On the other hand, the trapped states are limited in number so their effect on ΔV_{th} should decrease with time and tends to saturation as it is clear in Figure 4.7.

The threshold voltage shift observed for indium oxide thin film transistor can be well described with the stretched exponential equation [146, 147].

$$\Delta V_{th} = [V_{th}(\infty) - V_{th}(t = 0)][1 - \exp[-(t/\tau)^{\beta}] \quad (4.4)$$

where V_{th} (∞) is the threshold voltage when equilibrium has been reached at t→∞ . Therefore we can rewrite the above equation as:

$$\Delta V_{th} = \Delta V_{tho} \; [1 - \exp[-(t/\tau)^{\beta}] \quad (4.5)$$

where β is the stretched function exponent with value ($0 < \beta < 1$) and τ represents the characteristic trapping time (time constant) which correlates with the average effective energy barrier. Equation 4.4 is an empirical function introduced by Rudolf Kohlrausch in 1854 to describe the time dependent discharge of a capacitor and sometimes known as the Kohlrauch function. The exponent β describes the degree of deviation from an exponential function. When β is equal or close to 1, it indicates a narrow distribution of time constants, the limiting value of 1 corresponding to a single time constant. However, smaller values of $\beta < 1$ imply a broader distribution of time constants [175].

Figure 4.7 represents the fitting of threshold voltage shift with stressing time according to Equation 4.4 in both linear and logarithmic scale.

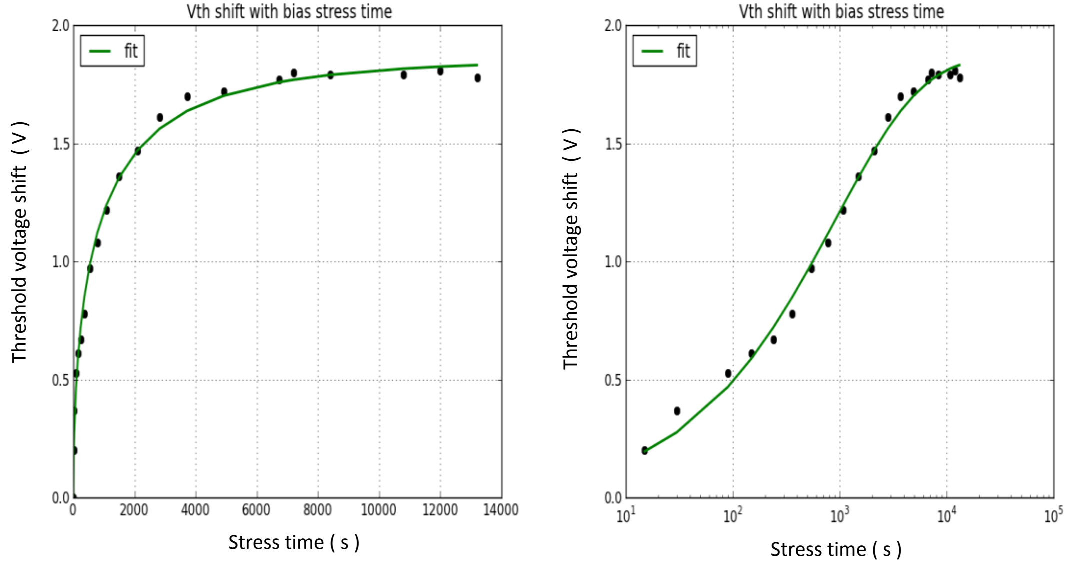


Figure 4.7: Time dependence of threshed voltage shift under the applied gate bias stress 10 V in linear scale (left) and logarithmic scale (right). The extracted fitting parameters are ΔV_{tho} =1.9±0.1 V, β = 0.53± 0.14, and τ = (3.64 ±0.23) * 10^4 s.

The experimental data of the threshold voltage shift with stressing time agree well with the stretched exponential function presented in Eq.4-4 and the extracted fitting parameters from curve fitting are ΔV_{tho} =1.9±0.1 V, β = 0.53±0.14, and τ = (3.64±0.23) *10^4 s.

Based on the gradual channel model and the stretched exponential function of ΔV_{th}, the drain current can be written as [148].

$$\frac{I_d\,(t)}{I_d\,(t=0)} = \exp[-(t/\tau)^{\beta}\,] \qquad (4.6)$$

The measured drain current under varied stressing time also agreed with Equation 4.6 and the obtained fitting parameters β = 0.52±0.11, τ = (3.6±0.16) * 10^4 s are consistent with the previous calculation.

Figure 4.8 below shows the time dependent drain current under positive stress.

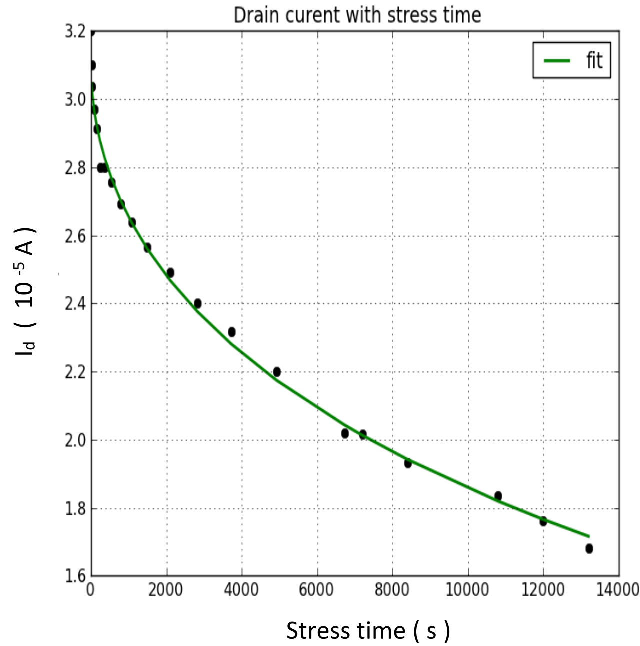


Figure 4.8: Drain current decrease with stress time according to equation 4.4. The extracted fitting parameters are I_{do} = 3.08 *10^{-5} A,   = 0.52±0.11, and τ =(3.6±0.16) * 10^4 s.

Our study results reveal that the charges gradually trapped likely in the channel/dielectric or dielectric bulk leading to the observed threshold voltage shifts over time. The actual nature of charge trapping is not clear but our experimental data indicates that:

The trapping time constant is widely distributed and the dynamics of bias stress become increasingly slower with time. This means at the beginning of stress the traps of small time constant filled firstly. As the stressing time increases, traps with increasingly higher time constant get filled. Accordingly a mechanism of wide distribution of time constant should provide either a distribution of energy barriers between majority carriers and traps or both. So, the charge trapping is a progressive process which starts quickly at the beginning of the bias stress then slows down as the stress duration increases corresponding to gradual filling of trap states.

The most significant effects of bias stress is threshold voltage shift and the amount of shift decrease with time till we see no any noticeable effect of shift suggesting saturation process which is evident in Figure 4.8. Similar behaviours is observed [28, 132, 145, 154, 176] in the metal oxide, organic and amorphous silicon TFT.

The rate at which V_{th} shifts during gate bias stress; depends on the applied gate and drain-source voltages. A greater gate-source voltage leads to a faster threshold voltage shift [145], likely because a bigger gate voltage induces a larger density of charge carriers in the channel, which at a constant trapping rate increases the number of carriers trapped per time and area . On the other hand, a larger drain-source voltage leads to slower bias stress-induced threshold voltage shift. This monitoring has been attributed to the fact that a larger drain- source voltage opposes the electrical field produced by the gate voltage near the drain contact, thereby reducing the density of carriers in the channel close to the drain terminal and thus decreasing the number of carriers trapped per time and area.

In contrast to the defect creation which is irreversible and roughly stable at room temperature, the charge trapping process is reversible even at room temperature and the threshold voltage shifts with associated decrease in drain current will recover after stress removing [145, 177]. This means the charge release (detrapping) from trapped states back to the channel layer is energetically favourable when the gate bias is removed.

In some electronic applications such as active matrix displays, the TFT switched on only for limited time or temporarily, so the produced shift in threshold voltage relaxes in the off state. Therefore, recovery is as important as stress and the device should return to its original state after stress release. The recovery of ΔV_{th} after switching off the bias stress was studied in the above mentioned devices and we found that the threshold voltage shift is reversible and recovered gradually.

Figure 4.9 illustrates the backward shift of transfer characteristic after stress release.

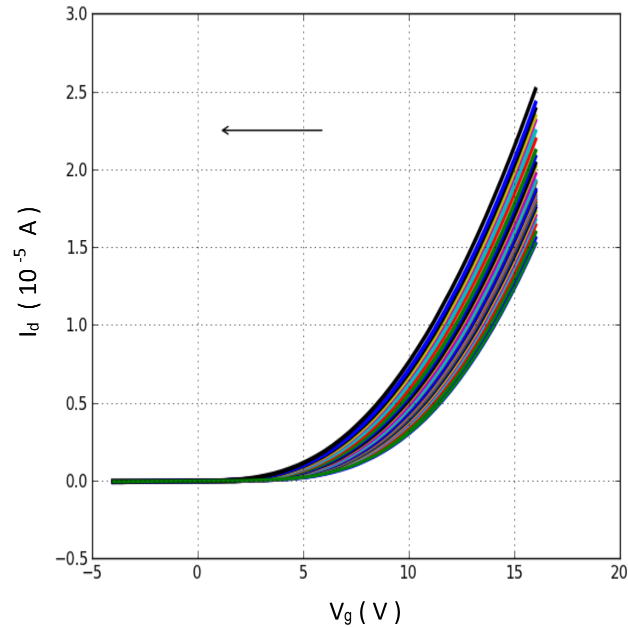


Figure 4.9: Transfer characteristics back shift after stress release of device *W*= 1000µm and *L*=30µm. The arrow shows the direction of shift.

The recovery of threshold voltage over time is shown in Figure 4.10.

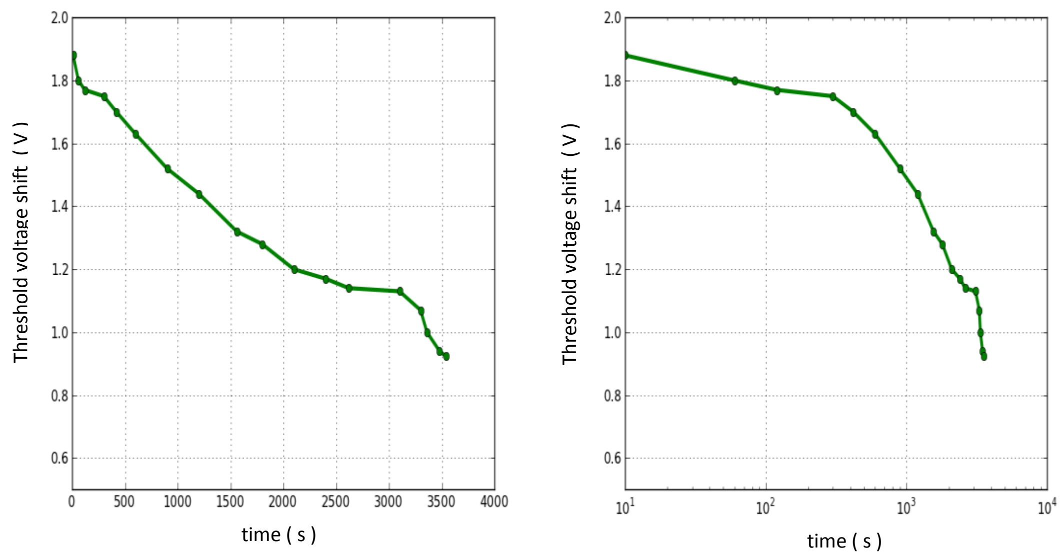


Figure 4.10: Threshold voltage recovery after switching off the gate bias. The data is plotted in both linear and logarithmic scale. The time close to zero is refer to the switch off the gate bias.

Hence, the process of charge trapping is reversible and the charge release (detrapping) from the gate dielectric back into the TFT channel layer, is energetically favourable - when the gate bias switched off.

The trapped charges occupy energy levels close to the dielectric Fermi level which is below the Fermi level of channel layer. Once the gate bias is removed, the energy of trapped charges lies above the Fermi level in the channel layer. This energy difference favours detrapping and back tunnelling of charges into the channel layer.

Generally, similar behaviours was found in other indium oxide TFT devices during bias stress and after stress relaxation. Finally, we expect that the reduction or elimination of ambient interaction with the device by encapsulation would reduce instability of a bottom gate top contact TFT.

4.8 Surface potential images about charge trapping (spatial distribution of trapped charges)

In this section we are studying charge trapping by monitoring EFM-SKPM (Scanning Kelvin probe mode) images before and after applying a gate voltage. We show that EFM also can be used to image charge trapping spatial distribution. The detected trapped charge can affect device performance and its life time. For this purpose, we performed a set of EFM measurements with the Vecco Multimode SPM. The scanning stage, including the sample, was maintained at ambient temperature in the dark under flowing nitrogen using a metallic hood. During this experiment the source and drain electrodes are grounded whereas the gate terminal connected to the power supply. EFM images captured (using Pt/Ir conducting tip of the resonance frequency 73.4Hz) in the channel between the source-drain before applying gate bias. Then a constant gate voltage +5V subjected to the gate terminal for fixed time 1:30 hour.

It has been suggested that greater mobility permits charges to travel into traps quicker [178] and slow charge release enable EFM to follow it easily[179]. We selected a device of dimension (W = 1500 μm, L = 40 μm) from an earlier batch of poorer quality films to illustrate the use of EFM to detect charge trapping. The output and transfer characteristics of this device is shown in Figure 4.11 below.

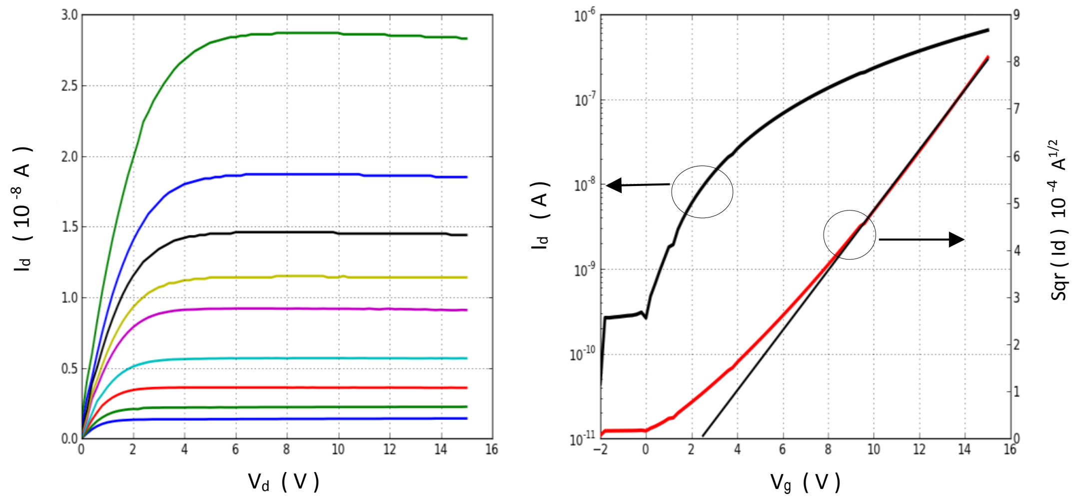


Figure 4.11: The output curves of W=1500 µm and L= 40 µm at gate bias V_g = 1, 1.25, 1.5, 2, 3, 3.5, 4, 5, 7 V and its transfer characteristic at drain voltage V_d =20 V. The measured device saturation mobility is μ_{sat} = 0.023 cm^2 V^{-1}s^{-1}, V_{th} = 2.5 V, V_{on} = 0.1 V and I_{on}/I_{off} = 10^4.

The device is working in an enhancement mode with V_{th} = 2.5 V so we expect the presence of mobile charge at interface layer at In_2O_3/ SiO_2 interface for that gate bias.

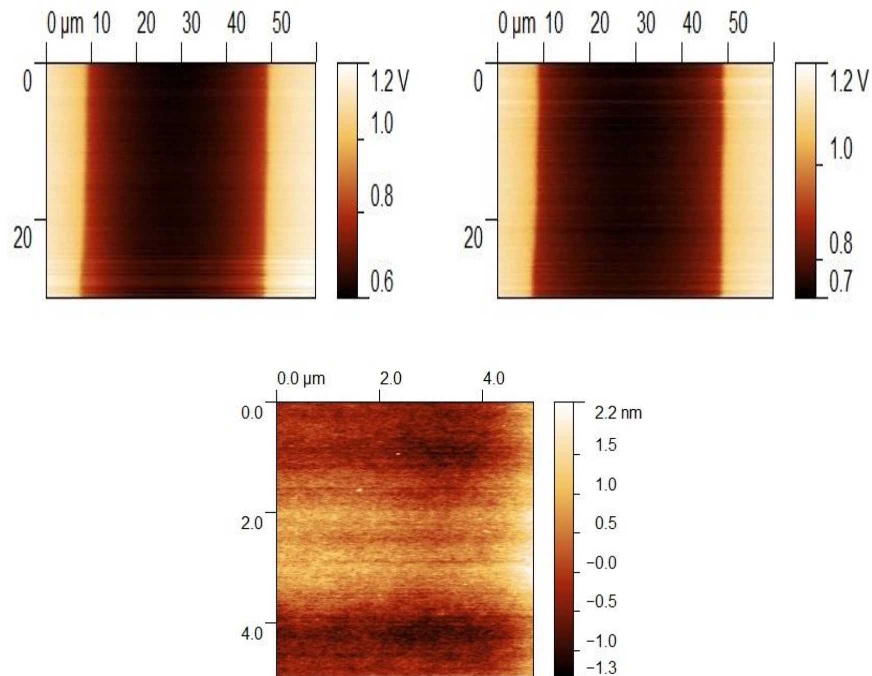


Figure 4.12: Surface potential images before (top right) and after (top left) applying +5 V gate bias with source and drain electrodes grounded. The bottom is 5µmx5µm AFM image shows the surface morphology between source and drain. The roughness (r.m.s) of the AFM image was 0.56±0.12 nm. The film is smooth and contain no any voids or discontinuity between two the electrodes.

Figure 4.12 shows the EFM images before and after gate bias is applied, together with an AFM image of the film topography in the channel between the two electrodes.

After applying gate bias, we might expect the appearance of dimpled patches corresponding to the location of trapped charge. However, this was not observed: we see no significant difference between the two images of Figure 4.12 (left and right). Since the source and drain terminals are grounded and the mobile charges accumulate in the channel at the interface with the gate dielectric when the gate voltage is applied, any traps are electrically screened [180]. Since there is no lateral electric field between source and drain electrodes, there is no pinch off or space charge region either.

In contrast, EFM image showed a dramatic changes after switching off the gate bias. The mobile charges, accumulated electrons disperse to the electrodes and into the bulk In_2O_3 leaving only the trapped charges. In other words, when the gate bias is switched to zero, the transistor will be in depletion and there is no longer a conducting layer present at In_2O_3/SiO_2 interface to mask the charge trapping effect. The trapped charges remain for sufficient time which is enough for EFM imaging and monitoring. Accordingly, we monitored the images as a function of scanning time till the device is recovered. To do this and in order to follow and map the potential distribution as a function of time after gate bias removal the slow axis scan of EFM was disabled so the potential is only a function of time. Figure 4.13 shows the change of EFM with time starting from t=0 at the bottom of image (time where $V_g = 0$).

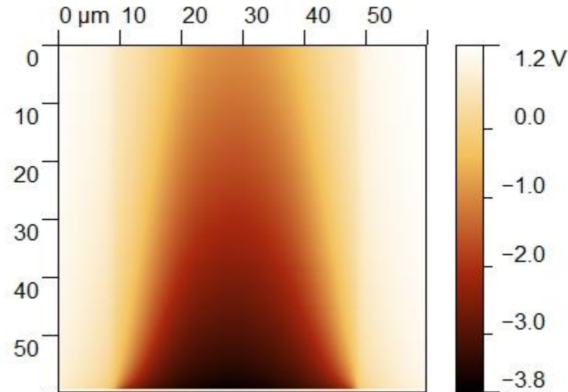


Figure 4-13: Surface potential image after setting gate bias to zero. The bottom of the figure where the dark image cover the region between source and drain is represent the initial time t = 0 where the gate voltage switched to zero. The scanning is from bottom to the top.

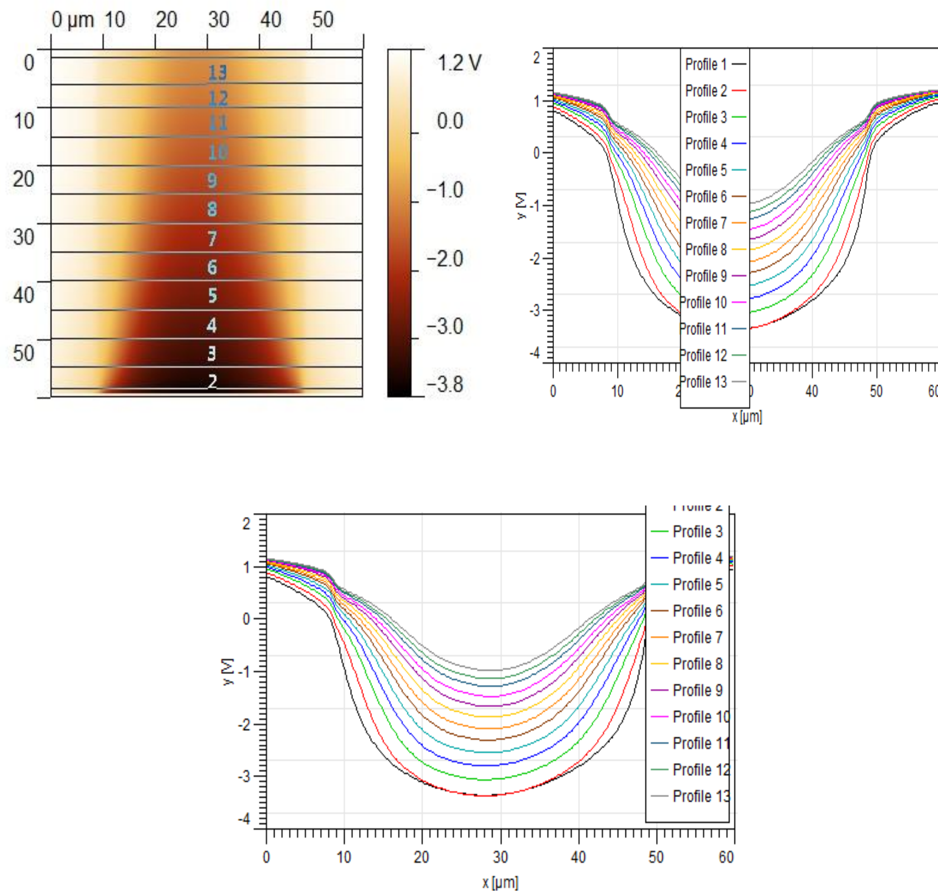


Figure 4.14: Surface potential profiles variation as a function of scanning time when the slow scan axis was disabled. The EFM image (left) is measured from bottom to the top with profiles equally spaced in time. The potential profiles (right and bottom) corresponding to the numbered lines in EFM image, drawn using Gwyddion software package.

Figure 4.14 illustrate the variation of profiles with time. The scanning was from bottom of image (at $t = 0$) to the maximum or highest point (total scanning time is 8.25 min).

The trend of profiles with time is consistent with gradual discharge to the electrodes. Furthermore, it is important to mention here that the time between the profiles is same (image equally divided) but the rate of change of the measured potential decreases with time. Figure 4.15 illustrates the second scan, from top to bottom following continuously from the scan in Figure 4.15, with corresponding profiles of cross sectional line drawn in EFM image. The EFM images show that the device will recover gradually and has a trend to come back to its original state before stress was applied.

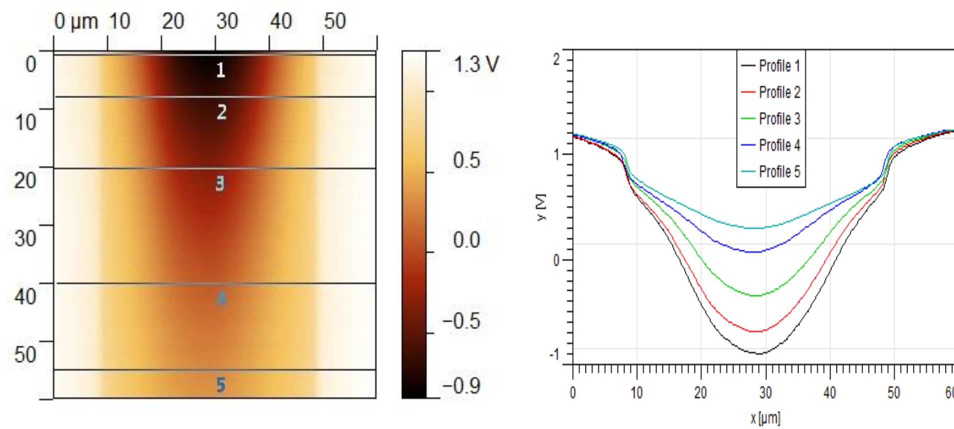


Figure 4.15: Captured surface potential image and line profiles according to cross sectional lines, continuing from Figure 4.14. The figure shows device recovery process with time for the second scan from top to bottom.

This results is consistent with *I-V* measurements of bias stress of this device where we noticed it return to its virgin state after stress release gradually.

However, we studied the charge trapping by subjecting another device (*W* = 1000 µm, *L* = 20 µm)[also an earlier batch] to gate bias stress of +8V for 1 hour while the device was kept in the dark. Figure 4.16 shows AFM images across drain and source in addition to EFM images before and after applying gate bias.

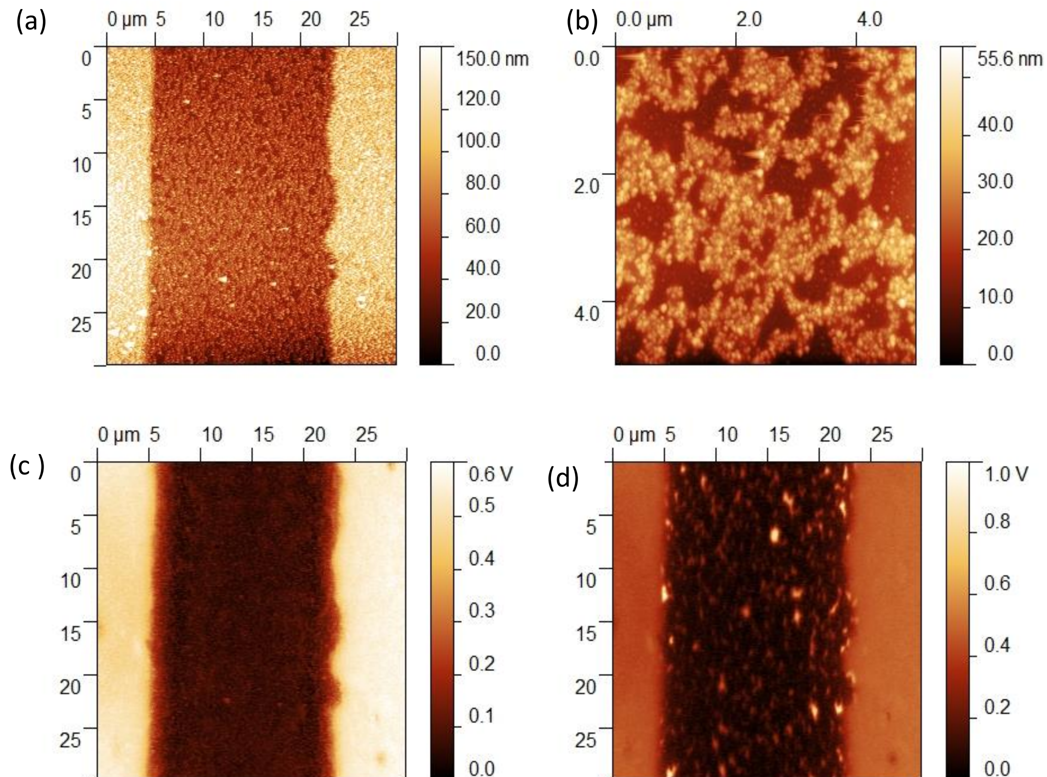


Figure 4.16: a) AFM height image across two electrodes b), 5µmx5µm AFM image captured between two electrodes c), Surface potential image before applying gate bias d), SP after applying +8V gate bias.

It is obvious from AFM images that the film between electrodes contains many voids and discontinuity in addition to large grains which accumulate as clusters. The film roughness (r.m.s) value of 5µm x 5µm is 7.4±0.83 nm which is about 13 times greater than previous case illustrated in Figure 4.12. The origin of this feature of morphology is not known and we don't know the actual reasons of such device topography.

Comparing Figure 4.16 c,d, there is a clear difference between images before and after gate bias subjection which directly correlates with charge trapping process. In this sample, charge trapping does not occur uniformly throughout the film, but there are

well-defined sites at which charges are trapped preferentially. We see clearly that the bright spots in the surface potential image Fig.4-16d coincide with troughs or voids in topography image Fig.4-16a which implies that the trapped charges preferentially occupy the disordered position such as small voids or grain boundary. This appeared as a bright dots and corresponding to the higher density of trapped charges.

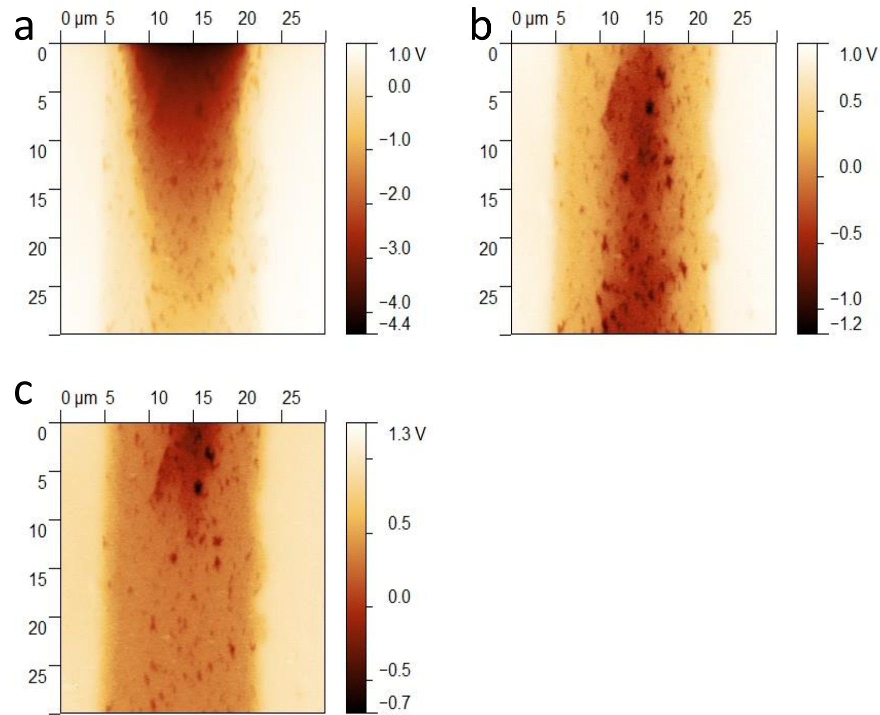


Figure 4-17: Recovery of the device after switching the gate bias to zero. a) Scanning from top to bottom, b) scanning from bottom toward top, c) scanning from top toward bottom. The time taken per image is about 8.1min.

Figure 4.17 depicts the device recovery after turning off the gate bias. Switching off the gate bias initiates device depletion and release of trapped charges. In this case the bright dots which correlated to the voids or small troughs positions in stress case become darker than other parts of film in recovery or after stress release (compare Fig.4-16d and Fig.4-17). Finally, after continuous monitoring of the surface potential images the device return to its original state (before stress) and no difference recorded between them.

Part 3:

4.9 Surface potential study of indium oxide TFT

The main aim of the experiments presented in this section was to investigate the potential profile in operational In_2O_3 TFT. They were performed on top contact bottom gate thin film transistor with spin coated thin film of indium oxide as active layer as described previously. All experiments were performed under a flushing N_2 environment in our dark room using the Bruker Nanoscope IIIa SPM. In our study for surface potential, an AFM is operated with Ir/Pt conductive probes of typical resonance frequency 70-79 kHz and spring constant around 5 Nm^{-1}. SKPM technique was used for obtaining surface potential profiles and 2D images. SKPM is a dual pass technique; during the first pass sample topography is obtained by the intermittent contact AFM mode. After completing a line, the tip is raised 20- 30nm relative to the topography and the same line is scanned again, and the surface potential data is collected during the second pass. The first sweep data measurements depends on the mechanical oscillations of cantilever. While the second pass is performed by turning off the mechanical oscillation and applying a mixed potential $V_{dc} + V_{ac}$ to the cantilever. A lock-in amplifier is used to measure the deflection of the cantilever resulting from the electrostatic force and extracted the component of oscillation at the driving frequency ω. The feedback loop minimizes the electrostatic deflection by adjusting the applied dc potential to the tip and operates to maintain the second term of Equation 4.7 at zero. As the AFM scans and generates a topographical image, a measure of the nulling dc potential applied to the tip is simultaneously used to generate a map of the surface potential of the sample.

During a scan, the electrostatic force F between the sample surface and the tip is expressed as:

$$F = \left(\left(V_{dc} - \frac{V_{CPD}}{q}\right)^2 + \frac{1}{2}V_{ac}{}^2\right)\frac{\partial c}{\partial z} + \frac{\partial c}{\partial z}\left(V_{dc} - \frac{V_{CPD}}{q}\right)V_{ac}\sin(\omega t) + \frac{1}{4}\frac{\partial c}{\partial z}V_{ac}^2\cos(2\omega t)$$

… (4.7)

In other words, the voltage applied to the conducting tip is regulated by a feedback loop such that the long range electrostatic force is minimized or nulled. This nulling dc voltage measures the contact potential difference V_{CPD} between the tip and sample which is the difference in work functions of tip and sample.

The V_{CPD} is very sensitive to the sample surface such that in atmosphere the oxidation of sample and tip, contamination, and surface moisture can affect the measured V_{CPD}. Therefore, all our measurements achieved in dark room and under dry N_2 slow flush with careful handling and safe keeping of sample to avoid or minimize such contaminations. Figure 4.18 shows the schematic of a typical TFT and surface potential (SP) experiment setup. A Silicon substrate served as the gate with a 100 nm thermally grown oxide as the dielectric, Al source and drain were patterned by shadow mask.

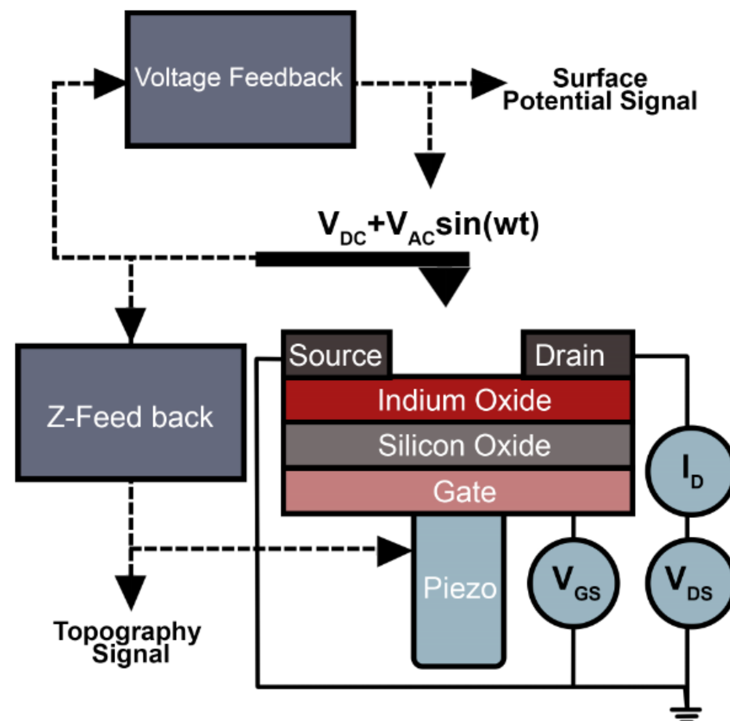


Figure 4.18: Experimental setup used for indium oxide TFT surface potential measurements.

In the current study the source was grounded while the gate and drain electrodes were biased. Scanning of the probe for each line starts above the source electrode, across the channel region and ends above drain electrode.

Figure 4.19 depicts the topographic image and corresponding line profile of single spin coating device W1000L30S. The central smooth area is the channel region and the area to the left and right of yellow colours are the Al contact regions.

Hence, the channel is clearly seen in the topographic image and position (x) in profile presents the distance between the source and drain. The 5 µm x 5 µm captured image between electrodes revealed surface roughness of order of 0.56 ± 0.06 nm as indicated in Figure 4.2. Based on the topographic image and extracted line profile analysis it is clear that the homogeneous and flat indium oxide thin film completely covers the gap between the source and drain. The film shows no voids or discontinuity that disturb smooth carrier flow between well-defined electrodes edge.

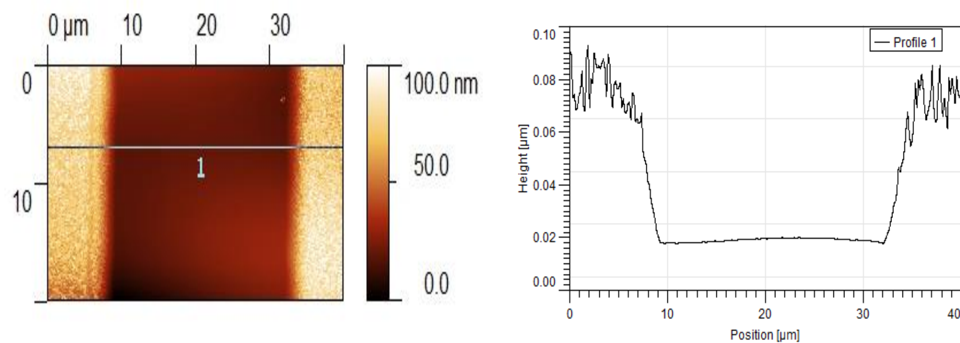


Figure 4.19: AFM topographic image of W1000L30S device (left) and the corresponding line profile (right) along line 1 across contacts and the channel. The channel between electrodes is clearly seen and contain no voids or discontinuity.

Figure 4.20 shows the 2D SP images consecutively taken while the drain electrode was biased at 0, 1, 2, 4, and 6 V respectively. The surface potential distributions across the channel and at the contact edges at zero drain voltage seem very uniform. This uniformity infers that the active material between electrodes is thin enough to have the same conductivity all over the channel. Applying bias to the drain contact, the change in potential distribution near the electrode is observed and two distinct regions in the conducting channel was noticed. The dark brown area from source to the indicated vertical red line and the lighter coloured region aside drain electrode which fades as the drain bias increase.

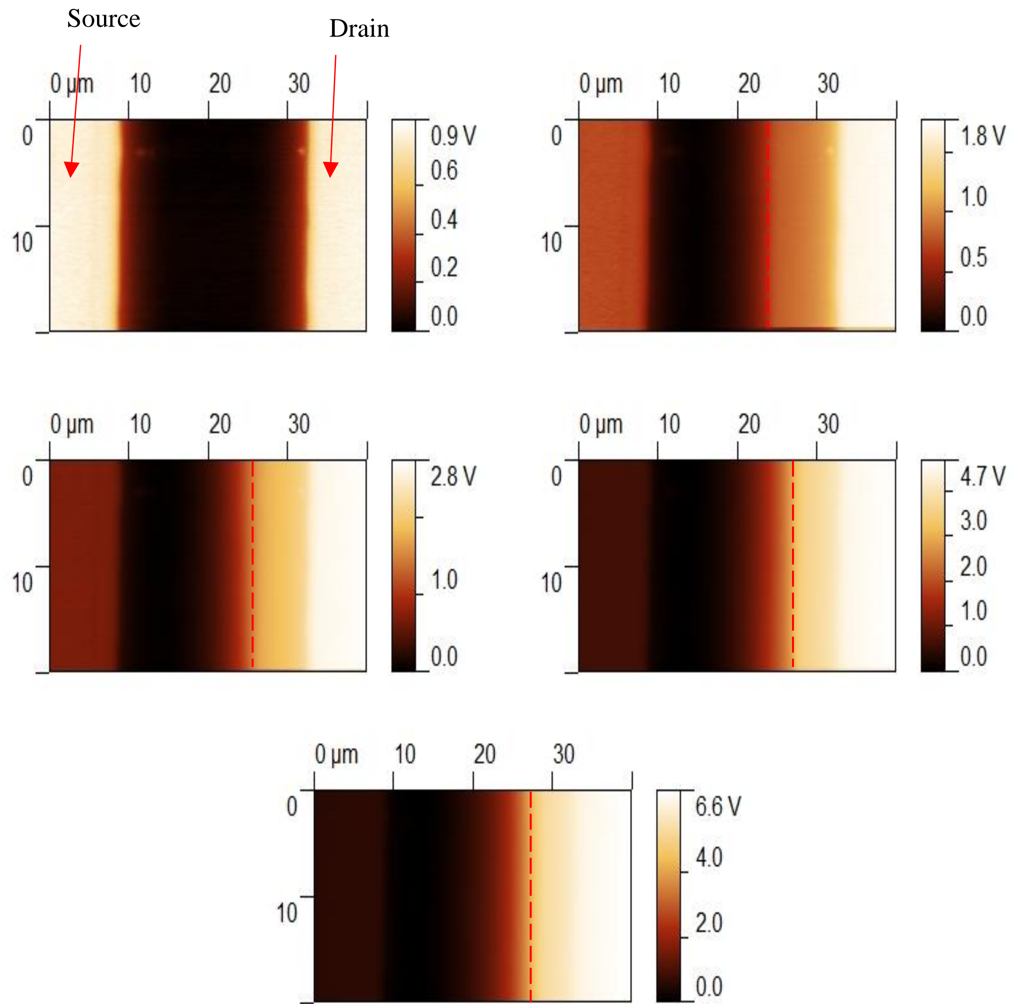


Figure 4.20: 2D surface potential images of L30W1000S device at 0, 1, 2, 4, and 6 V drain bias.

The corresponding line profiles at indicated and some different drain biases at room temperature 25 ^{o}C and under N_2 flush are shown in Figure 4.21. The variation of profiles between two electrodes were investigated and we found smooth and uninterrupted profiles for all drain biases used.

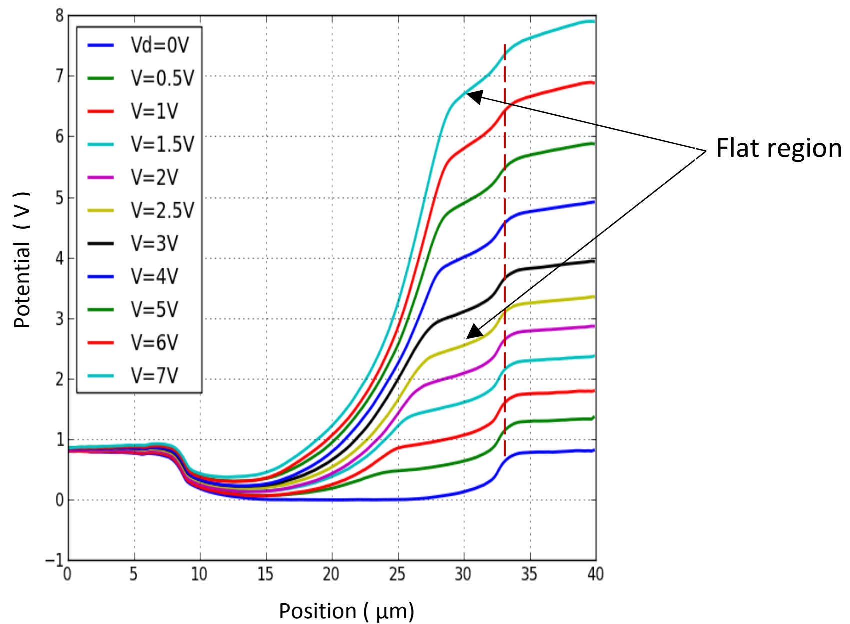


Figure 4.21: The W1000L30S device potential profiles acquired for different drain biases with grounding the source and gate terminals. The drain electrode edge is marked as a dashed red line.

In surface potential measurements the recorded profiles are a combination of the local potential in the accumulation layer and work function difference between the tip and sample. The latter can be deduced from a reference potential profile measured at zero drain bias. In Figure 4.21, a relatively flat region is observed close to the drain electrode, and a small potential drop at semiconductor /metal contacts. This drop is caused by the work function difference and the contact resistance. The 2D images and line profiles show that the extent of this flat region is a function of drain bias, it becomes narrow as the drain voltage increase. For instance, a drain bias 1 V gives a flat region that extends to around 24.6 μm in Figure 4.21, whereas, this edge shifts to 28.9 μm at 7 V drain bias. The apparent flatness in the profiles cannot relate to the pinch off region as the pinch off point under saturation conditions should move further away from the drain electrodes as the bias is increased. The cause of this flat region in the potential profiles will be discussed later and correlates to contact diffusion into the device channel.

Applying 5 V gate bias, the above profiles shows changes that reflect directly the effect of gate bias due to gate induced charges in the channel.

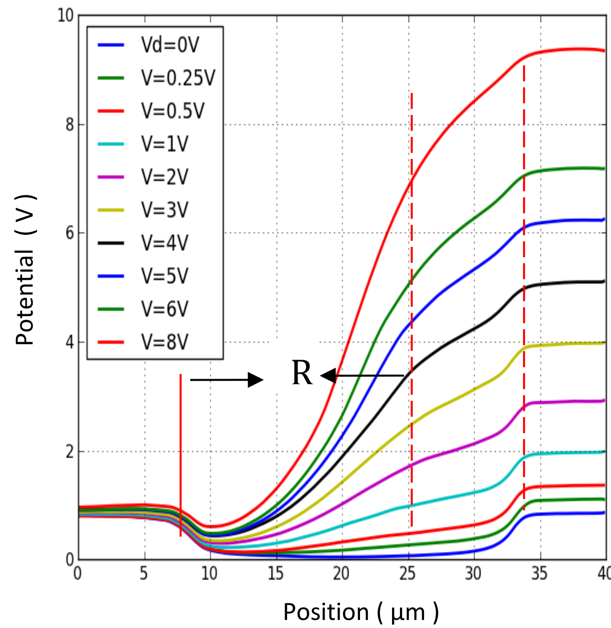


Figure 4.22: The W1000L30S device potential profiles at fixed 5 V gate voltage and varied drain biases.

Comparing the potential profiles in Figure 4.23 with those in figure 4.22 helps clarify the effect of the positive 5 V gate bias. We note:

1. The potential drop at the electrode edges due to the work function difference and contact resistance is similar.
2. There is a flatter region close to the drain electrode for both gate voltages, though the edge of this region is more rounded and less clear for $V_g = 5$ V.
3. For low drain bias, $V_d < V_g$, the profiles are approximately linear between the source electrode and the onset of the flattened region.
4. At high drain bias, $V_d > V_g$, the gradient of the profiles increase with distance from the source electrode until the onset of the flattened region

The shape of the potential profile can be qualitatively related to the local carrier concentration. Since the current flowing past each point in the transistor is constant, then the local potential drop scales approximately with the local resistivity. Since we can write $J = \sigma E$ (where J, σ, E are current density, conductivity, and electric field respectively), ignoring local changes in the cross- section of the conducting channel, we can see that the local conductivity σ is roughly inversely proportional to the local electric field E, which represents the gradient of the potential profile.

Hence, steep regions of the profile indicate low carrier density and flatter regions indicate high carrier density. (Alternatively, one can view the channel as a potential divider in which the potential drop across each component scales with its resistance.)

For low drain bias, $V_d < V_g$, the whole channel contains mobile carriers accumulated at the gate dielectric. Hence there are no high resistance regions where the electric field is large. For high drain bias, $V_d > V_g$, carriers accumulate in the channel as far as the region where $V_d \approx (V_g - V_{th})$ at which pinch-off occurs. Between this point and the drain electrode, no carriers accumulate in the channel, leaving it depleted. In this region, the electric field is expected to be high, resulting in a steep gradient in the voltage profiles. It is this depletion that leads to the saturated current observed in output characteristics (Figure 4.4B).

Up to this point, the interpretation of the potential profiles is reasonably straightforward and corresponds with our understanding based on the gradual channel model. However, this model does not explain the flattened regions close to the drain electrode. The EFM results strongly indicate that this region has a high carrier density that one would not expect based on the above discussion. It is known that aluminium tends to diffuse from electrodes into the channel. We interpret this flattened region as being caused by Al diffusing from the drain electrode. It should be noted that interpretation of potential profiles in depleted regions can be complicated by the lack of mobile carriers to screen the applied gate potential[180]. However, comparison of the potential profiles as a function of gate potential indicate that this is not a significant effect in the measurements reported here.

The region of the potential profiles become clear when we plot the first derivative of potential, dV/dx across the channel and contacts. Note that the magnitude of dV/dx changes rapidly at Al diffusion position, its peak position indicating the edge of the diffusion region. This peak value also increase as the device enter to the saturation region. However, at the source/drain electrode edge there is less variation between scans. The shift in the apparent edge of the diffused Al region with applied drain voltage is less clear. It may reflect the sensitivity of the intrinsic carrier density to the local potential in this region.

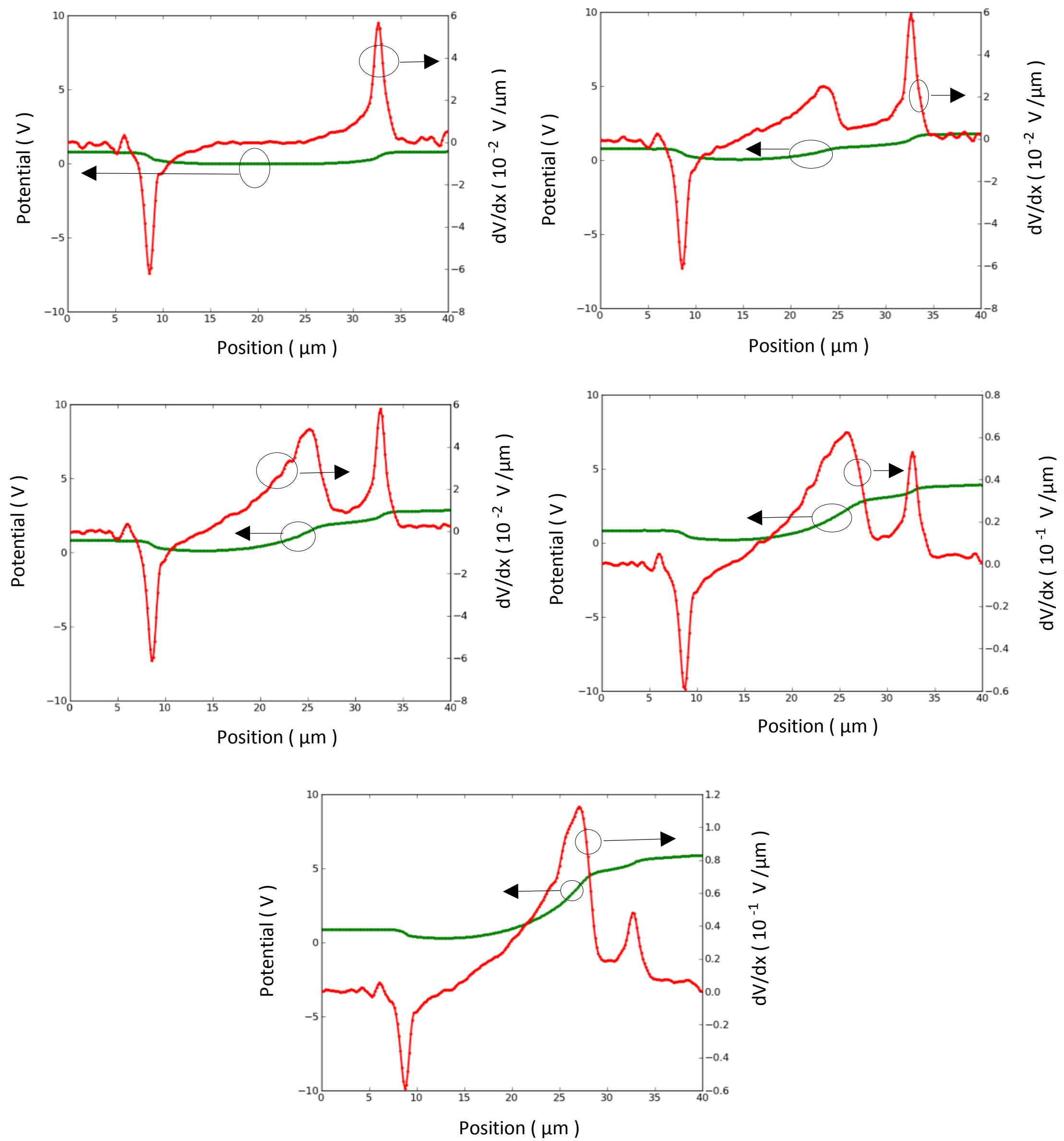


Figure 4.23: Change of first derivative of potential across the channel and specification of electrode and diffusion position. The green curves represents the potential and the red curve is the first derivative of potential. The plotted data corresponding to Figure 4.20 and Figure 4.21 for drain bias values 0, 1, 2, 4, and 6 V.

The profiles in Figure 4.24, 4.25 are two representative sets of figures taken for fixed drain bias but varied gate voltages for same W1000L30S device.

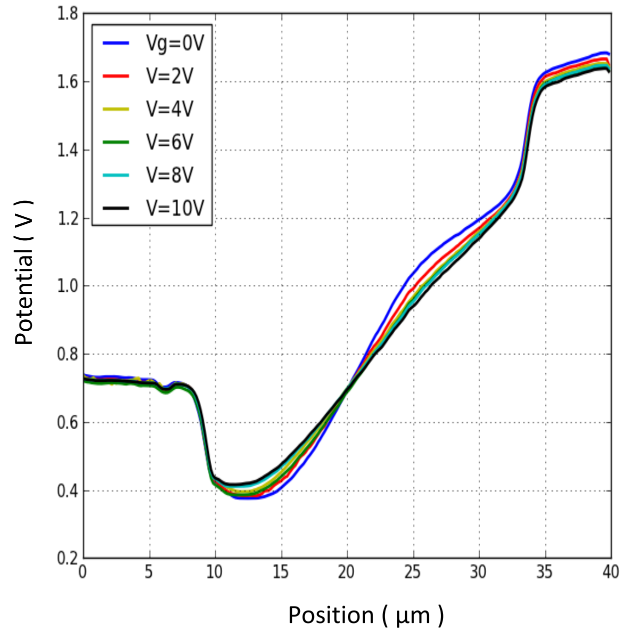


Figure 4.24: Potential profiles as a function of gate bias where V_d = 1 V (linear region) and gate bias changed from 0 to 10V step 2 V.

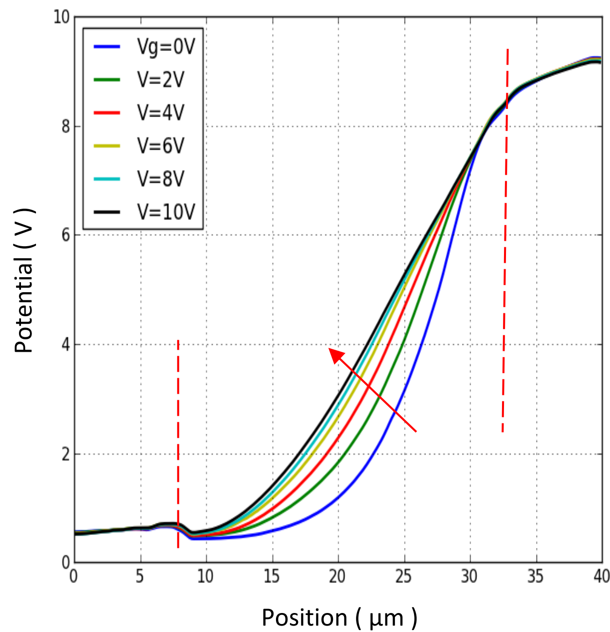


Figure 4.25: Potential profiles inside the operating device where drain voltage kept constant at high voltage 9 V and gate bias changed with step 2 V from 0 to 10 V.

The potential profiles of the above figures confirm the clean transistor operation for two distinct drain voltages. There is a progressive transition as gate bias V_g is increased from 0 -to 10V for $V_d = 9$ V from nonlinear profile for $V_d > V_g$ indicative of the saturation regime, toward a linear profile for $V_d < V_g$ in the linear regime. A weak gate bias dependence properties for $V_d = 1$ V is clear in Figure 4.24 where the device is working in the linear region (Figure 4.4B) throughout. Even though the current between the electrodes changes strongly due to increasing accumulation of carriers, the potential distribution only varies weakly.

Since the relative effect of contact diffusion decrease as the channel length is increased [181] so the flat region in the potential profiles will be less apparent for larger length device as in Figure 4.26 below.

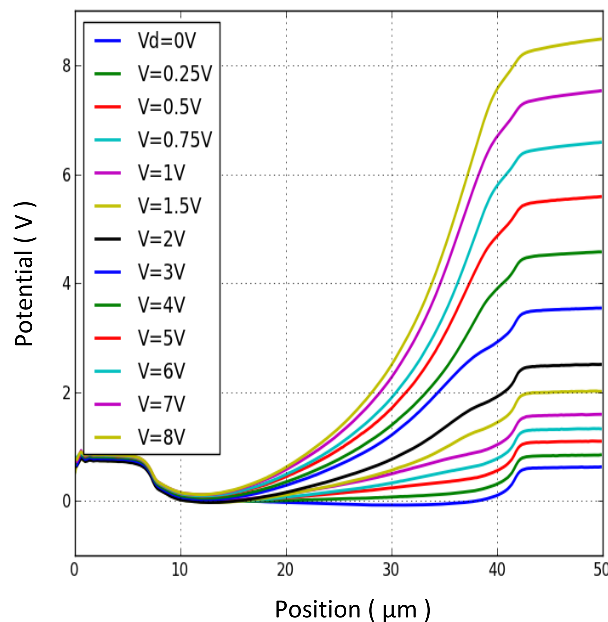


Figure 4.26: Surface potential line profiles across W200L40D operating device at fixed gate bias +5 V and varied drain voltages marked on the figure. The broadness at the vicinity of drain is roughly less clear. The device operation is clear and the change of profiles from linear behaviour to super-linear which corresponds to linear and saturation regime of operation is apparent.

Moreover, the effect of gate bias is very clear in this device (Figure 4.27) and the actual quick trend of profiles from super-linear to linear by increasing the gate bias is obvious and presents the increase of induced charge in the channel.

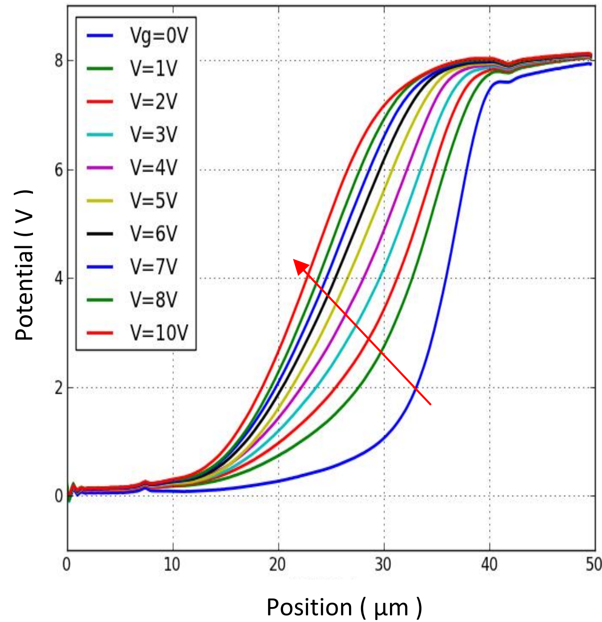


Figure 4.27: Gate voltage dependence potential profiles inside operating L40W200D device. The drain bias was constant +8 V during the experiment and gate voltage changed from 1 to 10V step 1 V. The profiles obtained after subtraction the reference profile at $V_d = 0$ from all $V_d \neq 0$.

The effect of the contact element diffusion is more marked as the channel length *L* decreases [181] . Effects of contact diffusion also reported on the other metal oxide based devices [129, 130, 140].

Part 4

4.10 Mapping of Aluminium diffusion in In_2O_3 Thin film transistor and modelling potential profiles.

In this section we complement the experimental data shown in the previous section with simulation results for detection of Al contact diffusion into the indium oxide channel. We also report on a simple, alternative approach to non-destructive detection of contact diffusion in thin film transistor. Aluminium is desirable useful metal for contacting metal oxide semiconductor because of its electrical properties, low resistivity, good adhesion, and cost [182, 183]. However, Al can diffuse into semiconductors and is, easily oxidised when exposed to air because it's high oxygen affinity. This is the major limitation that can affect the contact reliability.

The Silvaco Atlas software package [184]was used, shown to reliably model working device [185]. When the problem is simulated in Atlas, the physical structure and mesh are first defined, then the physical models and the bias conditions are specified. The Atlas models are defined using commands and can run in the interactive run-time environment DeckBuild. Simulations of semiconductor devices are performed as a system of discrete non-linear problems that only approximate the behaviour of the continuous model. This approximation is performed using a discretisation method. Therefore, any solution for a device system will be presented as a non-linear algebraic problem which consists of discrete nonlinear partial differential equations which are solved on the structure mesh. It is important to have a refined mesh in the following regions: at the electrode and channel junctions with the high electric field, insulator layer through which tunnelling is allowed heterojunctions which form the channel in high electron mobility transistors.

The calculation of the discrete non-linear problem starts with the initial guess solution. The solution is then optimised iteratively. The iteration is finished when the convergence criteria are achieved: the corrections between iterations are smaller than the specified tolerance. In addition, a maximum number of iterations is often defined. If the convergence was not achieved in the maximum allowed number then a different numerical technique should be used or a structure mesh needs to be reconsidered. Corrections between the iterations are obtained by linearization of the problem. The

convergence criteria are important in determining whether a solution will be obtained, the accuracy of the approximation in the solution and the time needed to obtain the solution (efficiency). Accurate results and stable convergence are provided by the numerical methods of solving a non-linear algebraic problem and algorithm for the selection of the initial solution.

To model the transport across a metal-semiconductor interface the barrier height and potential distribution are calculated. The barrier lowering term due to the image force and dipole effects is included in the model. When calculating the thermionic emission current a surface thermal velocity is taken into account. The tunnelling current across the barrier is calculated using universal Schottky tunnelling model which is based on the calculation of the local tunnelling rates. Transport across ultrathin insulator layer is accounted for using a direct tunnelling model. The transmission probability of the tunnelling is calculated using the Gundlach formula and the Schenk model for the image force barrier lowering term in the insulator layer. The image force potential is calculated based on the Kleefstra and Herman formula. The model assumes a parabolic approximation for the barrier as this approximation is accurate for ultrathin insulator layers. This work was performed by our colleagues (Olga Kryvechenkova), Swansea University, in collaboration with us.

Surface potential data for working devices are complicated by continuously produced mobile charges that transport across the device. These also interact with electric field of a scanning probe [186]. Hence, the experimental data includes not only the intrinsic sample properties but also some artefacts due to the existence of the tip [186, 187]. The group at Swansea employed 2D drift-diffusion simulations of the In_2O_3 TFTs incorporating contact diffusion into the simulation.

In simulating the W1000L30S device, gate lengths of 25.62 μm single spin coating is used with 70 μm Al source and drain electrodes, 4 nm thick film n-type In_2O_3 conducting channel layer with a doping concentration of 8×10^{17} cm^{-3}, 100 nm SiO_2 insulator layer and 300 nm n-type Si substrate layer with a doping concentration of 10^{20} cm^{-3} followed by a bottom Al gate.

An n-type doping concentration of 2×10^{18} cm^{-3} was used to simulate the contact diffusion regions around drain and source electrodes. Other material parameters used in

the simulations are: In_2O_3 permittivity of 8.9 [188], bandgap of 4.0 eV [189], affinity of 4.45 eV [189], field-effect mobility of 0.27 $cm^2 V^{-1}s^{-1}$, and electron effective mass of $0.3m_0$, tip work function of 4.6 eV. The Schottky barrier height of 0.7 eV is extracted from the measured profiles for the source and drain electrodes. The simulated devices showed threshold voltage 1.8 V which is in good agreement with the value obtained from transfer characteristic curve.

Figure 4.28a depicts that the surface potential profile at $V_g = V_d = 0$ V is flat and homogeneous through the channel with the averaged line scan shown beneath in Figure 4-28b. The well-defined position of source and drain electrodes edges can be seen at around 8 µm and 33 µm respectively. Figure 4.28b also reveals that the potential profile across the channel at V_d =5 V flattens in the region from 28 µm up until the previously determined edge of the drain electrode at 33 µm both in the simulations and the experiment. The potential flattening suggests that this area has a higher dopant screening effect and a higher doping concentration after Al diffusion into the In_2O_3 channel. Simulations suggest that a doping concentration in the diffusion region increased from 8×10^{17} cm^{-3} to 2×10^{18} cm^{-3}. The edge of the diffusion region was estimated at 28.0 µm where the gradient of the surface lateral electric field Fig.4-28c, calculated as a second derivative of the potential, has a local extremum. Analogously, using the data in Fig.4-28b the electrodes edges at 7.7 µm and 33.3 µm where detected where the absolute change in the electric field has a local extremum. Both profiles at $V_d = 0$ V and $V_d = 5$ V are in good agreement. It should be noted that the diffusion region edge can be specified only from the potential profiles of the biased device. It would not be possible to determine the diffusion region edge using potential profile for a grounded TFT ($V_g = V_d = 0$ V) in Fig.4-28b because the surface potential change will only depend on the intrinsic material parameters, In_2O_3 affinity of the channel layer, diffusion region, and Al work function. The potential drop between the In_2O_3 channel layer with the estimated n-type doping concentration of 8×10^{17} cm^{-3} and the In_2O_3 diffusion region with the estimated n-type doping concentration of 2×10^{18} cm^{-3} from the diffused Al is only 0.028 V as derived from the simulation results. This potential drop of 0.028 eV is below the real sensitivity of SKPM measurement[190] and will not be visible in the measured profiles with both source and drain electrodes grounded. Hence the diffusion edge cannot be detected in Figure 4.28 for the $V_d = 0$ V profile due to the tip cone and cantilever averaging effect limiting measurement sensitivity[191].

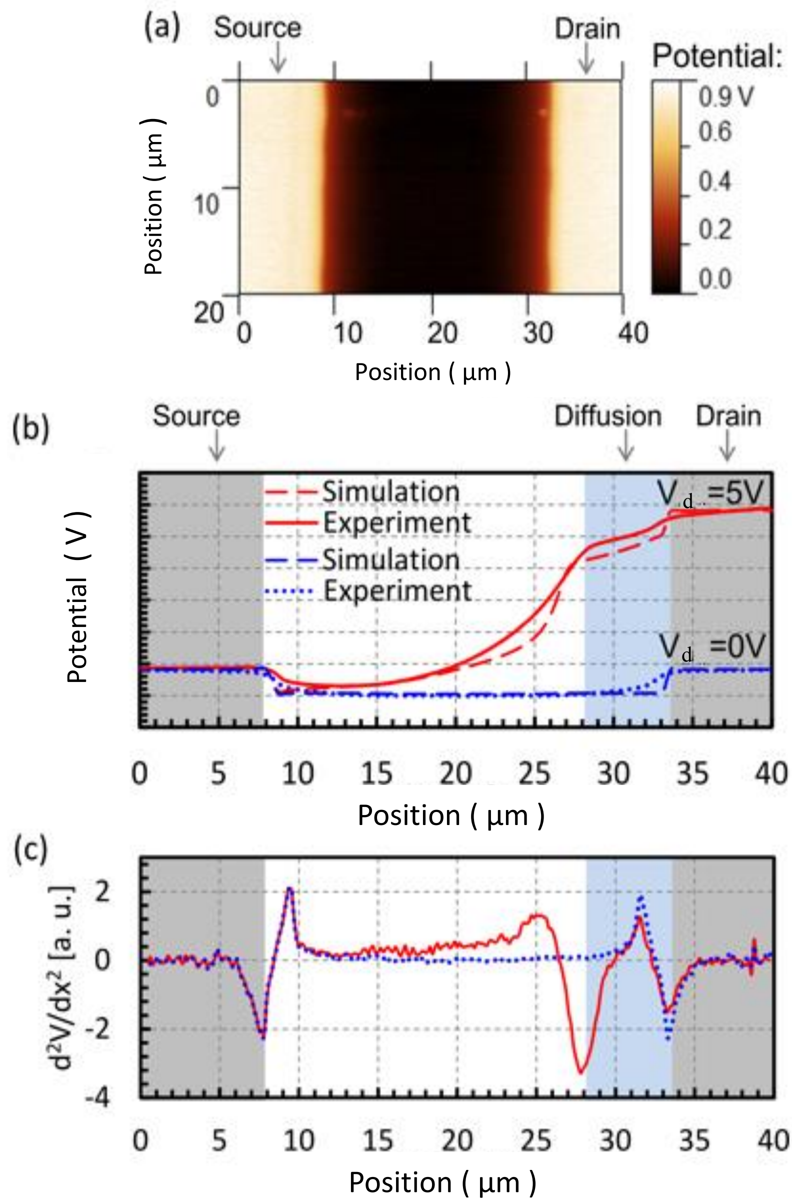


Figure 4.28: The potential distribution at the surface when the single-spin TFT is grounded. Only the source and drain electrodes can be detected at 0 V. (b) Measured and simulated potential profiles at V_d = 0 V and V_d = 5 V when V_g = 0 V. (c) Calculated second derivative of the surface potential at V_d = 0 V (dashed line) and V_d = 5 V (solid line) represents a change in the lateral electric field and allows determining exactly a diffusion region edge

A Simulation was also performed to compare the effect of gate bias. The measured and simulated potential profiles for W1000L30S device at V_d = 3 V and for gate biases V_g = 0 V and V_g = 5 V are shown in Figure 4.29 below. Applying a gate bias will introduce more carriers in the channel hence increase the conductivity of the In_2O_3 channel and screening effect of the dopants. Figure 4.29 reveals again the consistency of measured potential profile with simulation results where the potential through the channel will increase with the applied gate bias. When V_g = 5 V is applied the change of the surface potential gradient at the edge of the diffusion region reduces. That is why for a precise detection of the diffusion region edge it is recommended to take into account only SKPM profiles measured when no gate bias is applied on the TFT.

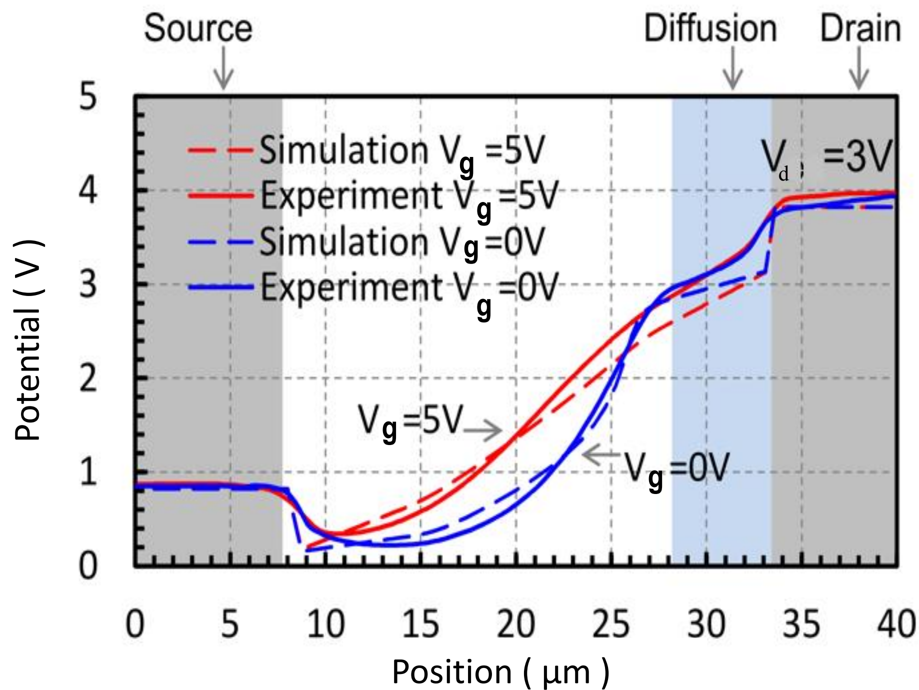


Figure 4.29: Measured and simulated potential profiles at V_d = 3 V for the single spin coating In_2O_3 TFT at V_g = 0 and V_g = 5 V.

During our SKPM investigation, we noted an interesting effect that may have other applications. We noticed that AFM measurements alone with a biased drain electrode can be used to identify the contact diffusion. When scanning above the uniformly charged diffusion region at V_d = 5 V, the AFM tip will keep the constant height from 28 µm up until the edge of the drain electrode at about 33 µm. This apparent increase in height across the Al diffusion region and the electrode arises from the feedback loop compensating for the longer-range electrostatic interaction with the tip. The topography or height profiles for range of drain biases is shown in Figure 4.30. While the measurement does not give quantitative values for potentials, it is nevertheless a sensitive test for the existence of highly doped region close to an electrode as a result of contact diffusion.

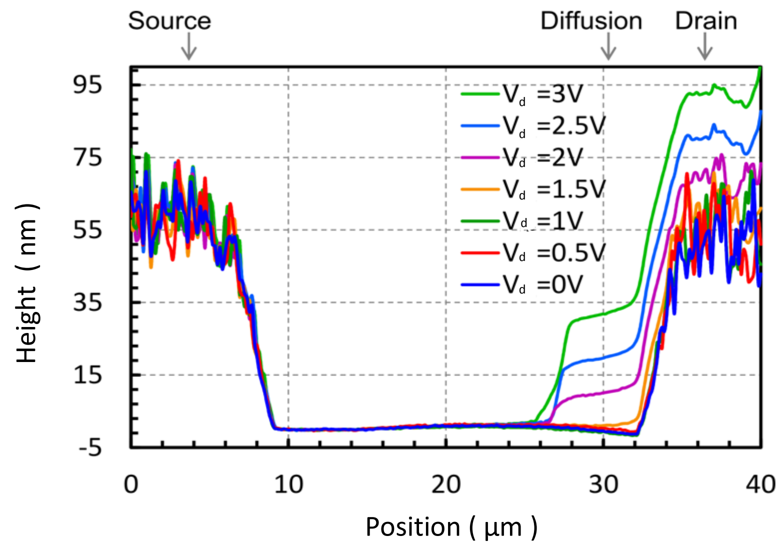


Figure 4.30: Height line scans for V_d from 0 to 3 V demonstrate the electrostatic contribution to the apparent morphology of the sample and for the drain bias V_d > 2 V position of the diffusion region can be determined.

4.11 Conclusion

In summary, we investigated the variation of electrical characteristics of single (4 nm) and double (7-8 nm) layered spin coating indium oxide TFT. The double spin coating devices revealed an increase of drain current, a shift of threshold voltage in the negative direction, an increase of off currents, small changes of on currents, and an increase of mobility. Double spin coating device showed mobility 5 times greater than its counterpart single spine device. Furthermore, it was observed that the decrease of the device length leads to deviation from hard saturation which in turn causes shift of electrical parameters such as threshold voltage and onset bias to the negative direction.

A threshold voltage shift was detected as a result of bias stress, and this shift was quantified as a function of bias stress voltage and duration. Both *I-V* and EFM spatial charge distribution measurements were used to determine the voltage instability that arises due to the process of charge trapping in the channel/dielectric interface or in the dielectric due to bias stressing effects. Also, the device recovery after stress release was investigated. All investigated devices backed to its original state (before stressing) when the gate bias was switched off and after some period of time.

SKPM was used to map the surface potential profiles and 2D images of working devices. The surface potential profiles provide a detailed picture of local potential within working transistor channel, allowing for separation of device characteristics in both linear and saturation regime. The device characteristics at fixed V_g and varied V_d showed clearly linear and super linear potential profiles relating to the linear and saturation regime for the TFT. Increasing the gate voltage leads to a change from non-linear to linear regime in 1-D profiles as a result of the gate induced charge accumulation in the channel. Small and symmetrical potential drop at contacts edges was observed, implying small contact resistance and consistent with high devices mobility.

An interesting feature of the potential profiles is a detection of a flat region close to the drain electrode. This flat region is attributed to the Al contact diffusion into the device channel. The experimental data are a greed well with the simulation results of different devices.

Chapter Five

High Spatial Resolutions Electrostatic Force Microscopy (EFM)

5.1 Introduction

Atomic force microscopy has been widely applied to map the electrical properties of a sample in nanoscale size. Martin *et al.* [192] showed the usefulness and high sensitivity of AFM for imaging surface properties and for potentiometry through the detection of electrostatic forces by using sharp tungsten tip. In this new version of AFM, settled later as an electrostatic force microscopy (EFM) technique, a conductive AFM tip is biased versus grounded sample and the derivative of force is detected.

As device dimensions become ever smaller, the capability to characterise electrical properties at microscopic scales gains greater importance. EFM measures the long range electrostatic force between the tip and sample [193] when bias is applied between tip and sample. It is a powerful technique which enables the measurements of electrostatic properties for different applications such as thin film transistors [180, 194, 195], carbon nanotube [196], solar cell [197, 198], and graphite [199]. Furthermore, it allow characterization of electrical properties such as the distribution of charge [200, 201], surface potential [202, 203], surface capacitance[204, 205], charge density and dielectric properties [206] of different materials.

Das *et al.* [202] used the phase-sensitive EFM technique to investigate the surface and electronic characteristics of poly(3-hexylthiophene) (P3HT) and poly(9,9-dioctylfluorene) (F8) polymers between Au contacts. The EFM data showed, that the bottom and top contacts configuration has a dramatic effects on the device performance, detecting differences in conductivity of two films by EFM, a sharp drop in potential at the top contact in the F8 film, and trapped charge in the F8 polymer on an untreated silicon substrate which has impact on charge transport. Krayev and Talroze in 2004

[207] reported EFM ability for analysis of thin films of dielectric heterogeneous polymer blends composed of polymers with different dielectric constants. Gupta *et al.* [208] used the EFM-phase method to show the electrical conductivity heterogeneity of boron doped diamond films. Simultaneous topography and EFM-phase images revealed electrically non-active regions with isolated sites of high conductivity. These conducting sites are randomly distributed over the surface, having submicron diameters, being well distinguish through sharp phase contrast. Castellano-Hernandez *et al.*[209] used EFM to determine the dielectric constant of many nanometre thickness films and presented numerical calculations of electrostatic interaction between tip and sample. Also, the calculation showed that the EFM signal sensitivity will increase when using substrates with low dielectric constant. Lei *et al.*[204] carried out analytical calculations for metallic tip-sample capacitance and its gradient to demonstrate resolution difference between SKPM and EFM (phase mode) and the results agreed well with experimental data. Also, the latter showed the changes of tip apex, cone, and cantilever capacitance as a function of tip-sample separations. Lilliu *et al.*[210] have reported a technique for EFM mapping into 2D images. The technique permits simultaneous probing, in the same scanning area, of the contact potential difference (CPD) and the second derivative of the capacitance between tip-sample. For this purpose, an open-source MATLAB Graphical User Interface (GUI) for images acquisition, processing and analysis has been developed.

Here in this chapter we will discuss the theory and fundamental principles of electrostatic force microscopy (phase mode) and how phase correlates with voltage. The initial aim of the chapter will focus on experimental techniques and instrumentation needed for measuring EFM. After the initial discussion, we outline some issues that appeared during experiments and we review several studies such as effect of tip height, tip bias, type of applied signal, scan size, and signal frequency performed to sort these issues. Later we present new software designed as phase-corrected EFM for sorting the main issue. We apply our software to test some surfaces like Au(111)/mica, graphite, and MDMO-PPV/PCBM. Following these test samples, the results of applying this approach to working biased field effect transistor devices is presented and related issues discussed.

Finally, we compare SKPM and EFM phase measurements and survey the main results of this chapter and suggestions for future work.

5.2 EFM phase measurements and its theory

Electrostatic force microscopy is an important type of scanning probe microscopy, distinct from AFM, devoted to measure the long rang electrostatic force between sample – and tip when a bias applied between them [192, 193, 211]. EFM tips are usually coated with a thin metal film in order to ensure its conductivity but sometime its application for qualitative imaging is hindered by tip geometric effects and cross talk between topographic potential effects [212]. The electrostatic force is proportional to the square of the voltage between the tip and the sample. Likewise, the convenient lock-in technique in addition to ac and dc voltage can measure electrostatic interaction with high accuracy. In this way we increase the sensitivity and allow proper discrimination against other type of forces which not depend on the bias.

Although SKPM provides a direct potential measurement of the surface, its spatial resolution which is around 100nm [213], limits its use for high precision experiments. That is because the long range Coulomb force includes contributions from the cantilever, tip cone, and tip apex. One way of reducing the impacts of the cantilever and tip cone is to use a probe with a narrow cantilever, a high angle tip cone, and small tip radius. A more versatile approach is to employ an EFM mode that measure the force gradient $\frac{dF_z}{dz}$ instead of the force itself [214]. In this case the above effects are avoided and the tip apex will be the principal contributor in detection. Lei *et al.*[215] have demonstrated and confirmed experimentally lateral resolution of about 20nm using what they called the EFM-phase mode. As well, in order to avoid cross talk from topography signal, a binary pass method is adopted. Following an initial topography scan in intermittent contact mode, the tip is lifted a fixed height (typically 20 – 30 nm), a bias is applied to the tip and the phase difference is recorded. This technique assumes that the impact of other forces such as van der Waals interaction will diminish in this lift mode so that only the effect of electrostatic interaction is measured.

The tip-sample applied bias voltage stimulates an electric field according to the equation:

$$\boldsymbol{E}(x,y,z) = -\boldsymbol{\nabla}V(x,y,z) \tag{5.1}$$

This correlates with charge distribution according to Maxwell Equation

$$div\boldsymbol{E} = \frac{\rho}{\varepsilon_o} \qquad (5.2)$$

where ρ, ε_o are the charge density and space permittivity (8.85 10^{-12} F/m) respectively.

The electric field thus leads to an interaction energy (U) between the tip and sample [216]

$$U_{tip-sample} = \frac{1}{2}\int k\varepsilon_o\, \boldsymbol{E}^2\; dv \;= \frac{1}{2}\; C\, V^2 \qquad (5.3)$$

Since the electric interaction, potential, and electric force depends on the tip – sample separation in the z- direction, we get

$$F_{tip-sample}\,(z) = -\frac{dU}{dz} = \frac{1}{2}\,\frac{dC(z)}{dz}\; V_{tot}^2 \qquad (5.4)$$

where C(z) is the capacitance between tip and sample and $V_{tot} = V - \Delta V$ [ΔV is the CPD(contact potential difference) between sample and tip]. In a Kelvin probe, the sum of ac and dc bias is applied to the tip during lift mode where the dc component (feedback system) is controlled by a feedback loop to minimize the cantilever vibration amplitude, Hence *F(z)* is nullified which led to a direct measurement of surface potential. However, in EFM phase mode the force gradient rather than force is measured. This reveals an enhanced special resolution compared to KPM [217]. This operation method ensure that in lift mode the electrostatic interaction force is the dominant one because both van der Waals and chemical force minimized exponentially as the tip moved away from sample surface [206].

In EFM phase mode, as the cantilever is driven to oscillate at or close to its natural frequency ω_o, and for freely vibrating cantilever of spring constant k, effective mass *m*, quality factor *Q*. The phase angle *Φ* of the cantilever oscillation relative to ω_o can be expressed as [206, 218].

$$\Phi = \tan^{-1}\left(\frac{m\omega\omega_o}{Q(k-m\omega^2)}\right)$$

or

$$\tan\Phi = \frac{\omega\omega_o}{Q(\omega_o^2-\omega^2)} \tag{5.5}$$

where ω is the actual cantilever vibration. If $\omega = \omega_o$ (freely oscillating cantilever) then there is a phase differe $\Phi = \frac{\pi}{2}$ between the sinusoidal drive signal and the cantilever oscillation [206].

In EFM experiments, when the tip is close to the surface, the force gradient $\frac{dF}{dz}$ (because of varied tip – sample interaction) modifies the vibrating cantilever's effective spring constant k , and consequently affects phase angle *Φ*. In the case of small cantilever oscillation amplitude the force gradient $\frac{dF}{dz} \ll k$, the phase angle become [218].

$$\Phi = \tan^{-1}\left(\frac{k}{Q\ (dF/dz)}\right) \approx \frac{\pi}{2} - \frac{Q}{k}\frac{dF}{dz} \tag{5.6}$$

It is important to mention that the force gradient representing all force derivative acting in normal direction between tip – sample. The above equation can be written without the π/2 term if the phase shift is perceived as the delay from free oscillation stat of cantilever. So, we write

$$\Phi = -\frac{Q}{k}\frac{dF}{dz} \tag{5.7}$$

Hence, the phase shift is proportional to the sum of all the force gradients between tip and the sample. The sign of Equation 5.7 is negative for attractive forces and positive if the overall forces are repulsive. By combining Equation 5.4 and Equation 5.7 we obtain:

$$\Phi = -\frac{Q}{2k}\frac{d^2C(z)}{d^2z}\,(V_{tot})^2 \qquad (5.8)$$

For a parallel plate capacitor, the capacitance is approximatly $C(z) = \varepsilon_0\,k\,S/z$ where k, ε_o, S (Equation 2.8) are the dielectric constant , space permittivity, and the surface area respectively. Hence, the force is attractive in a purely capacitive tip - sample and the measured phase shift is always negative.

$$\Phi = -\frac{Q}{2k}\frac{d^2C(z)}{d^2z}\,(V - \Delta V)^2 \qquad (5.9)$$

This can be expressed as a simple function for fitting

$$\Phi = A\,(V - B)^2 + c \qquad (5.10)$$

where A = $-\frac{Q}{2k}\frac{d^2C(z)}{d^2z}$, B = ΔV, and c is the phase offset. In our experiments the bias is applied to the tip and sample left electrically grounded. Since there is no feedback voltage applied, the raw EFM data needs to be calibrated to determine the above parameters. Accordingly, the equation shows that in lift mode EFM the second derivative of the capacitance and contact potential difference can be extracted with parabolic fit.

5.3 Experimental details

1- EFM (phase mode) measurements done in our Vecco clean and dark room and all experiments used a Nano-Scope® IIIa multimode™ with Extender™ electronic model which allows recording of three separate channels. A highly doped n^+-Si Pt/Ir coated tip of resonance frequency 70- 85 kHz is used. Tip thickness: 3.0±1μm, length: 225±10 μm, width: 28±10μm and the tip resistivity 0.01- 0.02 Ω cm utilized during experiments.

2- In all experiments the sample was grounded and EFM tip was biased. The pins inside Multimode were accessed via an extension of wire across AFM base forming eight separate connectors which facilities the electrical connection with tip or sample Figure 5.1.

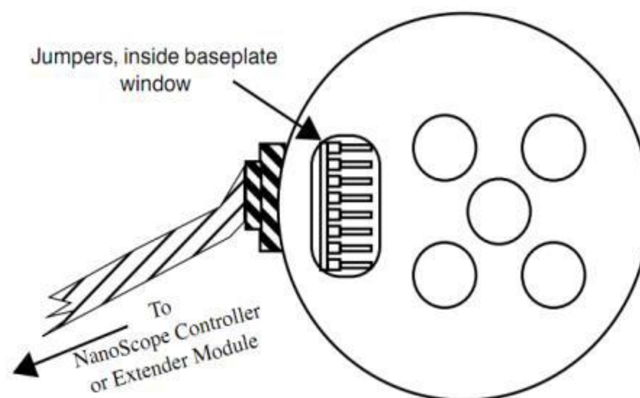


Figure 5.1: Multimode base plate showing location and orientation of jumpers [Vecco manual(2004)]

3- The voltage is applied to the tip by a Agilent (A33220A,USA, 20 MHz) wave form signal generator which enables different waveforms with varied bias and frequency. The outside accessed pin is connected to the Agilent via coaxial wire as shown in Figure 5.2 below.

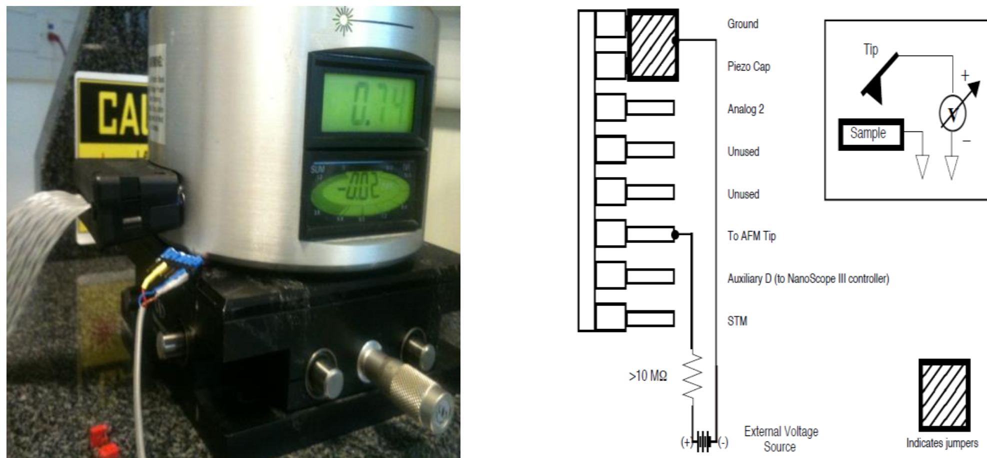


Figure 5.2: Jumper configuration of applied voltage to the tip

4- Before EFM scanning, proper images of surface topography should be obtained. To ensure that the voltage is applied to the tip only in lift mode, a triggering module was constructed by R Tucker which is used to switch on drain and tip voltages at the start of the lift mode scan. The circuit diagram of the device is shown in Figure 5.3.

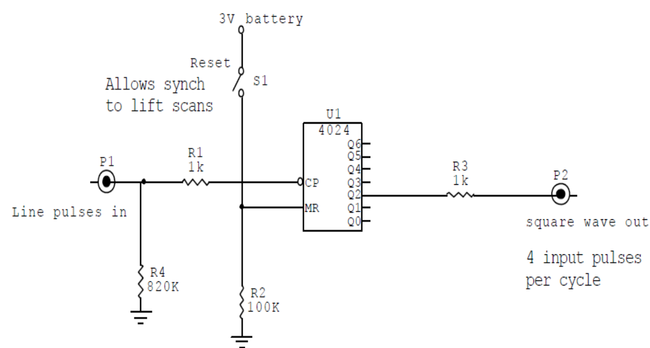


Figure 5.3: Triggering module for EFM synchronization

A scan thus has four segments repeated cyclically, topographic trace, topographic retrace and lift trace, lift retrace. Our device was made in such way that it apply bias only in lift trace and lift retrace and leaves other segments at zero bias.

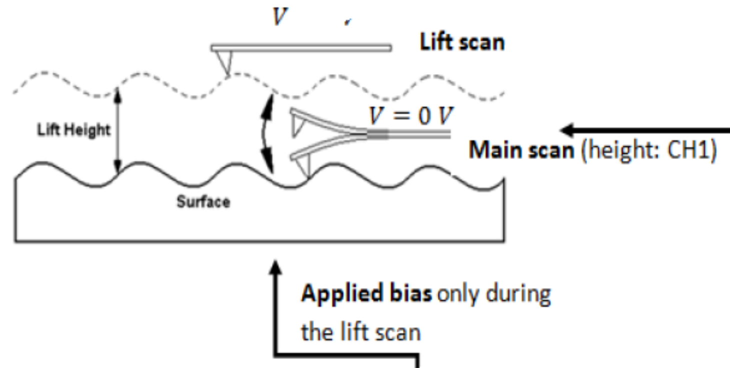
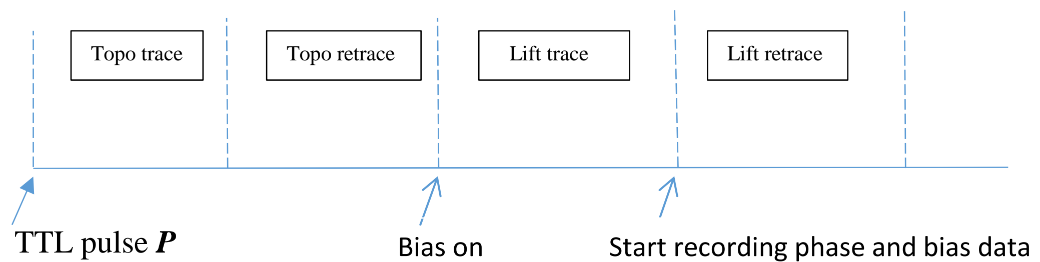


Figure 5.4: Diagram of EFM scanning process in height and lift mode

5- Synchronization between line scan and applied bias was achieved with the trigger module described in 4 above: it was adjusted so that the biases were switched on at the start of the lift trace segment and the phase mode and bias recorded during the retrace lift mode.



As was mentioned, our Multimode system permits recording only three channels. The first channel monitored the height image for main scan in tapping AFM mode. The second channel for measured the applied voltage wave form while the third channel recorded the corresponding phase shift. The last two channels must be measured during the lift mode part of the scan. The experiments were performed under an earthed metallic hood, through which nitrogen was continually flushed. Suitable amplitude set point, drive amplitude and gain were adjusted to achieve good topographic images with

a scan rate of around 1 Hz [219], Vecco Manual). The EFM data was recorded with typical lift mode height of 20 nm, taking care to set up the triggering correctly.

5.4 Imaging processing and data analysis

Phase –voltage calibration is the first priority before any investigation of the sample surface. **Gwyddion** software for Scanning Probe Microscopy (SPM) and data analysis implemented directly to process our captured images.

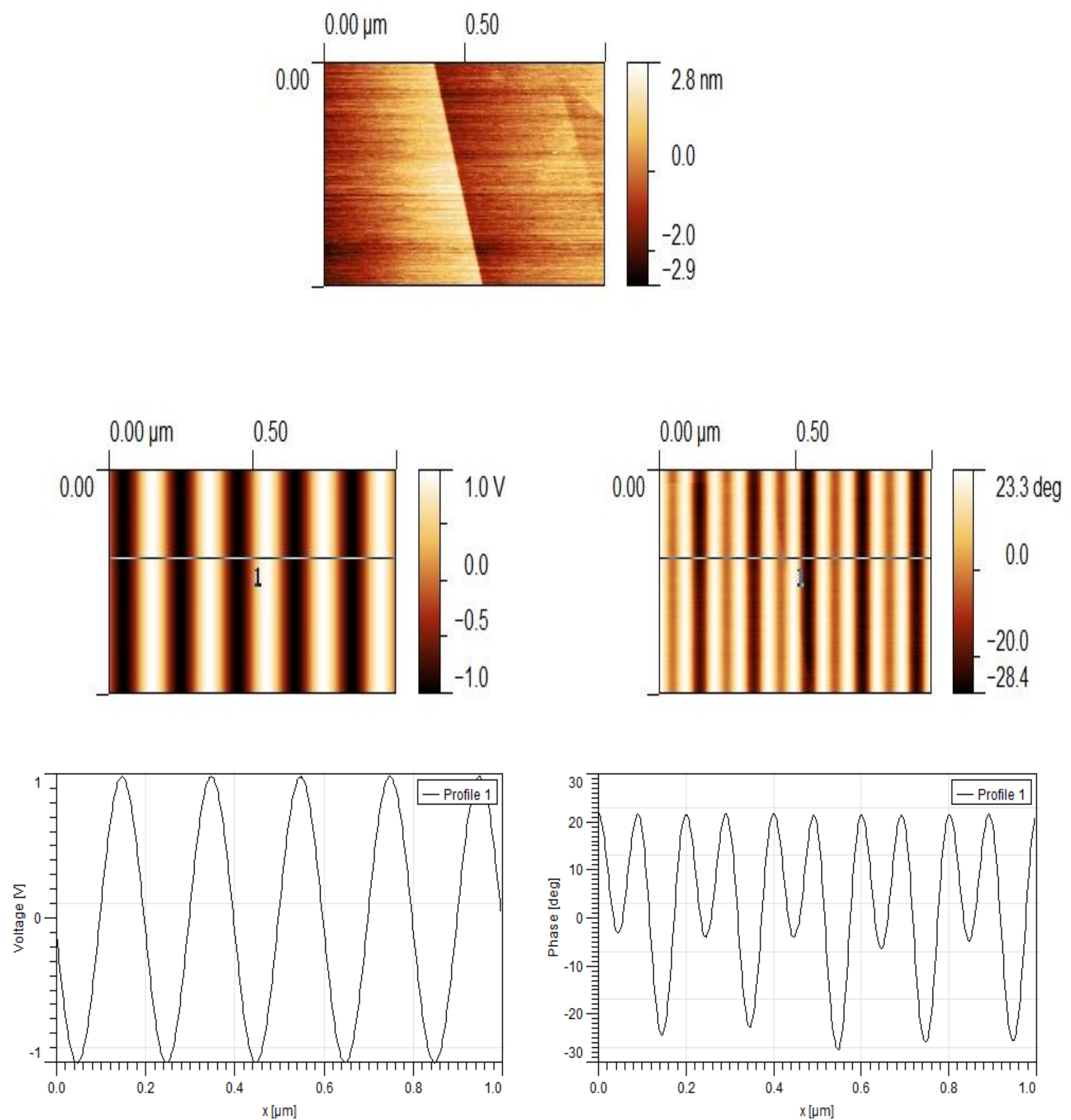


Figure 5.5: AFM captured image for graphite surface for 1µm scan size (top) and applied 1 V AC signal, 10 Hz AC sinusoidal signal (left) with corresponding phase shift (right)

To reach such aim, a straight line on voltage and corresponding line on phase images were drawn by accurately specifying their starts and ends point. Then the voltage data at each pixel and corresponding phase shift can be extracted by the same software and converted to the separate file for data analysis processing and plotting. Figure 5.5 shows the topography of graphite surface at 1 μm scan size during EFM experiment. As it is clear there is no influence of applied bias during height scanning which confirms that the bias is only subjected at lift mode. AC 1 V signal and frequency 10 Hz is applied to the tip. The result of phase shift and applied voltage calibration curve is illustrated in Figure 5.6 below.

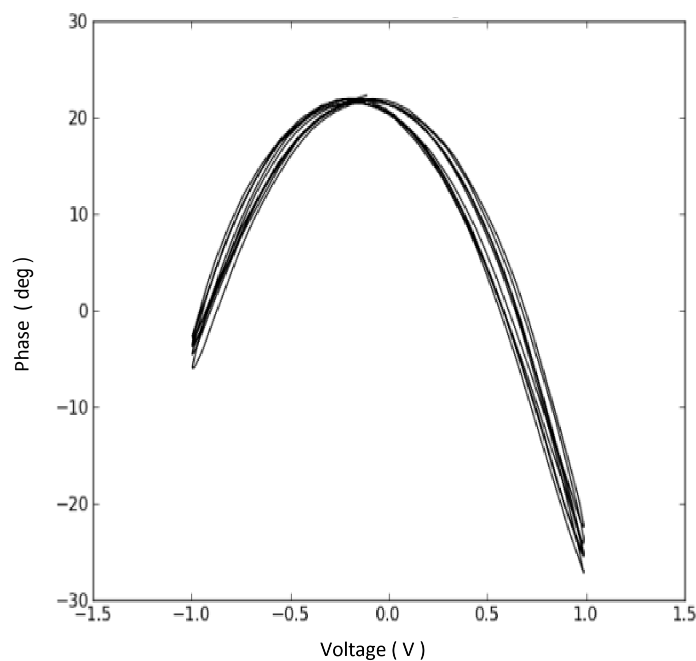


Figure 5.6: Phase- voltage calibration curve with AC sinusoidal signal at 1 V tip bias and 10 Hz. The tip height is 20 nm, scan rate 1 Hz and scan size is 1μm.

The theoretical basis of phase shift by applied voltage to the tip is a parabolic relation Equation 5.10. However, Figure 5.6 demonstrates that the phase-voltage data spreads over two shifted parabola rather than a single well-defined parabola one which was puzzling. Similar effects were observed on other surfaces. Therefore, during our study we tried to study different parameters that might be affected on our results and helps to solve this problem.

5.4.1 Study 1: Effect of scan size

The first study to tackle the above issue is decreasing the scan size to nm scale. As in this case we can minimize the effect of height and obtain clearer phase data. Figure 5.7 shows the image under the same experimental condition but at 5nm scan size.

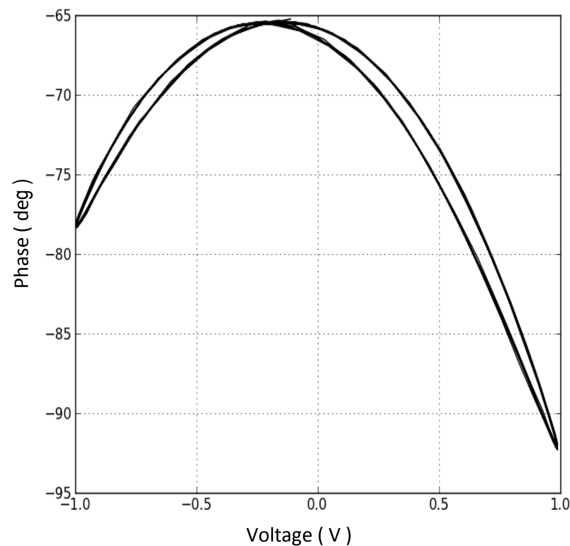


Figure 5.7: Phase-voltage parabola image for 5nm scan size, 1 Hz scan rate, frequency 10 Hz and bias 1V

Figure 5.7 shows clearly that the data is distributed over two distinct parabola and no improvements of shift with decreasing of scan size.

5.4.2 Study 2: Effect of tip height

According to Equation 5.6 we can obtain the force gradient from the phase signal. During our experiments we noticed that it's difficult to obtain the phase signal for tip height below 15 nm because the electrostatic force was so strong causing sometime crash of tip over the sample. Furthermore, for lift height above 200 nm it is difficult to identify the noise from the signal. The effect of tip-sample capacitance also investigated by increasing the tip height from 20 – 150 nm with step 10 nm. No visible or sensible improvement was detected because this capacitance is still quite small arising from the fact that the tip apex is a main contributor in imaging process in EFM (phase mode). We tried applying different types of signals such as sinusoidal, triangle, saw tooth and so on. The images below shows phase -voltage calibration for two types of signal. Again we see no effect of tip height on parabola shifts but only on phase shifts as the electrostatic interaction increase with decreasing distance between tip and sample.

a). Sinusoidal signal

Firstly, we applied a sinusoidal waveform to the tip and we studied the phase-voltage relations. A double parabola is obtained as it is clear in Figure 5.8

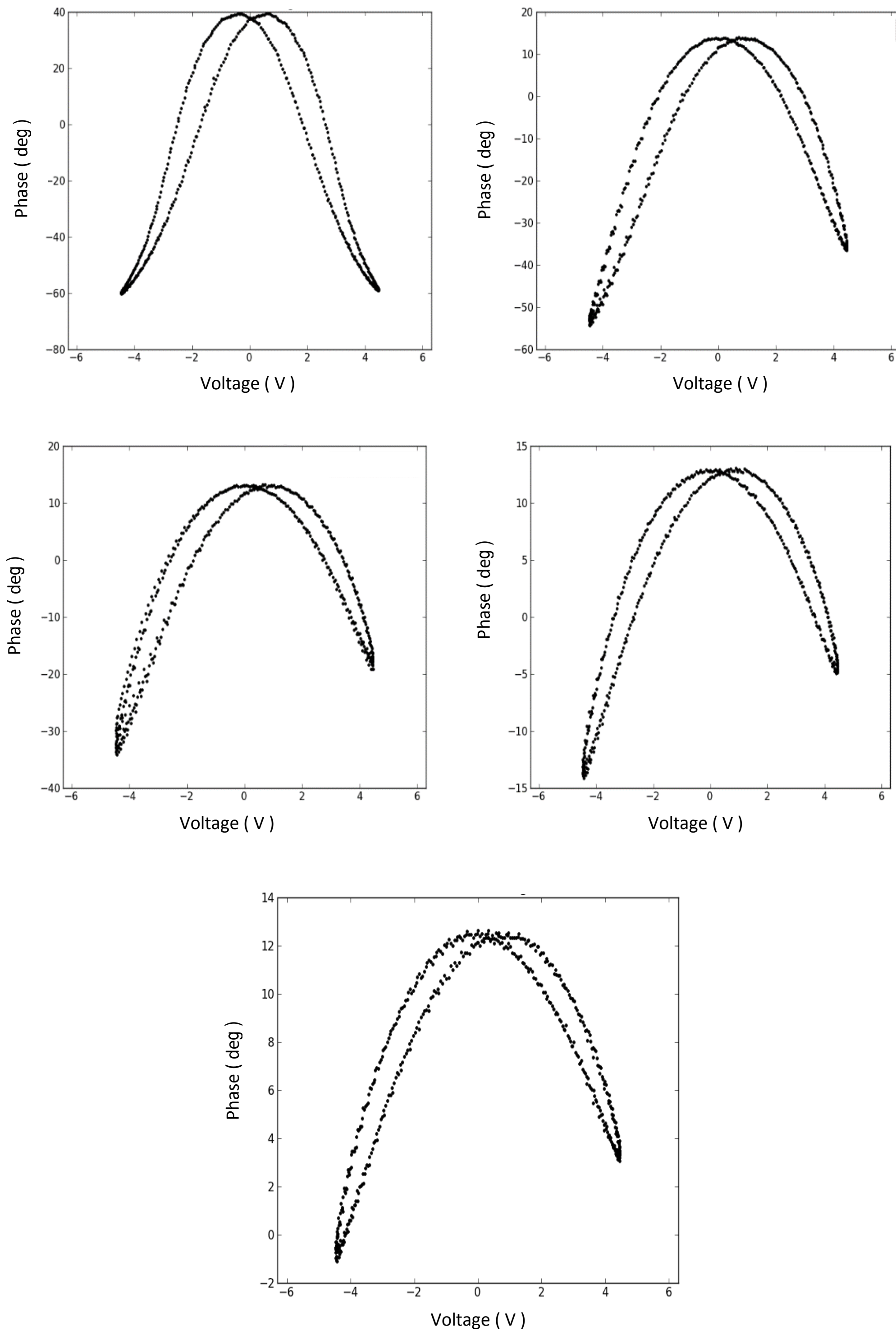


Figure 5.8: Phase-voltage parabola with different tip height 20nm (top right), 50nm (top left), 70nm (middle left), 100 nm (middle right), 150nm (bottom). Scan size 5nm, tip bias 4.5 V and frequency 12 Hz.

b). Applying triangle signal

A second type of applied signal was a triangle waveform, Figure 5.9 below shows phase-voltage calibration after applying tringle signal.

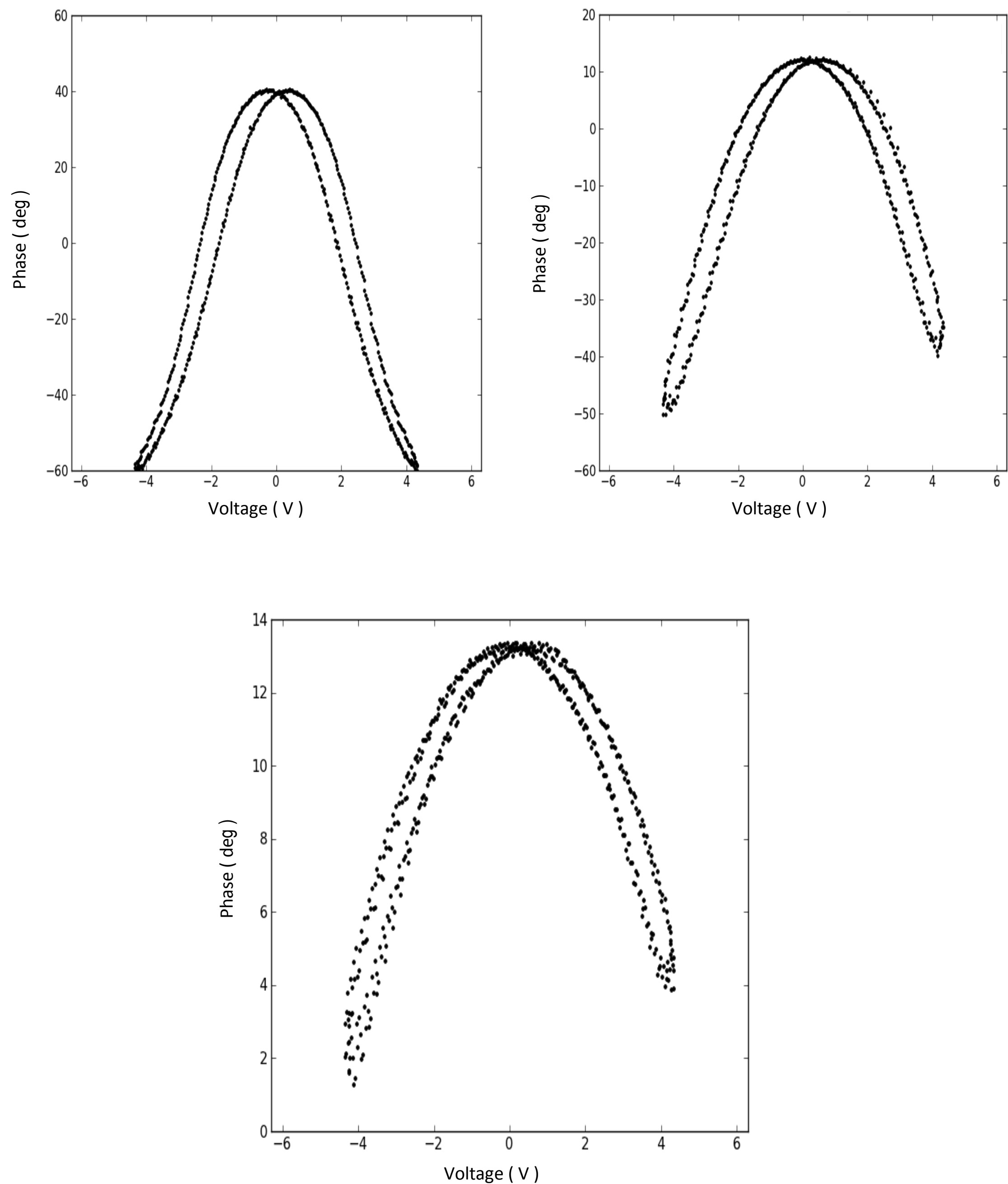


Figure 5.9: Phase-voltage parabola with tringle wave form of bias 4.5 V, frequency 12 Hz and tip height 20 nm (top left), 50 nm (top right), 150 nm bottom.

5.4.3 Study 3: Effect of tip bias

Then we tried to study the effect of tip bias on the type of produced parabola before doing the study of the potential of the required surface. The effect is increasing of electrostatic interaction only and no improvements noticed on the amount of shifts. Figure 5.10 shows phase-voltage curves for tip biases 1, 2, 3, 4 V.

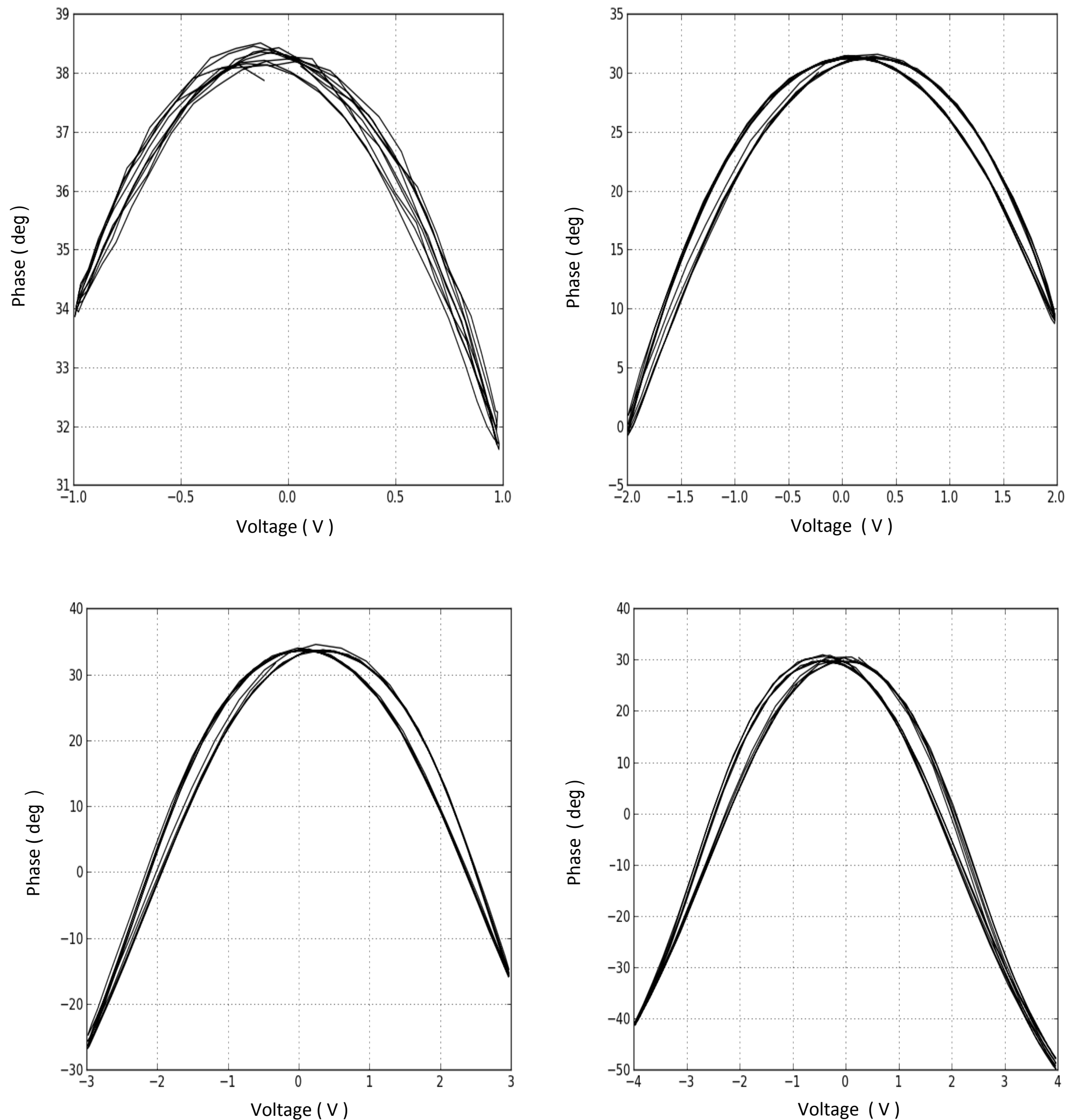


Figure 5.10: Phase-voltage calibration curve for various tip biases 1, 2, 3, and 4 V. The signal frequency is 10 Hz, tip height 20 nm and scan size is 1 µm.

5.4.4 Study 4 :Effect of signal frequency

During our investigation we noticed a big effect of frequency on the parabola shift: the shift increased with increasing frequency. The figures below show the impact of frequency change on parabolas. We tried to check the situation without and with connecting 8 MΩ resistance to the tip.

a). Without resistance

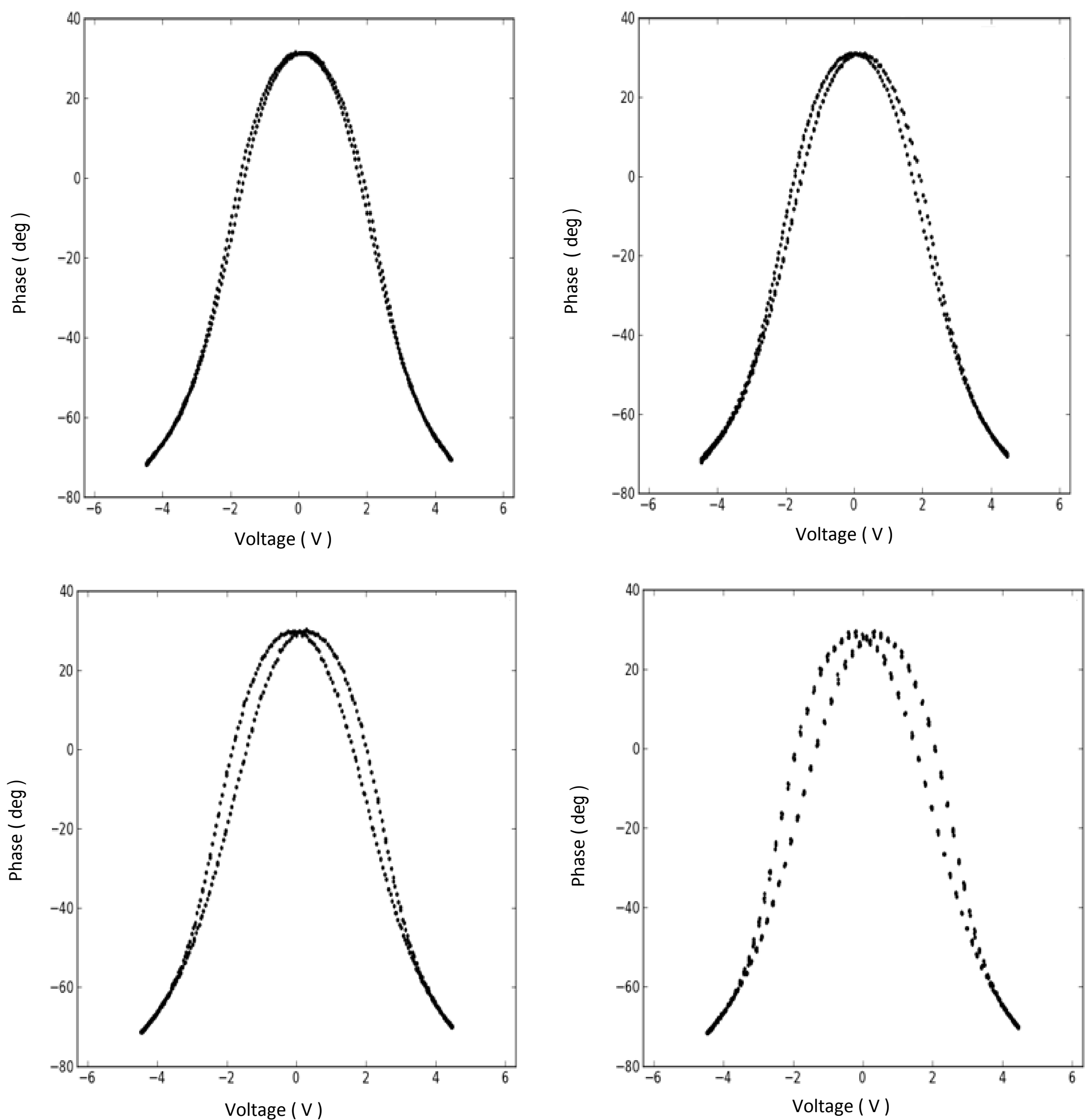


Figure 5.11a: Phase-voltage parabola for sinusoidal wave form of varied frequency 2 Hz (top left), 5 Hz (top right), 10 Hz (bottom left), 15 Hz (bottom right), tip bias 4.5 V, and 20 nm tip height

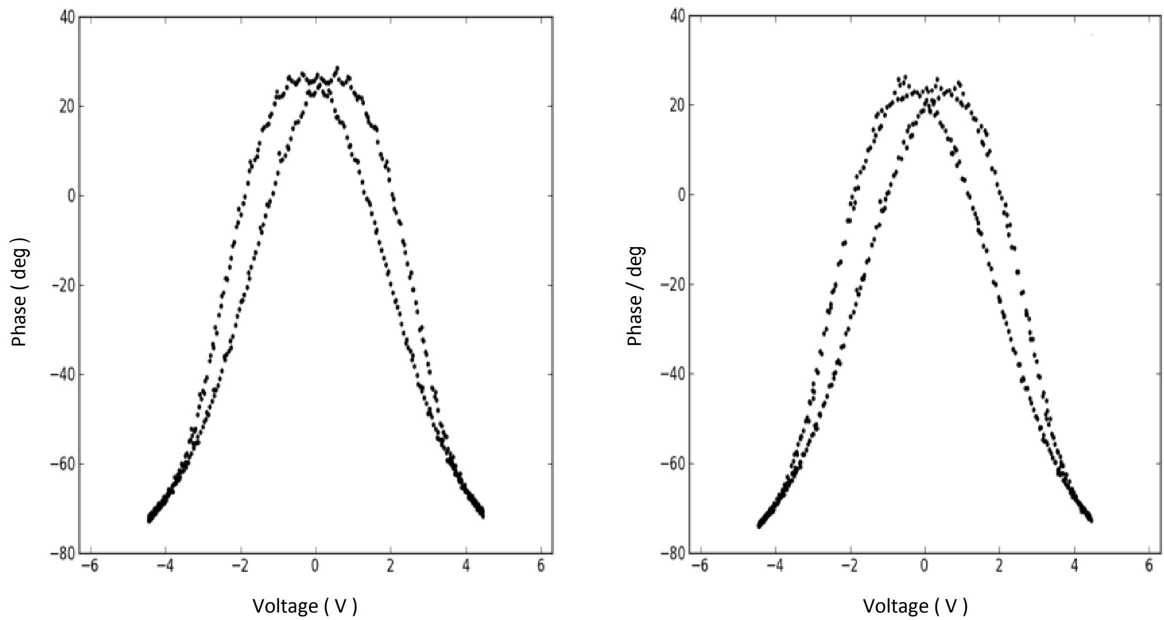


Figure 5.11b: Phase-voltage parabola for sinusoidal wave form at frequency 20 Hz (right) and 25 Hz (left), tip bias 4.5V, and 20nm tip height.

Figure: 5.11a,b above shows the phase-voltage parabola before connecting 8 MΩ resistance to the tip.

b). Connecting 8 MΩ resistance in series with tip.

Figure 5.12 below shows the phase-voltage calibration curve after connecting 8 MΩ in series with tip.

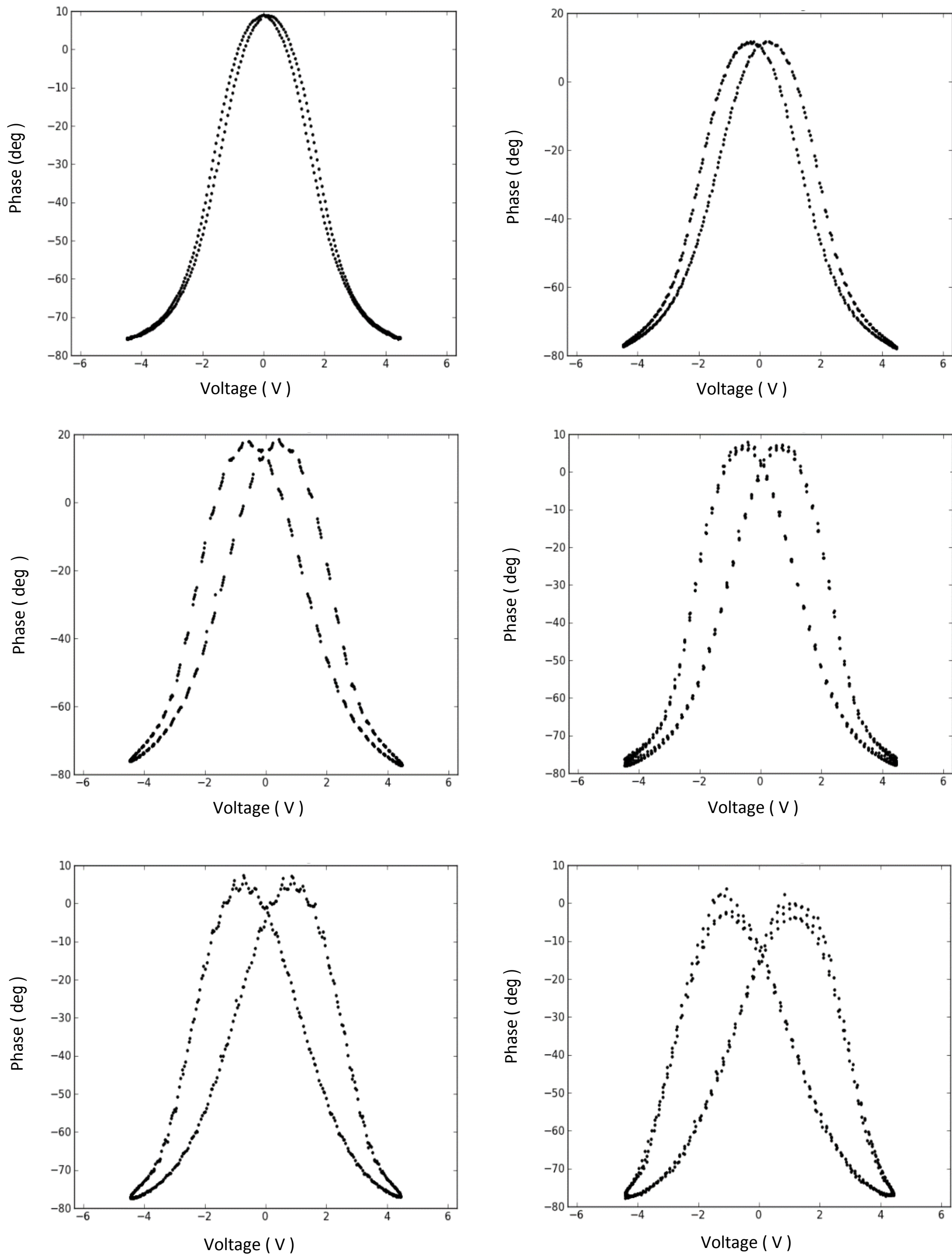


Figure 5.12: Phase-voltage curves after connecting 8 MΩ resistance in series with the tip. The images for 2 Hz (top left), 5 Hz (top right), 12 Hz (middle left), 15 Hz (middle right), 20 Hz (bottom left), 30 Hz (bottom right). Tip bias is 4.5V, tip –sample separation = 20 nm.

As it is obvious that the shifts between two parabolas increase with increasing signal frequency. However, we cannot use a very low frequency as we need to sample full parabolas locally during a normal AFM scan. On the other hand, we want to decrease frequency to minimize parabolas shift and reduce the cross talk between electrical and mechanical signal. However, we need to make a large number of cycles in order to increase the number of points (details come later) per pixel of images and decrease the noise in lock in detection [201]. Comparing two sets of parabola (with and without resistance) we see the shift of parabola increase with connecting resistance at same frequency value and same experimental conditions.

Furthermore, in order to increase the number of cycles we have to increase the frequency (f) over applied AC voltage which we found causes a dramatic growth of parabolas shift (ΔV) as it is clear in Figure 5.11 and Figure 5.12 above. Moreover, our experiments reveals a linear relation between shift in parabola and signal frequency.

Fig.5-13 below demonstrates correlation between (ΔV) and (f) with and without of 8MΩ resistance connected in series with tip. From varied (ΔV) and (f) values we can get an estimate of the time constant(τ) which is the most required parameter in developing a new software for data processing and analysis.

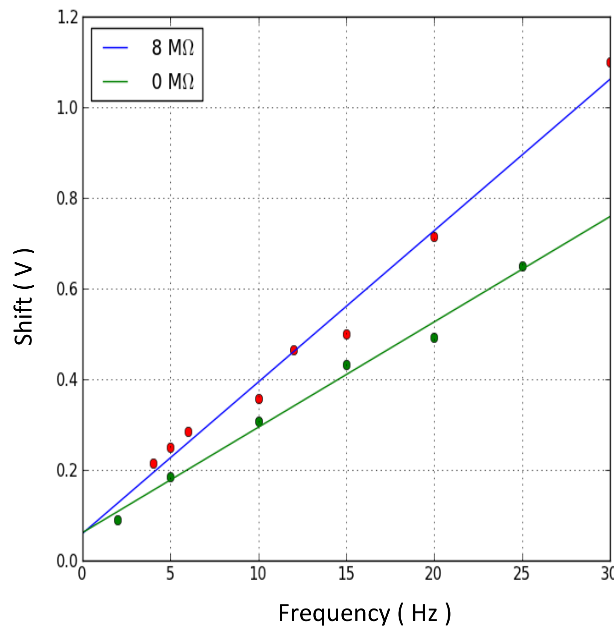


Figure 5.13: Parabola shifts as a function of frequency with and without connecting 8 MΩ resistance.

The shift of parabolas seems to be caused by a time delay between sensing and applied bias arising from a capacitive effect or different time response for rising and falling waveform [219]. Therefore, according to the above we can plot only for half cycle the phase –voltage relation only (rising or falling voltage) the result is only one parabola

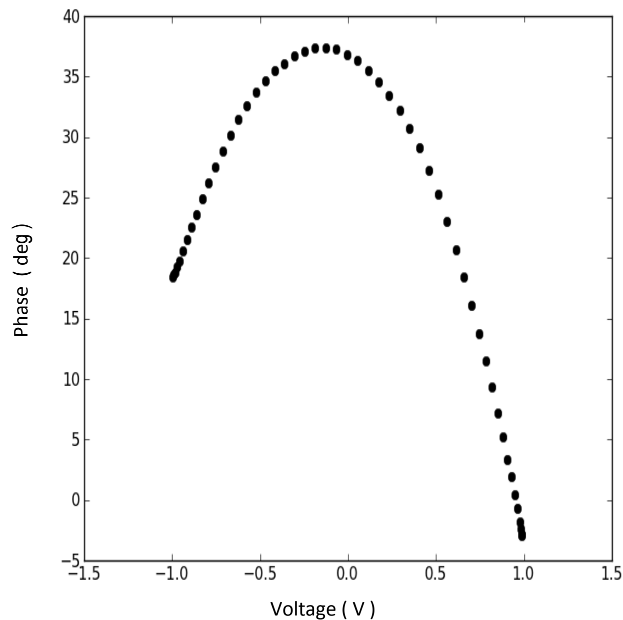


Figure 5.14: The phase-voltage calibration curve for only half of signal

Applying of half signal is of course is not true situation about what happening during experiment therefore we need to treat the problem for general case to see exactly what is going on.

5.5 Design of a new software for EFM data

The development of new software with the ability to open SPM files and data processing is a crucial way to overcome from above difficulties. Therefore, the first step of software should contain python code that be able to open the Vecco image file and then use the information in the file to extract images data array and all useful information. The Vecco system that we used allows display only three channels which are channel 1 (for height or topography), channel 2 (display bias on the tip), and channel 3 (shows the resulting phase signal).

Figure 5.15 below shows three obtained images of EFM experiment data on gold Au(111)/mica by using the new software. The surface of gold is relatively rough and grainy.

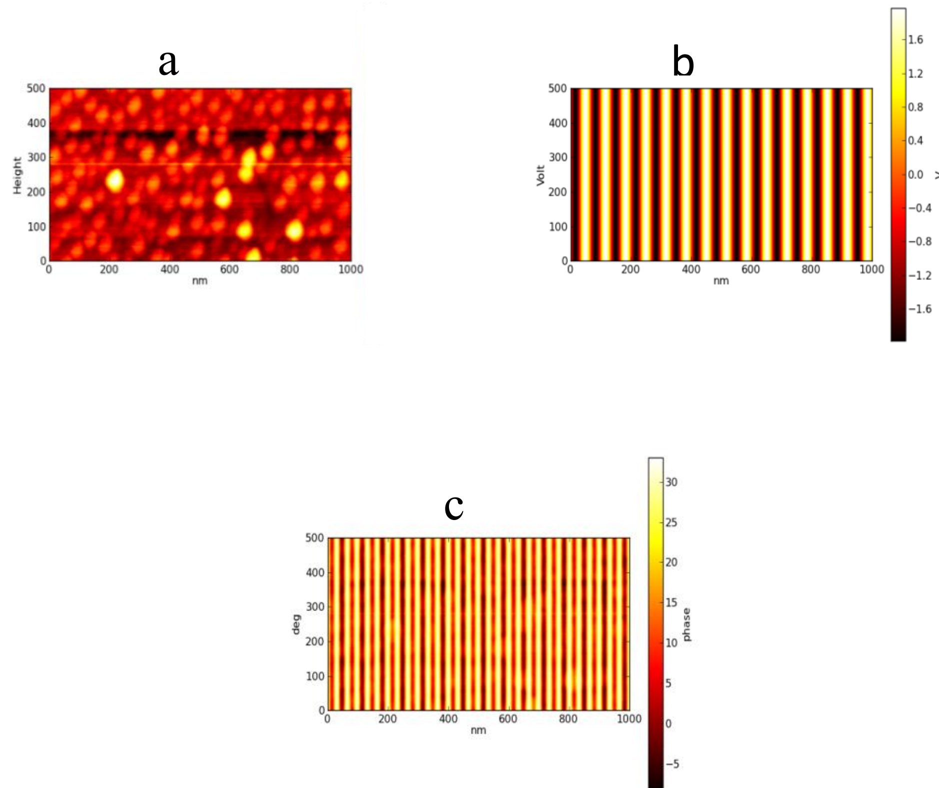


Figure 5.15: a), Topography, b), bias of signal frequency of 30 Hz, c), the resulting phase shift obtained by using the new software.

The second step should specify the voltage and corresponding phase data for each pixel as we did in Gwydion software for same raw in addition to a set of essential parameters needed in other parts of program. Figure 5.16 depicts the measured voltage and corresponding phase across first row obtained from Figure 5.15 by new software.

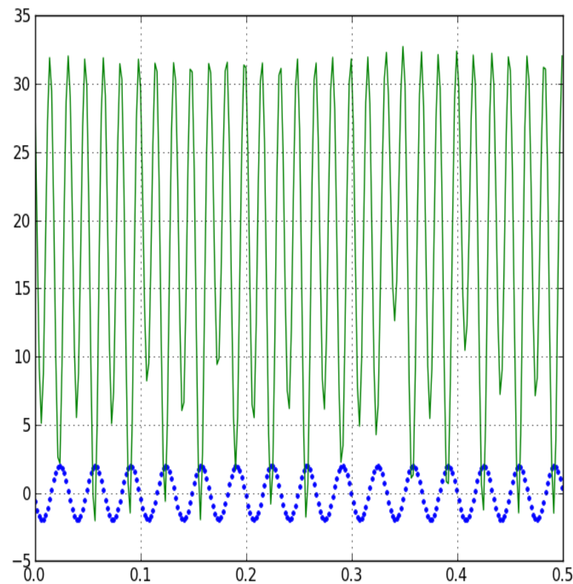


Figure 5.16: The measured voltage data (blue) and corresponding phase (green) for first row obtained from figure 5.15. The applied tip bias is 2 V, frequency 30 Hz.

The basic idea behind the new software is to work back from the measured output, affected by the time delay, to determine the undelayed input signal, assuming that the time delay is the result of electrostatic charging. The using of the filter function in python program by defining the function **Filter (*V*, *α*): (**which is a simple 1-pole digital filter, equivalent to a low-pass RC filter. It takes an input array V (original) and returns a filtered output in array $V_{o,}$ where alpha is the ratio dt / (dt + τ) where dt is the sample rate of x and **τ** is the time constant).

V_o = **Filter1**(V, $dt/(dt+ \tau)$)

and invert filter using **InvFilter** (v_o , α)**:** **(** Invert the simple 1-pole digital filter. Takes array V_o and returns unfiltered array V_{in}).

V_{in} = **InvFilter1**(V_o, dt / (dt+τ))

The routine requires the time delay, the scan rate and the number of data points. The new set of data points $V_{new} = V_{in}$ (which is the voltage lagging that reflects the effect of time delay) and the measured corresponding raw phase data (after converting it to true degree) can be used for calibration.

Figure 5.17 below shows phase –voltage calibration curve before (red dots) and after using the software (black dots) for various frequency values over the first row. The huge improvement with using the new software is clear and we see no parabola shifts appear. However, we notice an obvious shifts of red points over two shifted parabola which dependent on frequency.

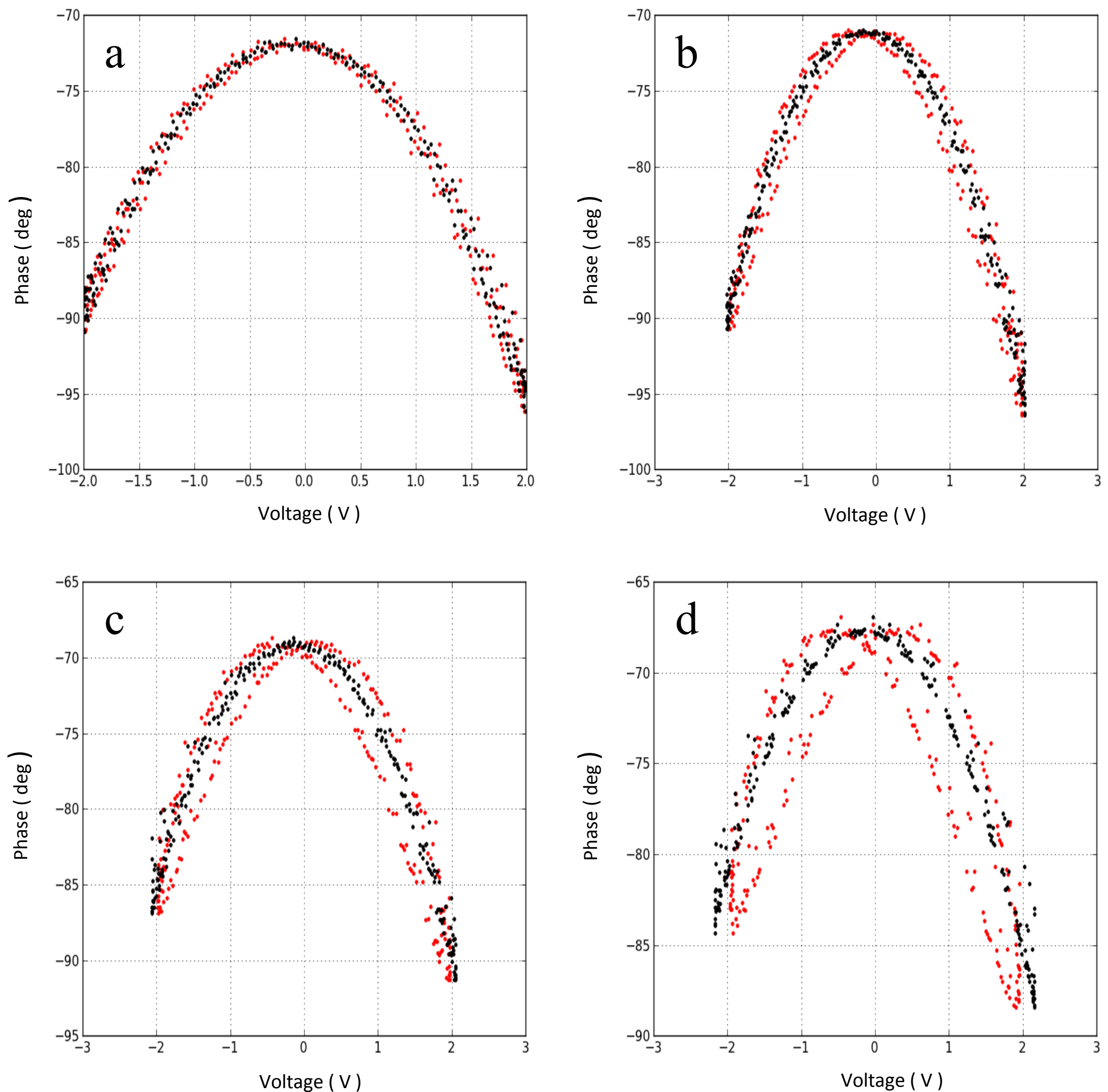


Figure 5.17: Phase-voltage calibration curves before (red dots) and after (black dots) applying time delay for different frequencies. a),10 Hz, b) 20 Hz, c), 30 Hz, d), 50 Hz with tip height 20 nm for all. All above images are for one whole line profile.

A clear picture is shown in Figure 5.18 where we fit the first raw of data from Figure 5.15 with the function:

$$\Phi = (\,[P0]\; - \;\arcsin(P[2] * (\mathrm{x} - P[1]) ** 2) \qquad (5.11)$$

where *P[0], P[1], P[2]* are fitting parameters.

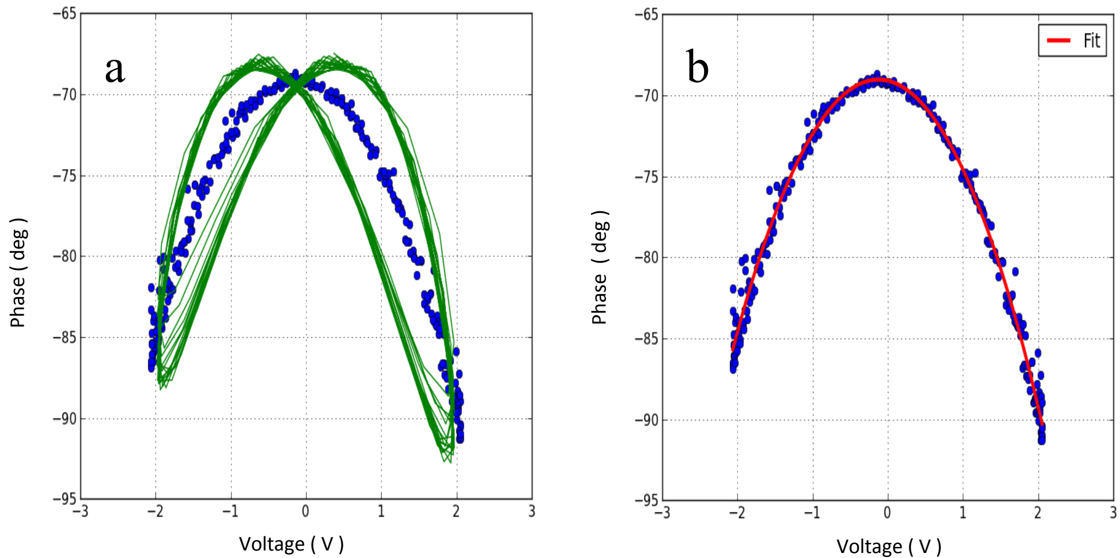


Figure 5.18: A clear improvement in phase-voltage calibration curve after applying the effect of time delay. The above image is for *f* = 30 Hz, *d* = 20 nm on gold surface. a), green line shows data distribution before applying time delay correction and blue circles indicate data after correction. b), the second image shows the effect after fitting with Equation 5.11 above with fitting parameters -1.201±0.0016, -0.125±0.0041, 0.076±0.00057.

Here the fitting parameters *P[1]*, *P[0],* and *P[2]* corresponds to contact potential difference, phase offset, and capacitance second derivative [($\frac{Q}{2K}\frac{d^2C}{d^2Z}$)] respectively. Now we are in position to fit a smaller region over the same line. For instance, if we start with point X_0 then we need to select an array for data - nside (number of data points at the left) and +nside (number of data points at right side) on other side of X_0 for fitting. A small value of nside improves spatial resolution but degrades the accuracy of the fit due to the smaller number of data points include. Figure 5.19 shows an image over 80 pixels of data where we used nside = 40 and frequency 30 Hz in same gold surface and for same row.

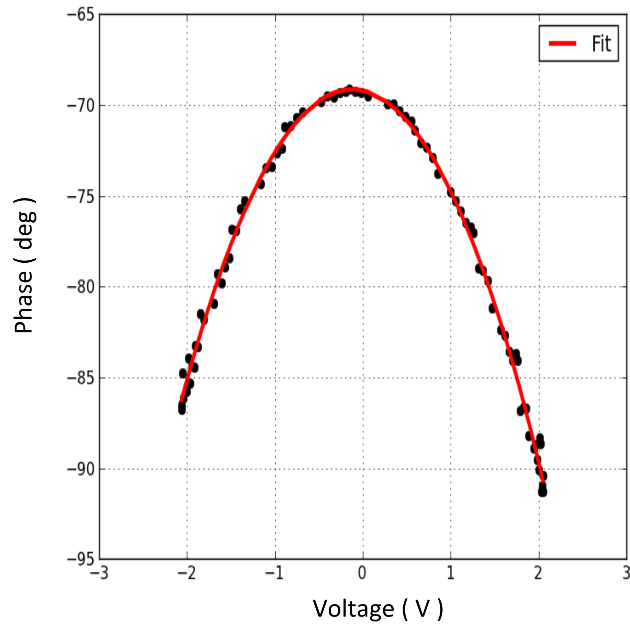


Figure 5.19: Phase-voltage calibration when nside = 40, f = 30 Hz, tip bias= 2 V, tip height = 20 nm, and scan size = 1µm.

We found that a time delay of 0.75 to 0.9 msec gave the best fitted parabola. We also found that an applied frequency of 30 to 40 Hz that gives synchronization useful number of cycles per scan line. Figure 5.20 shows the phase-voltage curve fitting for different values of nside. This procedure is then repeated, incrementing X_0 by one step.

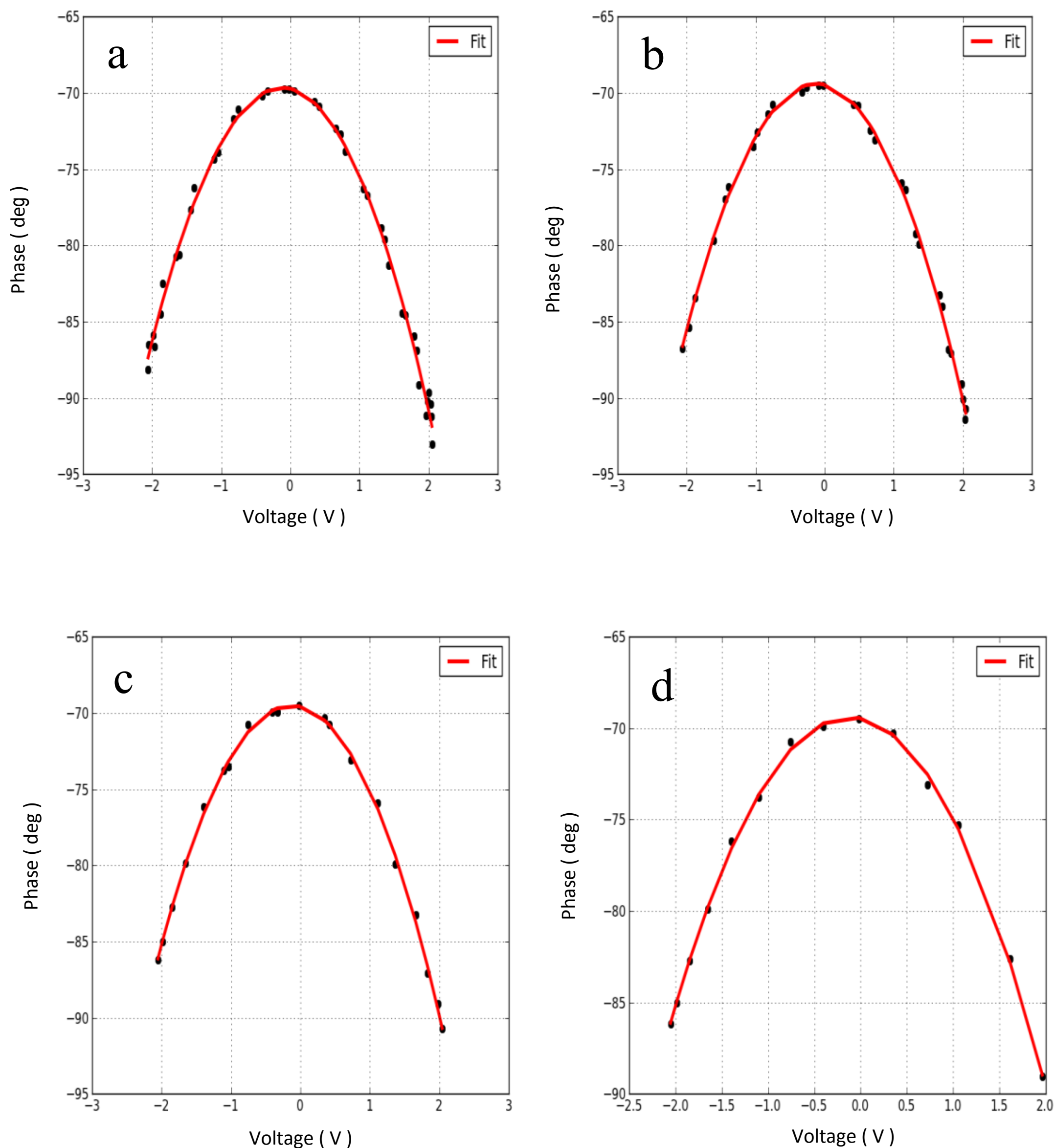
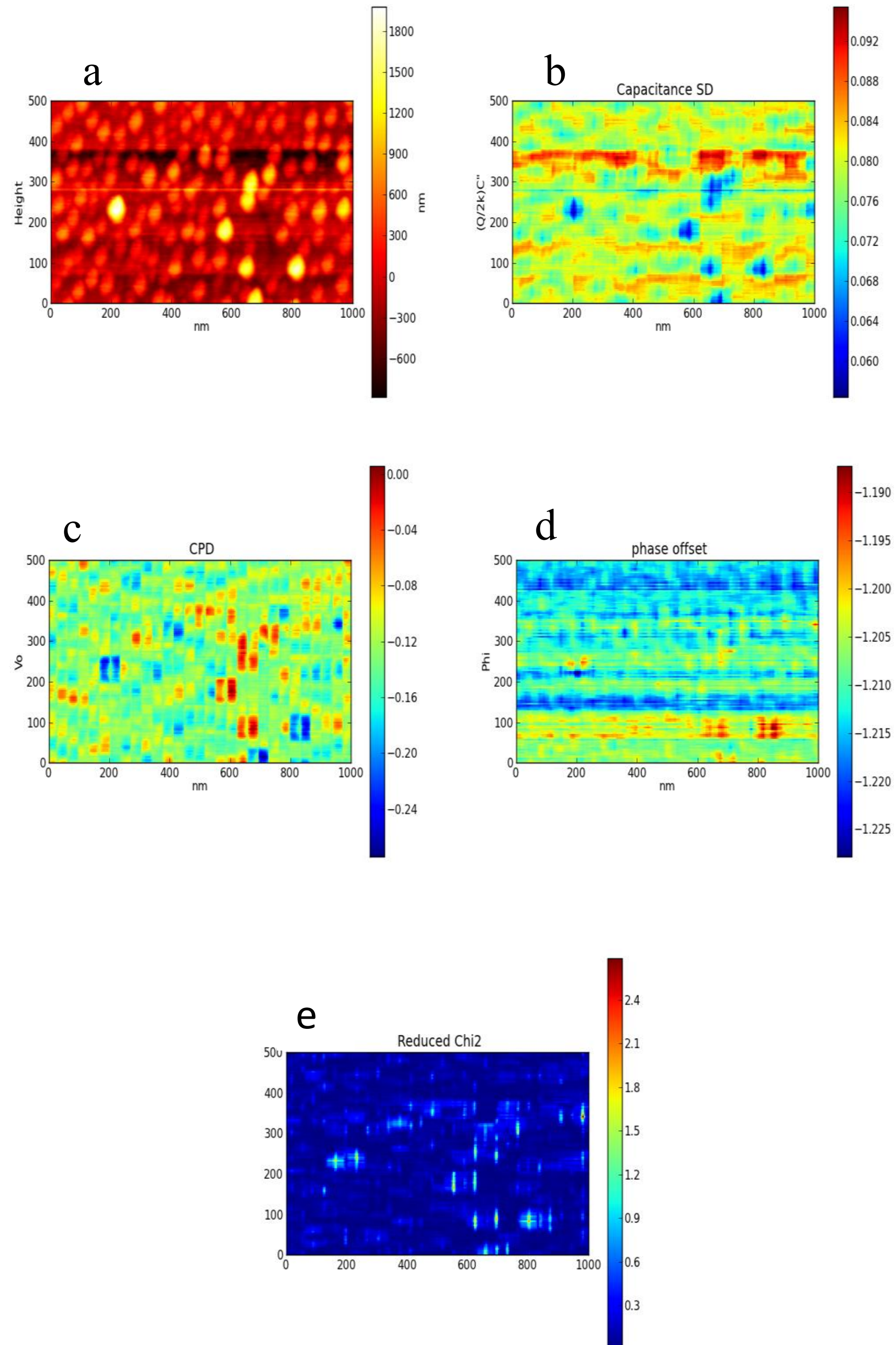


Figure 5.20: Phase-voltage calibration curves for different values of nside. a) nside = 20, b) nside = 15, c) nside= 10, and d), nside =7. All images for gold Au(111)/mica, tip bias = 2 V, tip height = 20 nm, and f = 30 Hz.

Thus we need a **PYTHON** loop over the whole row line transferring the parabola from one pixel to the next adjacent one ending at the last point in the same row. Moreover, the 2D images will be formed after a creation of row converting loops after finishing each specified row. The fitting of parabolas in each step and least_sq minimization were performed automatically by **PYTHON** ***curve_fit*** function through the scipy library.

We try to apply the new software to some test surfaces starting with:

5.5.1 Au(111)/mica Figure 5.21 shows the 2D images of potential, second derivative of capacitance, and phase offset obtained by using the new software. The sample had been in air for some time so we see some gold islands distributed over the sample.



We tried to check the result of fitting across the sample. The outcome depicts that even at small shining blue dots (redch2 is roughly between 0.8 to 1.1) the fitting is still good and representing parabolic shape within predicted sample contact potential difference (CPD).

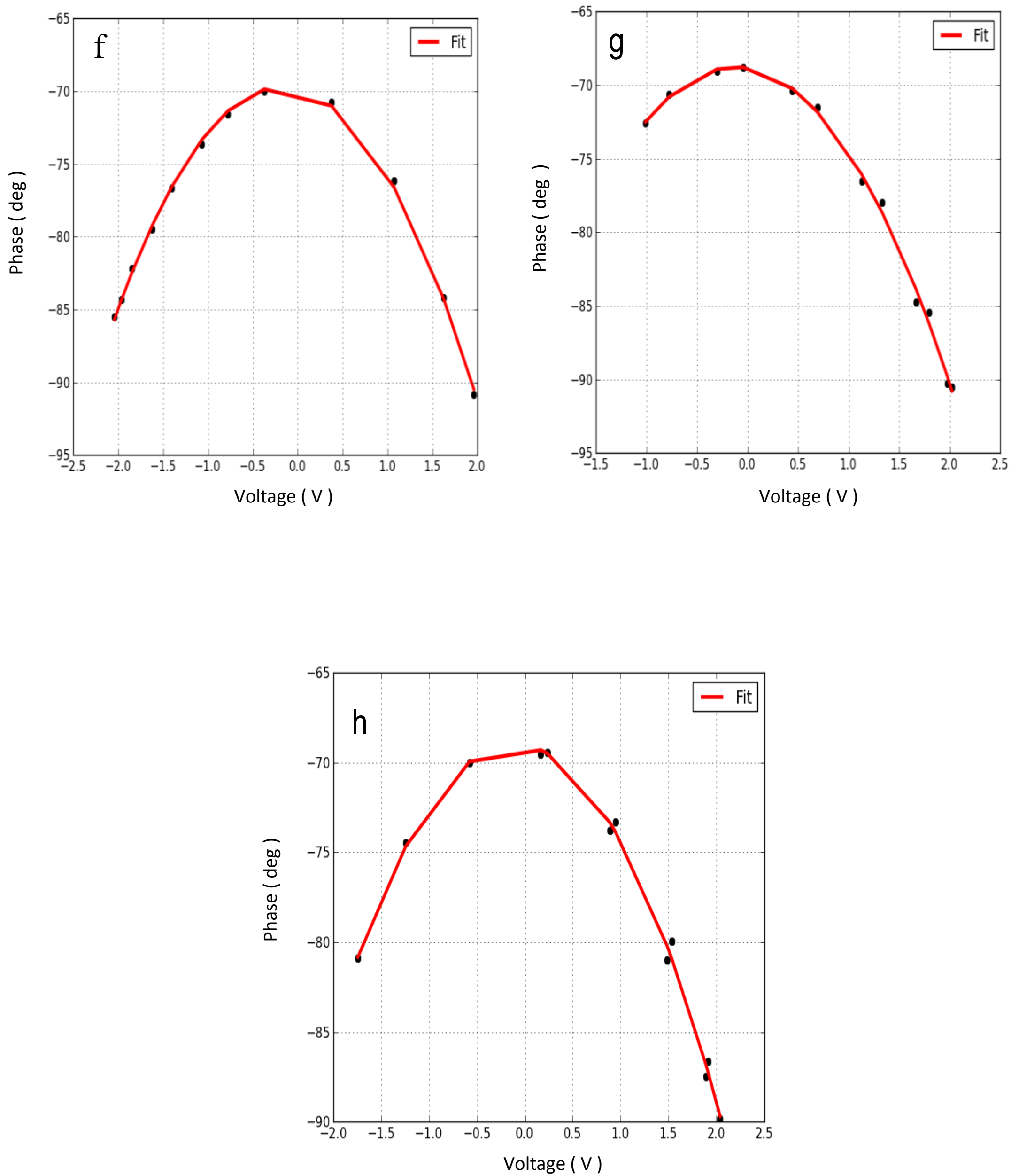


Figure 5.21: a) topography, b) the second derivative of capacitance, c) 2D images of CPD, d) phase offset e) reduced chi square, f) fitting with redch2 = 0.15, g) redch2= 0.63, h) redch2= 1.1. The images taken for d = 20 nm, V_t (tip bias) = 2V, f = 30 Hz, τ = 0.73 ms, nside = 6.

5.5.2 MDMO-PPV/PCBM

The investigated sample consist of MDMO-PPV/PCBM with blend ratio 1:4 dissolved in Chlorobenzene with continues stirring for 20min at 50 C^{o} to make a solution of concentration 1.25wt%.

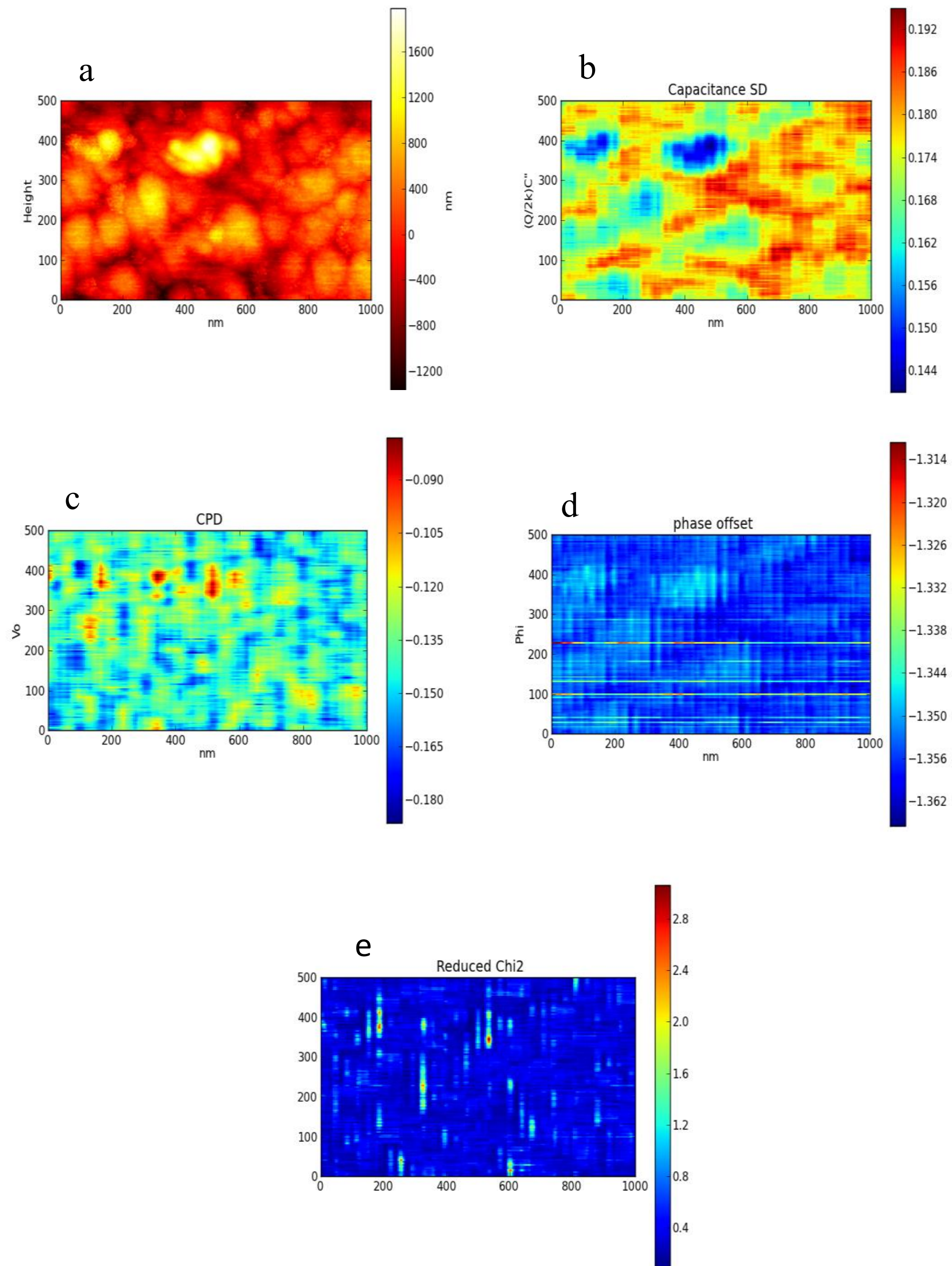


Figure 5.22: a) surface topography, b) second derivative of capacitance, c) 2D images of CP, d) phase offset e) redchi2. The image taken for d = 20 nm, f = 30 Hz.

The solution was spin coated on a clean surface of ITO-glass (1500 rpm) after washing it with isopropanol and acetone then drying it with flushing N_2. This ensured a film thickness about 50-100 nm [220]. Figure 5.22 depicts the 2D images of height, second derivative of capacitance, and CPD.

The maps of topography and the second derivative of the capacitance gradient show some correlation in which the latter parameter has its highest values where the topography is at its lowest. This may be a simple geometric effect rather than reflecting the intrinsic property of the material. The contact potential difference does not show direct correlation with the topography. One aspect is visually apparent: the maps of fitted parameters show vertical lines that indicate systematic effects that occur in fit to each row data.

5.6 Further improvements of EFM data

In order to tackle the above problem and stop the appearance of vertical lines in 2D images, we tried to improve our EFM data by varying the phase of the AC bias applied to the tip, as can be seen in Figure 5.23 below which is in contrast with Figure 5.15b.

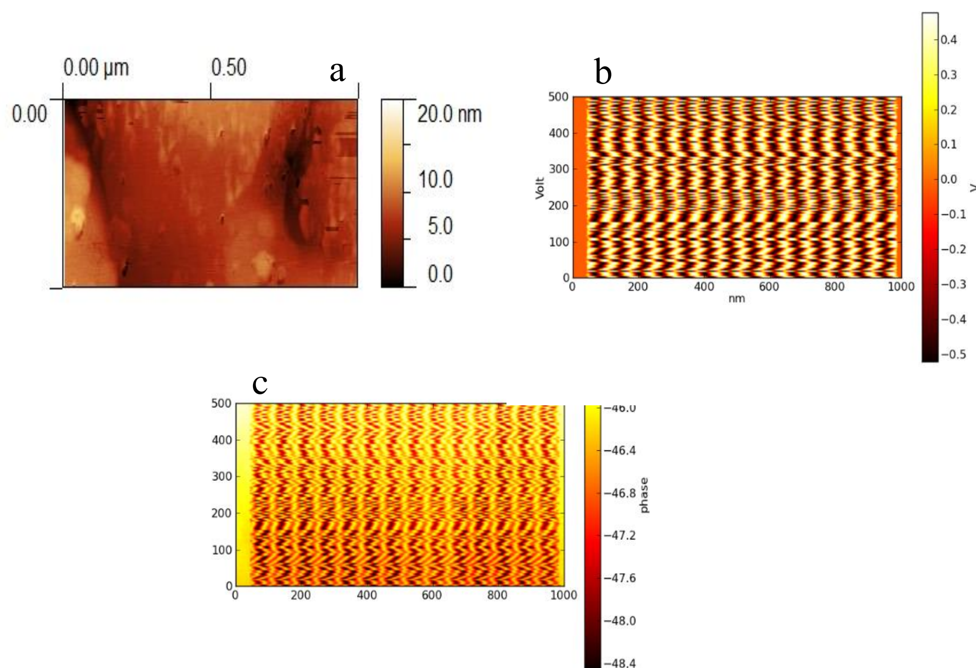


Figure 5.23: a) Surface topography of Au(111)/mica, b) random AC applied bias to the tip in contrast with Figure 5.15b, c) the resulting phase shift.

Then the resulting 2D images of above gold surface will be:

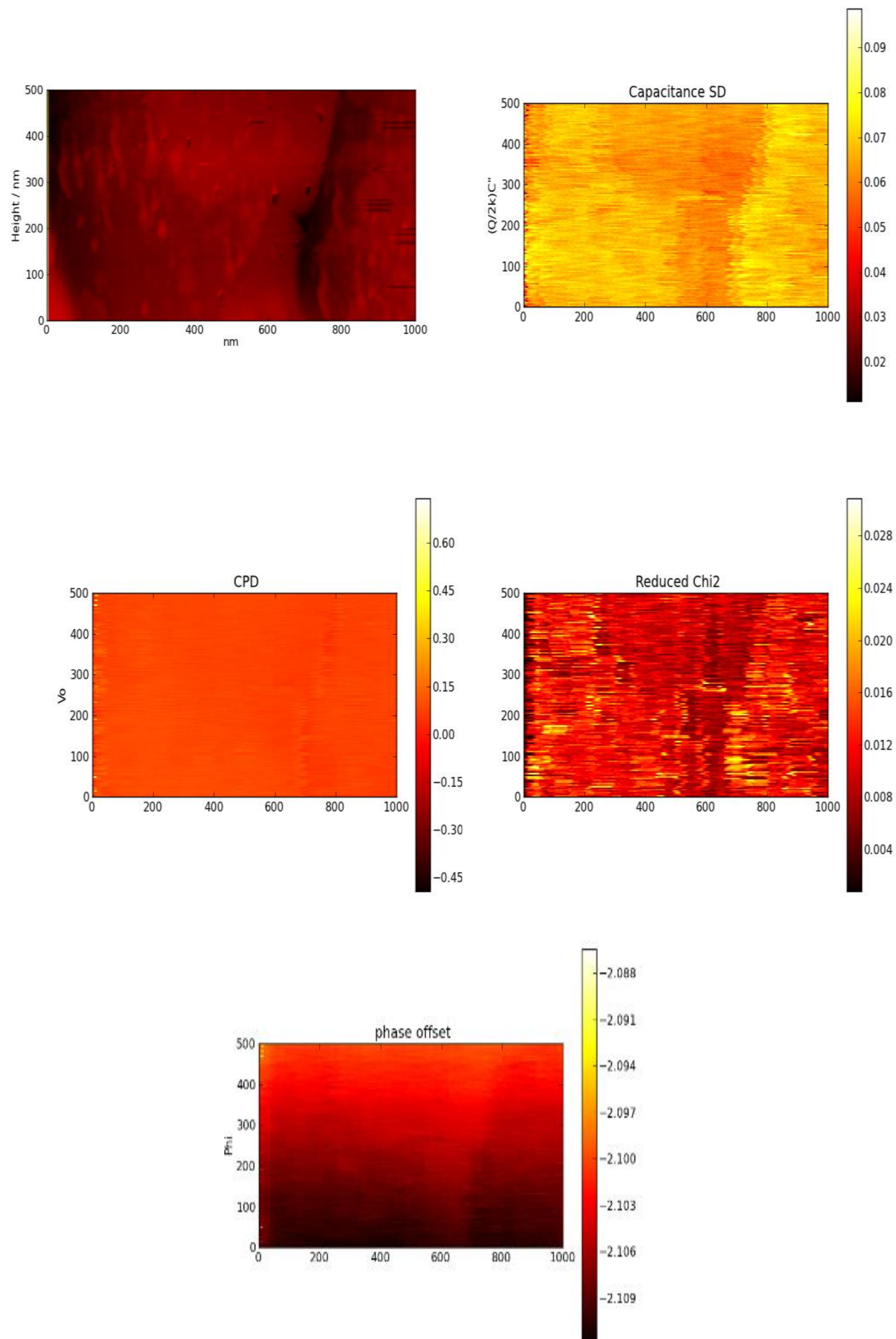


Figure 5.24: 2D images of Au(111)/ mica surface topography, second derivative of capacitance, CPD, the phase offset and related reduced chi square at tip bias 0.5 V, $f = 30$ Hz, $d = 20$ nm.

This type of signal also applied to the other surfaces such as graphite and the obtained result was good as well.

5.7 Organizing the new experiment set up for transistor measurements

The new set up has the same physical principle with one main difference which is introduction of the *LabJack U3- HV - USB Multifunction data acquisition and control device* Figure 5.25.

Following the above initial measurements on test materials, we adopted the experimental setup to investigate transistor devices as in Figure 5.26. LabJack has a flexible inputs which can be configured for any mix of analogue inputs, and digital inputs/outputs and can be controlled by software in various programming languages including python. More information about the LabJack data acquisition can be found at http://www.audon.co.uk/usb_multi/lju3hv.html.

The controlling program is designed to detect a linear trigger from Vecco AFM (as before) and perform various actions:

1. Apply zero bias in trace and retrace topography scans.

2. In lift mode, apply mixed (V_{ac} + V_{dc}) bias to the tip during either trace or retrace scan.

3- Has the capability to vary the voltage applied to the drain or gate.

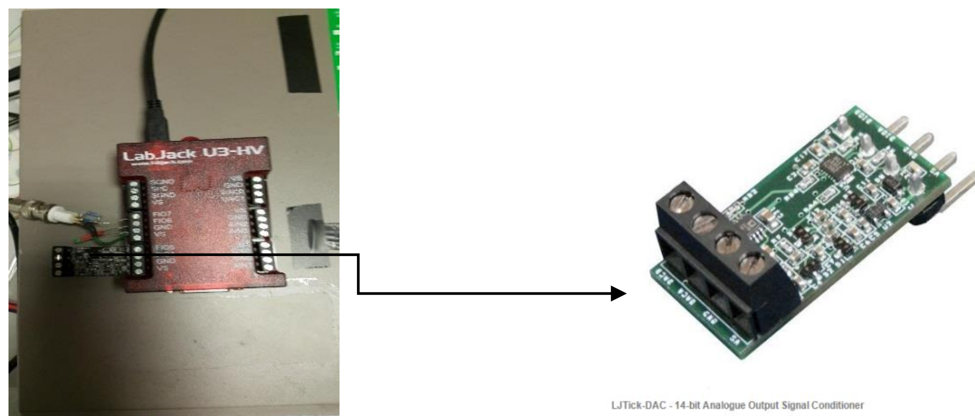
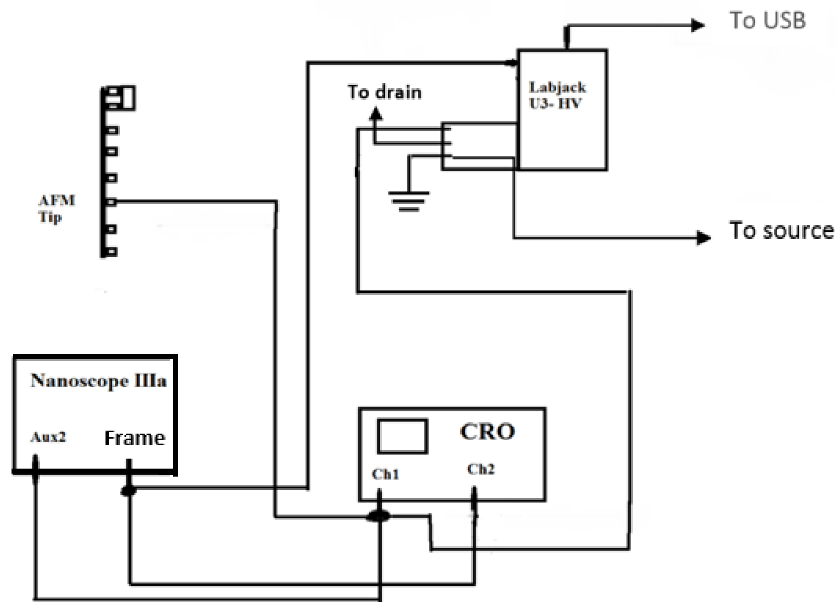


Figure 5.25: LabJack U3- HV - USB Multifunction data acquisition and control device



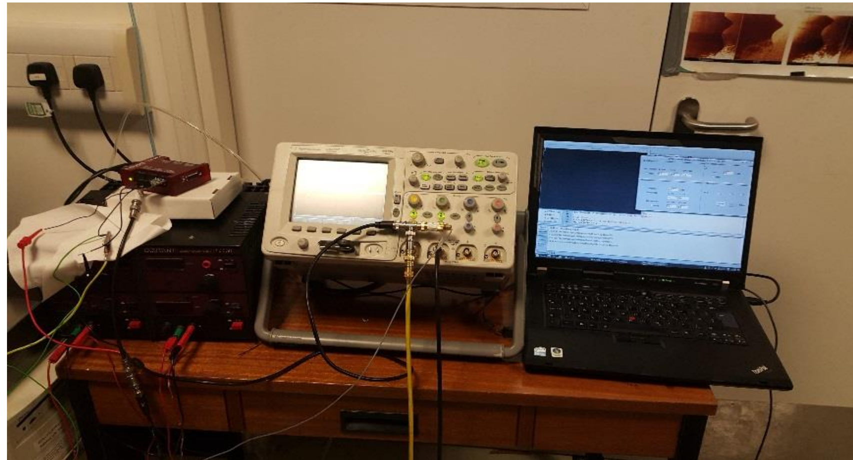


Figure 5.26: EFM experiment set up with controlling program

After an initial period to overcome the difficulties that appeared during our study, we applied this new method to a working transistor under bias. The study of potential distribution on the working device with the new software is more difficult than using it on a normal material surface because of: 1- metallic surface (electrodes) and semiconductor channel, 2- bias on drain and gate, 3- inhomogeneous charge distribution

in channel and pinch off region in vicinity of drain, 4- Al diffusion close to the electrodes.

In all experiments we applied bias to the tip and source electrode was kept grounded during EFM experiments. Figure 5.27 shows the potential profiles analysis of the W1000L30D device under various drain bias values. The figure clearly shows:

1- Clear evidence of the Al diffusion region and sharp drop at drain contact edge.
2- A drop close to the middle of the channel (roughly at 23 µm) more obvious at high drain bias, which also appears in the 2D image for 4V drain voltage as a (dark blue) region. The origin of this not known

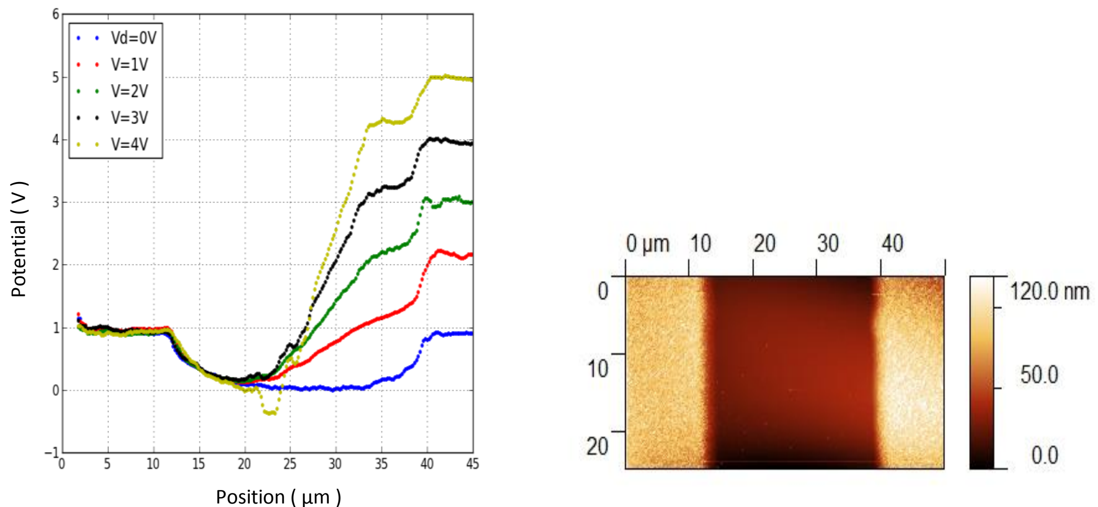


Figure 5.27: Potential line profiles at V_d = 0, 1, 2, 3, 4V and V_g = 0 V with grounded source (left image). The second figure in the right is a topography image which reveal the position of two electrodes and channel, Aspect ratio is 2/1:

It is clear from the above profiles picture that the phase mode is more sensitive to the detail of sample compare to the surface potential obtained in Kelvin probe Figure 5.31. The corresponding 2D image of above profiles is shown in Figure 5.28 below.

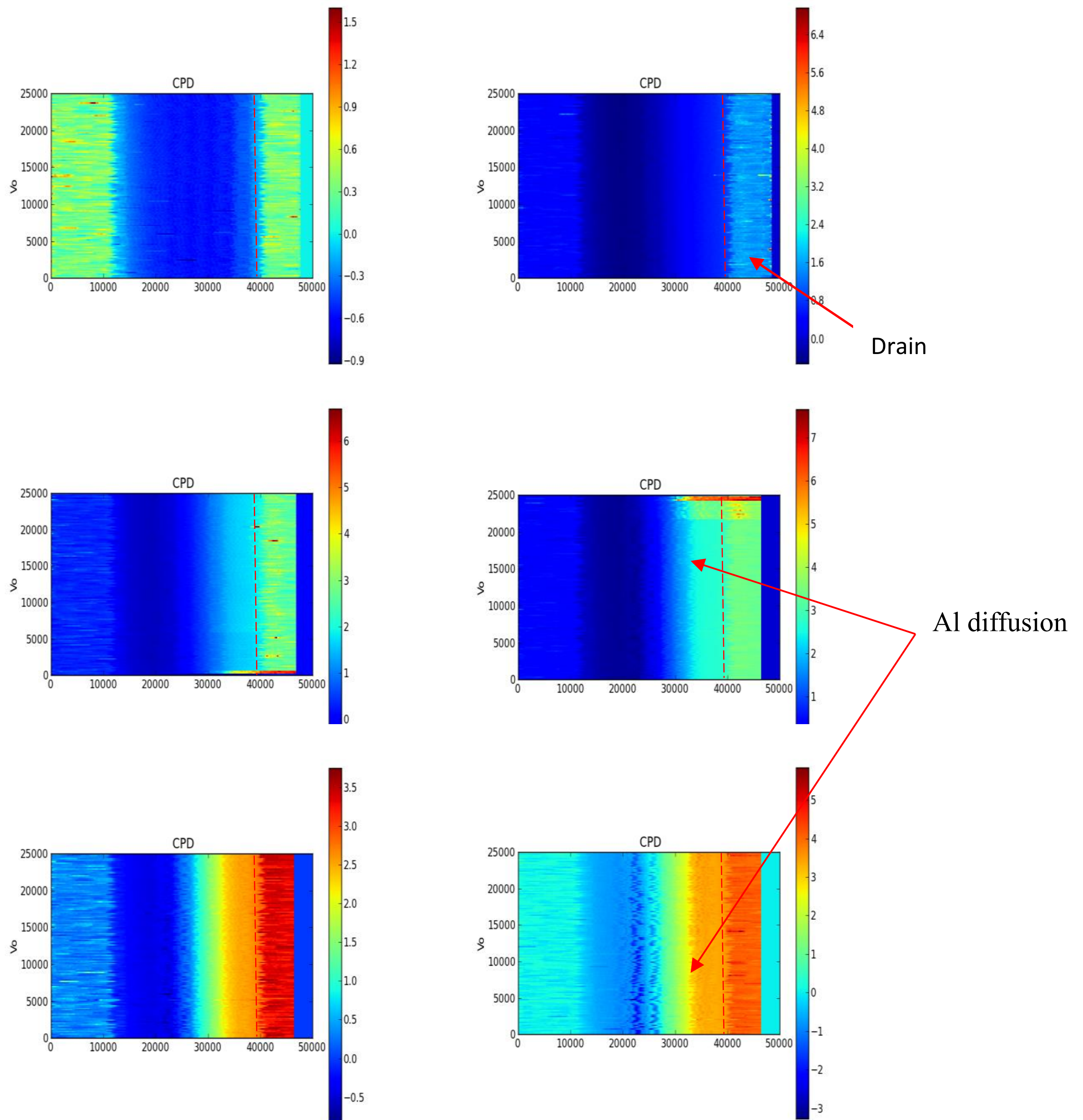


Figure 5.28: 2D images for W1000L30D corresponding to the above profiles for V_d = 0, 1, 2, 3, 4, 5 V. V_g = 0 V, nside = 9, delay = 0.73 msec . The dash vertical line represent drain electrode position.

The above 2D images not only shows the contact position and diffusion edge but also the details of the channel region which we didn't notice that in SKPM analysis. Moreover, the images confirm that there is no any voids or cracks in the region between source and drain. However, the potential profiles in the region close to the drain electrode at higher drain bias shows some changes and specifically at the edge of Al diffusion region and in the middle of channel. The red arrow refer to the edge of Al diffusion and the dashed line is the drain contact position. As drain bias is increased above 4-5V, the edge of Al diffusion region seems to shift towards the drain electrode, we don't understand this apparent effect currently.

During EFM-phase study and the results of different EFM experiments, we noticed that the time delay correction when the device working at depletion region or at high drain bias (from 5V and above) is challenging to determine- it seems to vary with position along the channel. This may reflect difference in the charging time of the channel material under the tip. This non uniformity of charge delivery is increased as we approach to the drain electrode. Therefore, we tried to perform some extra studies to see the impact of delay on the appeared potential profiles especially at Al diffusion region and drain contact at high voltage. For this purpose we changed τ from 0.5 to 2 msec and at each case we plot corresponding line profiles for both linear and saturation region.

5.7.1 Study 1: At low drain bias (linear region).

In the linear region of transistor the charge distribution is uniform across the channel between source and drain. Figure 5.29 shows the potential profiles for drain bias 1 V for various time delays values. It is clear that the exact value of τ has limited effect on the voltage profiles close to the middle of the channel, specifically in the region between the two dashed lines.

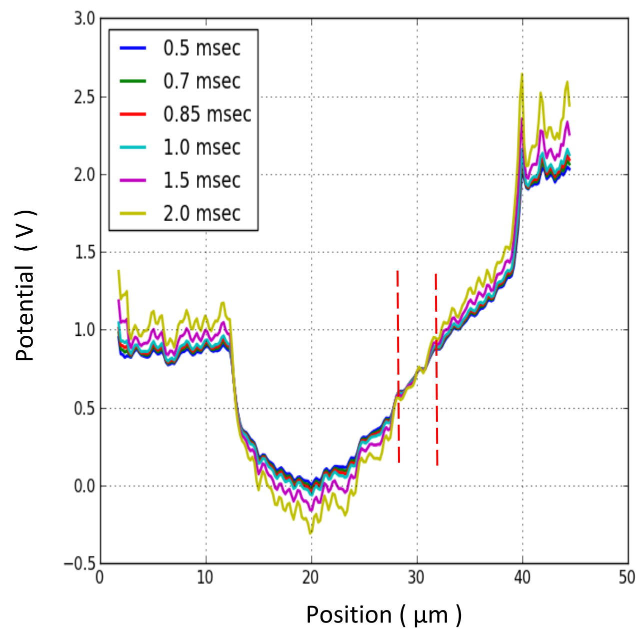


Figure 5.29: Effects of time delay changes on potential profile for 1 V drain bias.

5.7.2 Study 2: At high drain bias (saturation region)

At higher drain bias, the effect of τ is roughly the same at middle of channel as previous case but at the right of this region its effect become predominant as an abrupt peak develops at Al diffusion edge for longer time constants. However, in the case of SKPM this region was totally smooth. Figure 5.30 shows the effect of τ change on the potential profile at a drain bias 5 V. To sum up, the effect of the assumed time delay becomes more marked as the channel becomes depleted.

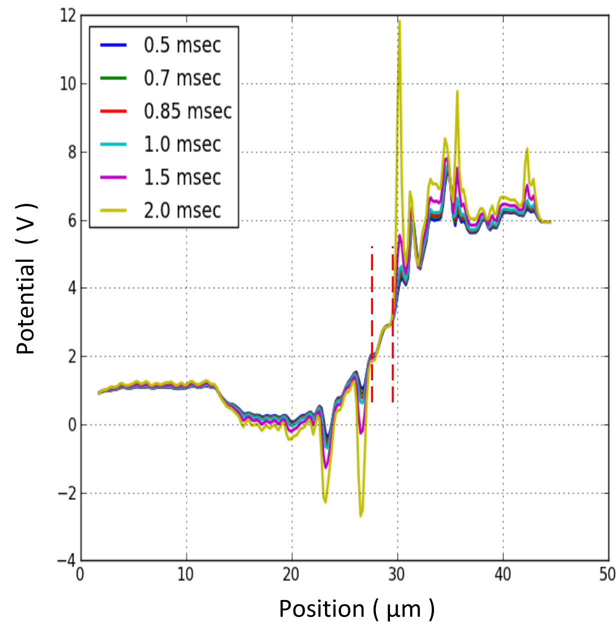


Figure 5.30: Effect time delay on potential profile for W1000L30D operating device under drain bias V_d =5 V and V_g = 0 V.

Hence, the study of time delay correction and effect of charge or lack of charge in device channel is crucial in investigation of actual potential profiles in this experimental method. To do this we tried to get a suitable time constant which gives the best fitting for each point across one row or line which means correction of τ for each pixel. The result is shown in Figure 5.31 below for W1000L30D device and at drain bias 6 V. The outcome reveals that the proper time constant is of the order of 0.5 to 1 msec when we are away from the drain electrode and the Al diffuasion region. As we approach to the drain terminal, the optimum value of τ changes more rapidly. This qualitative behaviour indicates that the time delay relates to the charging time of the region under the tip. It may point to a method of measuring the local charging time, but this is beyond the current scope of this thesis.

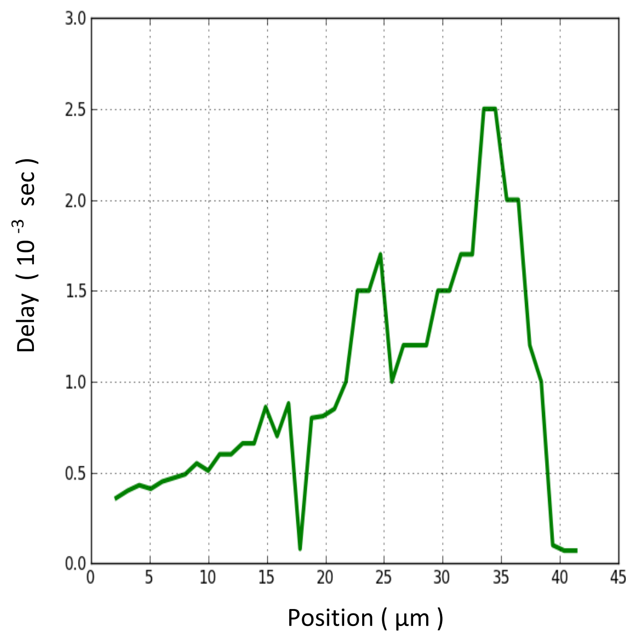


Figure 5.31: The optimal time delay needed for fitting of parabola at drain bias 6 V, as judged by the fit giving the lowest value of chi-square.

5.8 Comparison between SKPM and EFM (new software) images.

As we mentioned in the previous chapter that the SKPM is a technique which measure the electric potential of the surface by adjusting the tip bias to minimize the electrostatic force between the tip and surface. SKPM has worse spatial resolution due to long range force range contributions from tip apex, tip cone, and cantilever [221, 222]. Furthermore, as the Kelvin probe depends on the cancelling out of electrostatic force and nullifying the oscillation by adjusting tip voltage. Consequently, it is essential to notice that in case of ambient condition, surface contamination, charge trapping, oxidation, and existence of water film between tip and sample can lead to modification of Kelvin probe signal. Thus the measured surface potential causes difficulties in interpretation of resulting data in term of real work function [223, 224]. However, EFM- phase mode is sensitive to the electrostatic force gradient rather than the force itself and consequently its spatial resolution is better. The relevant force gradient is much shorter-ranged in EFM-phase, arising mainly from the tip apex.

Two dimensional images and surface profiles are ideal for transistor measurements because it identifies features causing lack of device performance such as contact resistance, trapped charge, voids or cracks in the channel, shift of potential profiles because of the contact particles diffusion. Likewise, 2D images of potential can provide a valuable feedback to the design team, by supplying needed data to understand the effect of the device structure. Figure 5.32 shows a comparison of potential profiles in SKPM(solid line) and EFM-phase (dotted line), obtained by using the software developed here, in the bottom gate top contact W1000L30D transistor. Both profiles confirm, the exact position of source and drain electrode edges, the Al diffusion region close to the drain electrode, and the change in the voltage profile linear to super-linear with as the drain bias is increased. However, the abrupt and sharp drop at drain contact edge is much clearer in the EFM-phase technique as a result of its superior spatial resolution. SKPM measures a smaller drop, which is also more rounded, because of the larger interaction area between tip and surface.

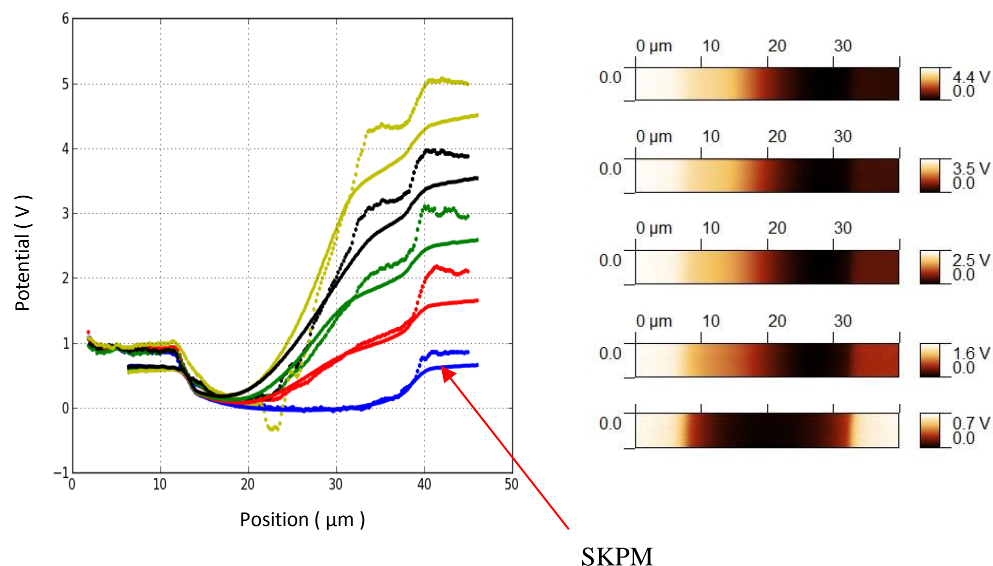


Figure 5.32: Potential profiles comparison in SKPM (solid lines) and EFM-phase mode (dotted lines) for V_g = 0 V and V_d = 0, 1, 2, 3, 4 V. SKPM and EFM profiles confirm Al diffusion region close to the drain which appeared as a flat region. The Profiles reveal the fast drop at contacts and the effect of weight averaging in SKPM. Right figure shows SKPM 2D captured potentials images for V_d = 0, 1, 2, 3, and 4 V which corresponding to left line profiles. The drain is at left side which converted to right in profile image.

Hence, both EFM-phase and KPM are attractive method of measuring sample surface potential. Both involve a two pass technique, with topography measured in a first scan, followed by a second scan with the tip lifted a constant distance above the sample.

In EFM –phase, the measured signal is the phase of the tip oscillation relative to the driving signal, whereas in SKPM the mechanical oscillation of cantilever is turn off. SKPM uses a feedback system to adjust dc bias to minimize cantilever oscillation and nullifies the force but in phase mode there is no feedback The relationship between the measured phase difference and the applied tip potential is recorded and the known relationship between them employed for fitting, after correction for instrument-related or sample-related time delay using a low-pass filter function consistent with electrostatic charging

5.9 Conclusions

We have developed a method for determining simultaneously the local surface potential and the local second derivative of capacitance for a thin film based on lift mode EFM-phase scan. However, when EFM raw data was extracted we noticed a mismatch or delay between sensing and applied bias. This mismatch reflect itself as a double parabola in phase-voltage curve. Furthermore, the mismatch is shown to be strongly dependent on the applied signal frequency. Importantly, it was found that the time delay could be corrected for by applying an inverse low-pass filter to the measured tip voltage and new software was developed to correct for this and display the corrected voltage profiles. Information about scan size, aspect ratio, and applied signal frequency is automatically extracted. The corrected data are then fitted by the predicted phase-voltage parabola.

The new software is applied to some samples to establish 2D images of contact potential difference and second derivative of capacitor of surfaces. These surfaces include Au(111)/mica, graphite, and organic thin films. Following these tests, the approach was applied to biased transistor devices. According to our experimental results we can state:

1. The time delay, and resulting parabola shifts, are not dependent on the shape of the applied waveform, or tip height.

2. We can adopt a constant time delay around 0.7 – 1.0 msec for flat and equipotential samples like Au(111)/mica and roughly graphite.

3- The EFM-phase approach, combined with the new software, on working TFT device give good consistency with SKPM results, but exhibit improved spatial resolution.
4- For high drain bias, greater than around 5V, the depletion region become more extended along the transistor channel and the time delay becomes inhomogeneous, probably the result of slower electrostatic charging from the electrodes. This effects demand further study.

Chapter Six

Conclusions and Potential Future work

In the thesis, we have investigated the structural and electrical properties of thin film transistors using Scanning Probe Techniques. In chapter three we discussed strategies for controlling the morphology and crystalline microstructure of soluble (TIPS-PEN) as a small molecule OS of interest in fabrication of OFET. In chapter four, we reported the electrical properties of In_2O_3 metal oxide semiconductor TFTs. In chapter five, we developed a new approach to Electrostatic Force Microscopy, as applied to the potential profile within an operating transistor. This approach has been filed for a patent. We summarise here the main findings for each of these areas and give some indication of possible directions for future work.

Control of morphology in TIPS-PEN thin films (chapter 3)

The performance of an organic field effect transistor is strongly influenced by the active layer properties. Varying the detailed composition in solution –processing of OSM, such as TIPS-PEN, can potentially give some control over the quality of the semiconductor layer for device applications. We have presented a systematic study of the growth and formation of TIPS-PEN films deposited from binary solvents of various compositions. Solvent mixtures with anisole:decane ratios (100/0 to 80/20 (v/v) or 100/0 to 85/15 wt-%) were used and the resulting solutions deposited onto SiO_2 substrate. The effect of the TIPS-PEN- aPS ratio up to 20 wt-% for drop-cast thin film was similarly investigated. The effect of the solvent mixture as a function of volume ratio for drop-cast TIPS-PEN thin film, and TIPS-PEN / aPS thin films were monitored by optical microscope, AFM and OFET measurements.

1- It was found that addition of up to 20% decane has no significant effects on micro-scale crystal pattern monitored by OM. We observed that the TIPS-PEN crystals do not cover the entire surface, regardless of the blend ratio of anisole and decane. The crystals appeared as feather- or spike-like shapes of width ranges from 50 μm to several hundreds of microns, which leave void regions between these crystals several hundreds of microns wide.

2- AFM monitored films of different anisole:decane blend composition showed a dramatic influence of decane concentration on the surface properties such as growth mode, terrace roughness, and molecular ordering. For TIPS-PEN films dried from pure anisole, AFM revealed high film roughness, featureless and grainy structure, with no clear evidence of molecular ordering. In contrast, addition of the high boiling point solvent decane induces a drastic changes in surface roughness and molecular ordering. TIPS-PEN deposited film from decane composition of 5, 9, and 10 % (v/v) on SiO_2 showed wavy, well defined terraces edge of height around 1.6nm, low values of surface roughness on terraces. However, further increase of decane ratio in the blend causes rougher film and less ordering.

3- Some smaller step heights of around 1.4 nm were also observed, which may correspond to a tilted molecular orientation.

4- The occurrence of the small grains at the step edges may indicate that these comprise impurities expelled by the growing step front.

5- The average mobility of organic field effect transistor (OFET) devices cast from different blend ratios of anisole:decane depicted values around 0.013 $cm^2V^{-1}s^{-1}$ up to 85:15 of anisole:decane. However, with the addition of 20% decane, average device performance suddenly drops to 0.004 $cm^2V^{-1}s^{-1}$. These data suggest that addition of low concentrations of decane may not have significant impact on the overall OFET performance.

6- OM images of drop cast TIPS-PEN / aPS blends crystals grown on both SiO_2 and poly(vinyl phenol) PVP surfaces showed that increasing polystyrene content

increases alignment of crystal plates and improves surface coverage , with almost the entire surface covered at a 85:15 wt-% TIPS-PEN / aPS ratio.

7- AFM images of TIPS-PEN / aPS on SiO_2 also revealed similar stepped surfaces of the flat terraces of heights of 1.6 nm with different aPS compositions. However, two differences are observed: the step edges are much straighter than those for pure TIPS-PEN and larger grains, of the order of 125 nm or more across, are observed on the terraces between steps. The large grains observed on terraces are likely to be rich in aPS, as deduced from the increased contrast in the phase mode plots.
8- AFM images of TIPS-PEN / aPS on PVP showed straight step edges over several areas imaged for 10 wt% aPS whereas they are more wavy at other compositions. A noticeable difference for the PVP-covered surfaces is the absence of grains on the terraces or at step edges for aPS compositions up to 15 wt-% .
9- The average mobility of OFET devices cast from various composition of TIPS-PEN / aPS on PVP shows values around 0.14 to 0.17 $cm^2V^{-1}s^{-1}$ which are roughly 10 times greater than those at same blends composition on SiO_2. This suggests that PVP treatment of SiO_2 surface has a beneficial influence on mobility.

The Local electrical properties of In_2O_3 thin film transistors (chapter 4)

Indium oxide is a high mobility n-type oxide semiconductor of band gap 3.6 eV at room temperature. It also has high optical transmittance in the visible region and its high electrical performance makes it a superior candidate for the oxide TFT active layer. The aim of this chapter was to investigate the local electrical characteristics of the indium oxide channel in an operating TFT with high spatial resolution. More specifically, we aimed to understand its stability (measured on devices without encapsulation), surface potential profile of the operating device under drain and gate bias, and to probe the interface between the electrodes and the channel. Two layer thicknesses were investigated: a very thin (~ 4nm thickness) layer prepared by a single

spin-casting process and a 7-8 nm thick layer, prepared by two consecutive spin-coating processes. (The films were prepared in Prof Thomas Anthopoulos' group at Imperial College.)

1- The single spin coated devices (~ 4nm thickness) demonstrated field effect mobility around 0.2 $cm^2V^{-1}s^{-1}$ whereas the mobility for double spin (7- 8nm) increased to about 1 $cm^2V^{-1}s^{-1}$. Generally, we found that, as the device thickness (single to double) is increased, the mobility increase, the threshold voltage is shifted towards the negative direction, off-drain current is increased, and on-drain current is less pronounced.

2- The effect of bias-stress measurements on indium based TFT were implemented to check the device stability under prolonged gate bias up to beyond 10^4 sec. A positive gate bias stress showed displacements of transfer curves in the positive direction, the device mobility remain unchanged during the time of gate bias stress. The stressed devices spontaneously recovered and returned to their original characteristics after a certain period of relaxation at room temperature.

3- The time dependence of the threshold voltage shift is described well by a stretched-exponential model, and charge trapping is believed to be the major cause of device instability and the threshold voltage shifts in these In_2O_3 devices.

4- Charge trapping is a gradual process which starts with a quick shift of threshold voltage, suggesting that the charge is initially trapped instantaneously into readily available states. These states are limited in number and subsequent trapping leads to more gradual, shifts of V_{th} with stressing time till it reaches saturation.

5- EFM-SKPM mode, was used to detect and image the trapped charges along the transistor channel prior to and after switching off the positive gate bias. EFM captured images clearly showed that the charges trapped across the channel when it is subjected to the prolonged positive bias. The trapped charge distribution appeared as localised deviations in surface potential in the channel immediately after switching off the gate bias.

6- The potential profiles of operating In_2O_3 TFT were also studied. We used SKPM to map 2D surface potential in the channel region and between the source–drain electrodes with bias voltage. The obtained data revealed useful information for understanding the device operation, the related surface topography, with a view to designing higher performance device structure. In the linear region, indium oxide TFT revealed a linear increase in potential across the device channel whereas, a super-linear characteristics of potential profiles were observed for high drain biases. We noticed a rapid change of electric field at the edge of the drain electrode as the drain bias enhanced. A small drop at the contacts edge was spotted which confirms a small contact resistance of the devices. A uniform film was observed between the two electrodes that covered the entire region between two electrodes without any voids or cracks.

7- An interesting feature of the potential profiles in our In_2O_3 TFT is detection of a flat region close to the drain electrode. This flat region is attributed to the Al contact diffusion into the device channel. Our experimental results also confirmed with modelling of potential profiles and simulation results. The device simulation consequences affirmed the same flat region, a threshold voltage close to experimentally determined values, simulated surface potential profiles were consistent with measured data for different gate bias.

8- AFM on biased samples can be used to detect the contact diffusion region. The AFM topography scans have revealed a flat surface of the In_2O_3 channel between the source and drain electrodes. The position of the diffusion region and the region of high electric field between the diffusion and the channel can be determined only when measuring electrostatic contribution to the measured morphology profiles on the biased TFT The tip height changes due to the electrostatic interaction with the regions of high electric field at the surface of a biased sample can be detected in the apparent morphology.

9- Both the AFM and the SKPM data are in a good agreement regarding the positions of the source, and drain electrodes and the extent of the diffusion regions.

New approach to Electrostatic Force Microscopy (chapter 5)

In this chapter we discussed the theory and fundamental principles of electrostatic force microscopy, specifically a variant developed at Cardiff originally named EFM-phase mode. It depends on the known relationship between the measured phase difference between the driving force applied to the tip and the response of the cantilever. We have explored a new method for determining simultaneously the local surface potential and the local second derivative of capacitance for a thin film based on lift mode EFM- phase scan. During our experiments we found that the extracted EFM raw data revealed a mismatch or delay between the measured and applied bias. We investigated the effect of tip height, tip bias, type of applied signal, scan size, and signal frequency to understand the cause of the time delay. We found that the delay could be described by a inverse filter function. The corrected data are agreed well with phase-voltage formula so the data are fitted to extract the essential information. This was implemented in a new software, which was tested on surfaces like Au(111)/mica, graphite, and MDMO-PPV/PCBM. Following these test samples, the procedure was applied to working biased field effect transistor devices. Finally, we compared the EFM-phase results with SKPM, as used in chapter 4, and found good consistency between the two techniques.

Recommendation for future works

We have used AFM, SKPM, and EFM- phase to enhance our understanding of TFT devices. As organic and metal oxide TFT technologies are both likely to be a part of future electronics, further investigation is suggested beyond the scope of this thesis in the following areas.

1- Blend formulation for TIPS-PEN is a non-trivial and difficult area in which several factors are influential, including: deposition technique, solvent mixture ratio, solute concentration, blend compositions. EFM-SKPM mode and EFM-phase to give higher spatial resolution, could be used together with metal electrodes to probe which part of TIPS-PEN/aPS film is conductive and which is not. Applying this method on the whole devices one can improve the device performance by suitable blend ratio and better formulations. The approach developed here could be applied for several material systems in future work.

2- The detection of metal diffusion from electrodes has wide applicability as confirmed in our study using SKPM, EFM-phase mode, and with the device simulation. This effect demands further study to probe the effect of local Ohmic heating in resistive regions. Furthermore, this could be extended to study contact diffusion as a function of device length and active layer thickness and its effect on device performance.

3- Our new EFM-phase approach may well have useful applications in monitoring operating devices. The simultaneous measurement of surface potential and the second derivative of the capacitance is a new capability, which may well be sensitive to the local buildup of charge in a device.

References

1. Tans, S.J., M.H. Devoret, H. Dai, A. Thess, R.E. Smalley, L. Georliga, and C. Dekker, *Individual single-wall carbon nanotubes as quantum wires.* Nature 386 (6624), 474-477.(1997), 1997.

2. Fuhrer, M., B. Kim, T. Dürkop, and T. Brintlinger, *High-mobility nanotube transistor memory.* Nano Letters, 2002. **2**(7): p. 755-759.

3. Zheng, G., X.P. Gao, and C.M. Lieber, *Frequency domain detection of biomolecules using silicon nanowire biosensors.* Nano Letters, 2010. **10**(8): p. 3179-3183.

4. Xia, F., T. Mueller, Y.-m. Lin, A. Valdes-Garcia, and P. Avouris, *Ultrafast graphene photodetector.* Nature Nanotechnology, 2009. **4**(12): p. 839-843.

5. Binnig, G., C.F. Quate, and C. Gerber, *Atomic force microscope.* Physical Review Letters, 1986. **56**(9): p. 930.

6. Butt, H.J., B. Cappella, and M. Kappl, *Force measurements with the atomic force microscope: Technique, interpretation and applications.* Surface Science Reports, 2005. **59**(1): p. 1-152.

7. Bhushan, B., *Springer handbook of nanotechnology. 2004.* Springer-Verlag: Heidelbert. **99**: p. 145.

8. Meyer, G. and N.M. Amer, *Novel optical approach to atomic force microscopy.* Applied Physics Letters, 1988. **53**(12): p. 1045-1047.

9. Alexander, S., L. Hellemans, O. Marti, J. Schneir, V. Elings, P.K. Hansma, M. Longmire, and J. Gurley, *An atomic-resolution atomic-force microscope implemented using an optical lever.* Journal of Applied Physics, 1989. **65**(1): p. 164-167.

10. Nomura, K., H. Ohta, A. Takagi, T. Kamiya, M. Hirano, and H. Hosono, *Room-temperature fabrication of transparent flexible thin-film transistors using amorphous oxide semiconductors.* Nature, 2004. **432**(7016): p. 488-492.

11. Ha, T.J., *Photo-induced electrical instability in hydrogenated amorphous silicon based thin-film transistors and the effect of its phase transition.* Current Applied Physics, 2015. **15**(3): p. 330-334.

12. Madelung, O., *Technology and applications of amorphous silicon.* Springer, Berlin, 2000. **15**: p. 2934-2936.

13. Kelley, T.W., L.D. Boardman, T.D. Dunbar, D.V. Muyres, M.J. Pellerite, and T.P. Smith, *High-performance OTFTs using surface-modified alumina dielectrics.* The Journal of Physical Chemistry B, 2003. **107**(24): p. 5877-5881.

14. Gundlach, D.J., Y.Y. Lin, T.N. Jackson, S. Nelson, and D. Schlom, *Pentacene organic thin-film transistors-molecular ordering and mobility.* Electron Device Letters, IEEE, 1997. **18**(3): p. 87-89.

15. Joung, M.J., J.H. Ahn, S.Y. Kang, K.H. Baek, S.D. Ahn, L.M. Do, C. Kim, G.H. Kim, I.K. You, and S.M. Yoon, *New soluble pentacene precursors for the application of organic thin-film transistors.* BULLETIN-KOREAN CHEMICAL SOCIETY, 2003. **24**(12): p. 1862-1864.

16. Anthony, J.E., J.S. Brooks, D.L. Eaton, and S.R. Parkin, *Functionalized pentacene: improved electronic properties from control of solid-state order.* Journal of the American Chemical Society, 2001. **123**(38): p. 9482-9483.

17. Chen, J., C.K. Tee, M. Shtein, D.C. Martin, and J. Anthony, *Controlled solution deposition and systematic study of charge-transport anisotropy in single crystal and single-crystal textured TIPS pentacene thin films.* Organic Electronics, 2009. **10**(4): p. 696-703.

18. Kang, J., N. Shin, D.Y. Jang, V.M. Prabhu, and D.Y. Yoon, *Structure and properties of small molecule− polymer blend semiconductors for organic thin film transistors.* Journal of the American Chemical Society, 2008. **130**(37): p. 12273-12275.

19. Rockelé, M., D.V. Pham, A. Hoppe, J. Steiger, S. Botnaras, M. Nag, S. Steudel, K. Myny, S. Schols, and R. Müller, *Low-temperature and scalable complementary thin-film technology based on solution-processed metal oxide n-TFTs and pentacene p-TFTs.* Organic Electronics, 2011. **12**(11): p. 1909-1913.

20. Park, S.K., Y.H. Kim, and J.I. Han, *All solution-processed high-resolution bottom-contact transparent metal-oxide thin film transistors.* Journal of Physics D: Applied Physics, 2009. **42**(12): p. 125102.

21. Kamiya, T. and H. Hosono, *Material characteristics and applications of transparent amorphous oxide semiconductors.* NPG Asia Materials, 2010. **2**(1): p. 15-22.

22. Ginley, D., H. Hosono, and D.C. Paine, *Handbook of transparent conductors*. 2010: Springer Science & Business Media.

23. Sun, Y. and J.A. Rogers, *Inorganic semiconductors for flexible electronics.* Advanced Materials, 2007. **19**(15): p. 1897-1916.

24. Lee, J.S., Y.J. Kwack, and W.S. Choi, *Inkjet-Printed In_2O_3 Thin-Film Transistor below 200 C.* ACS Applied Materials & Interfaces, 2013. **5**(22): p. 11578-11583.

25. Hwang, Y.H., J.S. Seo, J.M. Yun, H. Park, S. Yang, S.-H.K. Park, and B.S. Bae, *An 'aqueous route'for the fabrication of low-temperature-processable oxide flexible transparent thin-film transistors on plastic substrates.* NPG Asia Materials, 2013. **5**(4): p. e45.

26. Kim, M.G., M.G. Kanatzidis, A. Facchetti, and T.J. Marks, *Low-temperature fabrication of high-performance metal oxide thin-film electronics via combustion processing.* Nature Materials, 2011. **10**(5): p. 382-388.

27. Han, S.Y., G.S. Herman, and C.h. Chang, *Low-temperature, high-performance, solution-processed indium oxide thin-film transistors.* Journal of the American Chemical Society, 2011. **133**(14): p. 5166-5169.

28. Vygranenko, Y., K. Wang, and A. Nathan, *Stable indium oxide thin-film transistors with fast threshold voltage recovery.* Applied Physics Letters, 2007. **91**(26): p. 263508.

29. Pal, B.N., P. Trottman, J. Sun, and H.E. Katz, *Solution-Deposited Zinc Oxide and Zinc Oxide/Pentacene Bilayer Transistors: High Mobility n-Channel, Ambipolar, and Nonvolatile Devices.* Advanced Functional Materials, 2008. **18**(12): p. 1832-1839.

30. Faber, H., J. Hirschmann, M. Klaumünzer, B.r. Braunschweig, W. Peukert, and M. Halik, *Impact of oxygen plasma treatment on the device performance of zinc oxide nanoparticle-based thin-film transistors.* ACS Applied Materials & Interfaces, 2012. **4**(3): p. 1693-1696.

31. Diao, Y., L. Shaw, Z. Bao, and S.C. Mannsfeld, *Morphology control strategies for solution-processed organic semiconductor thin films.* Energy & Environmental Science, 2014. **7**(7): p. 2145-2159.

32. Thomas, S.R., P. Pattanasattayavong, and T.D. Anthopoulos, *Solution-processable metal oxide semiconductors for thin-film transistor applications.* Chemical Society Reviews, 2013. **42**(16): p. 6910-6923.

33. Sirringhaus, H., R. Friend, T. Kawase, and L. Buergi, *Thin-Film Transistors.* Marcel Dekker, NewYork, 2003.

34. Park, S.K., Y.H. Kim, J.I. Han, D.G. Moon, and W.K. Kim, *High-performance polymer TFTs printed on a plastic substrate.* Electron Devices, IEEE Transactions on, 2002. **49**(11): p. 2008-2015.

35. Kergoat, L., N. Battaglini, L. Miozzo, B. Piro, M.C. Pham, A. Yassar, and G. Horowitz,*Use of poly (3-hexylthiophene)/poly (methyl methacrylate)(P3HT/PMMA) blends to improve the performance of water-gated organic field-effect transistors.* Organic Electronics, 2011. **12**(7): p. 1253-1257.

36. Assadi, A., C. Svensson, M. Willander, and O. Inganäs, *Field-effect mobility of poly (3-hexylthiophene).* Applied Physics Letters, 1988. **53**(3): p. 195-197.

37. Rincon Llorente, G., *Synthesis and characterisation of solution processable acenes*. 2010, University of Manchester.

38. Kim, Y.H., J.H. Lee, M.K. Han, and J.I. Han. *Electrical properties of triisopropylsilyl pentacene organic thin-film transistors by ink-jet method*. in *Proc. of ASID*. 2006.

39. Hwang, D.K., C. Fuentes-Hernandez, J.D. Berrigan, Y. Fang, J. Kim, W.J. Potscavage, H. Cheun, K.H. Sandhage, and B. Kippelen, *Solvent and polymer matrix effects on TIPS-pentacene/polymer blend organic field-effect transistors.* Journal of Materials Chemistry, 2012. **22**(12): p. 5531-5537.

40. Hamilton, R., J. Smith, S. Ogier, M. Heeney, J.E. Anthony, I. McCulloch, J. Veres, D.D. Bradley, and T.D. Anthopoulos, *High-performance polymer-small molecule blend organic transistors.* Advanced Materials, 2009. **21**(10-11): p. 1166-1171.

41. Nomura, K., H. Ohta, K. Ueda, T. Kamiya, M. Hirano, and H. Hosono, *Thin-film transistor fabricated in single-crystalline transparent oxide semiconductor.* Science, 2003. **300**(5623): p. 1269-1272.

42. Mathews, W.P., R.N. Vemuri, and T.L. Alford, *Influence of extended bias stress on the electrical parameters of mixed oxide thin film transistors.* Circiuts and Systems 2012. **3**: p. 295-299.

43. Necliudov, P.V., M.S. Shur, D.J. Gundlach, and T.N. Jackson, *Contact resistance extraction in pentacene thin film transistors.* Solid-State Electronics, 2003. **47**(2): p. 259-262.

44. Street, R. and A. Salleo, *Contact effects in polymer transistors.* Applied Physics Letters, 2002. **81**(15): p. 2887-2889.

45. Zhang, X., *Device engineering of organic field-effect transistors toward complementary circuits*. 2009: ProQuest.

46. Zaumseil, J. and H. Sirringhaus, *Electron and ambipolar transport in organic field-effect transistors.* Chemical Reviews, 2007. **107**(4): p. 1296-1323.

47. Bain, S., *Kelvin force microscopy of polymer and small molecule thin-film transistors*. 2011, University of Southampton.

48. Weis, M., *Gradual channel approximation models for organic field-effect transistors: The space-charge field effect.* Journal of Applied Physics, 2012. **111**(5): p. 054506.

49. Wager, J.F., D.A. Keszler, and R.E. Presley, *Transparent electronics*. 2008: Springer.

50. Robertson, J., *High dielectric constant oxides.* The European Physical Journal Applied Physics, 2004. **28**(03): p. 265-291.

51. Brütting, W., *Physics of organic semiconductors*. 2006: John Wiley & Sons.

52. Tickle, A.C., *Thin-film transistors: a new approach to microelectronics*. 1969: John Wiley & Sons.

53. Schroder, D.K. and L.G. Rubin, *Semiconductor material and device characterization.* Physics Today, 2008. **44**(4): p. 107-108.

54. Calvetti, E., L. Colalongo, and Z.M. Kovács-Vajna, *Organic thin film transistors: a DC/dynamic analytical model.* Solid-State Electronics, 2005. **49**(4): p. 567-577.

55. Dimitrakopoulos, C.D. and P.R. Malenfant, *Organic thin film transistors for large area electronics.* Advanced Materials, 2002. **14**(2): p. 99.

56. Blanchet, G.B., C. Fincher, M. Lefenfeld, and J. Rogers, *Contact resistance in organic thin film transistors.* Applied Physics Letters, 2004. **84**(2): p. 296-298.

57. Kelley, T.W. and C.D. Frisbie, *Point contact current–voltage measurements on individual organic semiconductor grains by conducting probe atomic force microscopy.* Journal of Vacuum Science & Technology B, 2000. **18**(2): p. 632-635.

58. Zaumseil, J., K.W. Baldwin, and J.A. Rogers, *Contact resistance in organic transistors that use source and drain electrodes formed by soft contact lamination.* Journal of Applied Physics, 2003. **93**(10): p. 6117-6124.

59. Xu, Y., R. Gwoziecki, I. Chartier, R. Coppard, F. Balestra, and G. Ghibaudo, *Modified transmission-line method for contact resistance extraction in organic field-effect transistors.* Applied Physics Letters, 2010. **97**(6): p. 063302.

60. Pochettino, A., *Sul comportamento foto-elettrico dell'antracene.* Acad. Lincei Rend, 1906. **15**: p. 355.

61. Chiang, C.K., C. Fincher Jr, Y.W. Park, A.J. Heeger, H. Shirakawa, E.J. Louis, S.C. Gau, and A.G. MacDiarmid, *Electrical conductivity in doped polyacetylene.* Physical Review Letters, 1977. **39**(17): p. 1098.

62. Horowitz, G., D. Fichou, X. Peng, Z. Xu, and F. Garnier, *A field-effect transistor based on conjugated alpha-sexithienyl.* Solid State Communications, 1989. **72**(4): p. 381-384.

63. Park, S.K., T.N. Jackson, J.E. Anthony, and D.A. Mourey, *High mobility solution processed 6, 13-bis (triisopropyl-silylethynyl) pentacene organic thin film transistors.* Applied Physics Letters, 2007. **91**(6): p. 063514-063514.

64. Koželj, M., B. Cvikl, and D. Korošak. *Application of organic semiconductors for the detection of ionizing radiations*. in *Proc. International Conference Nuclear Energy for New Europe*. 2006.

65. Gomathi, N., V.K. Prasad, and S. Neogi, *Preparation and characterization of thin films of the poly (p-phenylene vinylene) semiconducting polymer.* Journal of Applied Polymer Science, 2009. **111**(4): p. 1917-1922.

66. Malloci, G., G. Mulas, G. Cappellini, and C. Joblin, *Time-dependent density functional study of the electronic spectra of oligoacenes in the charge states− 1, 0,+ 1, and+ 2.* Chemical Physics, 2007. **340**(1): p. 43-58.

67. Ostroverkhova, O., D. Cooke, S. Shcherbyna, R. Egerton, F. Hegmann, R. Tykwinski, and J. Anthony, *Bandlike transport in pentacene and functionalized*

pentacene thin films revealed by subpicosecond transient photoconductivity measurements. Physical Review B, 2005. **71**(3): p. 035204.

68. Coropceanu, V., J. Cornil, D.A. da Silva Filho, Y. Olivier, R. Silbey, and J.-L. Brédas, *Charge transport in organic semiconductors.* Chemical Reviews, 2007. **107**(4): p. 926-952.

69. Kahn, A., N. Koch, and W. Gao, *Electronic structure and electrical properties of interfaces between metals and π-conjugated molecular films.* Journal of Polymer Science Part B: Polymer Physics, 2003. **41**(21): p. 2529-2548.

70. Shen, Y., A.R. Hosseini, M.H. Wong, and G.G. Malliaras, *How to make ohmic contacts to organic semiconductors.* ChemPhysChem, 2004. **5**(1): p. 16-25.

71. Horowitz, G., *Organic field-effect transistors.* Advanced Materials, 1998. **10**(5): p. 365-377.

72. Jurchescu, O.D., J. Baas, and T. Palstra, *The effect of impurities on the mobility of single crystal pentacene.* arXiv preprint cond-mat/0404130, 2004.

73. Hong, M., B. Kim, Y. Lee, K. Song, J. Oh, J. Kim, T. Choi, M. Ryu, K. Chung, and S. Lee. *3.5: Invited Paper: Recent Progress in Large Sized & High Performance Organic TFT Array*. in *SID Symposium Digest of Technical Papers*. 2005. Wiley Online Library.

74. Maliakal, A., K. Raghavachari, H. Katz, E. Chandross, and T. Siegrist, *Photochemical stability of pentacene and a substituted pentacene in solution and in thin films.* Chemistry of Materials, 2004. **16**(24): p. 4980-4986.

75. Kuo, C.C., *High performance small-molecule organic thin film transistors*. 2005, The Pennsylvania State University.

76. Shin, S.I., J.H. Kwon, H. Kang, and B.K. Ju, *Solution-processed 6, 13-bis (triisopropylsilylethynyl)(TIPS) pentacene thin-film transistors with a polymer dielectric on a flexible substrate.* Semiconductor Science and Technology, 2008. **23**(8): p. 085009.

77. Hong, J.P., A.Y. Park, S. Lee, J. Kang, N. Shin, and D.Y. Yoon, *Tuning of Ag work functions by self-assembled monolayers of aromatic thiols for an efficient hole injection for solution processed triisopropylsilylethynyl pentacene organic thin film transistors.* Applied Physics Letters, 2008. **92**(14): p. 143311.

78. Payne, M.M., S.R. Parkin, J.E. Anthony, C.C. Kuo, and T.N. Jackson, *Organic Field-Effect Transistors from Solution-Deposited Functionalized Acenes with Mobilities as High as 1* $cm^2V^{-1}s^{-1}$. Journal of the American Chemical Society, 2005. **127**(14): p. 4986-4987.

79. Kaur, I., W. Jia, R.P. Kopreski, S. Selvarasah, M.R. Dokmeci, C. Pramanik, N.E. McGruer, and G.P. Miller, *Substituent effects in pentacenes: Gaining control over HOMO− LUMO gaps and photooxidative resistances.* Journal of the American Chemical Society, 2008. **130**(48): p. 16274-16286.

80. Hossain, F.M., J. Nishii, S. Takagi, A. Ohtomo, T. Fukumura, H. Fujioka, H. Ohno, H. Koinuma, and M. Kawasaki, *Modeling and simulation of polycrystalline ZnO thin-film transistors.* Journal of Applied Physics, 2003. **94**(12): p. 7768-7777.

81. Nomura, K., T. Kamiya, H. Ohta, T. Uruga, M. Hirano, and H. Hosono, *Local coordination structure and electronic structure of the large electron mobility amorphous oxide semiconductor InGaZnO: Experiment and ab initio calculations.* Physical Review B, 2007. **75**(3): p. 035212.

82. Kim, M.G., H.S. Kim, Y.G. Ha, J. He, M.G. Kanatzidis, A. Facchetti, and T.J. Marks, *High-performance solution-processed amorphous zinc− indium− tin oxide thin-film transistors.* Journal of the American Chemical Society, 2010. **132**(30): p. 10352-10364.

83. Sele, C.W., B. Kjellander, B. Niesen, M.J. Thornton, J. Van der Putten, K. Myny, H.J. Wondergem, A. Moser, R. Resel, and A.J. van Breemen, *Controlled deposition of highly ordered soluble acene thin films: effect of morphology and crystal orientation on transistor performance.* Advanced Materials, 2009. **21**(48): p. 4926-4931.

84. Rogowski, R.Z., A. Dzwilewski, M. Kemerink, and A.A. Darhuber, *Solution processing of semiconducting organic molecules for tailored charge transport properties.* The Journal of Physical Chemistry C, 2011. **115**(23): p. 11758-11762.

85. Chen, J., D.C. Martin, and J.E. Anthony, *Morphology and molecular orientation of thin-film bis (triisopropylsilylethynyl) pentacene.* Journal of Materials Research, 2007. **22**(06): p. 1701-1709.

86. Headrick, R., S. Wo, F. Sansoz, and J. Anthony, *Anisotropic mobility in large grain size solution processed organic semiconductor thin films.* Applied Physics Letters, 2008. **92**(6): p. 063302-063302-3.

87. Hamadani, B., D. Gundlach, I. McCulloch, and M. Heeney, *Undoped polythiophene field-effect transistors with mobility of 1* $cm^2V^{-1}s^{-1}$. Applied Physics Letters, 2007. **91**(24): p. 243512-243512-3.

88. Ojovan, M.I. and W.B.E. Lee, *Connectivity and glass transition in disordered oxide systems.* Journal of Non-Crystalline Solids, 2010. **356**(44): p. 2534-2540.

89. Mark, J.E., *Physical properties of polymers handbook.* Vol. 1076. 2007: Springer.

90. Lee, W.H. and Y.D. Park, *Organic Semiconductor/Insulator Polymer Blends for High-Performance Organic Transistors.* Polymers, 2014. **6**(4): p. 1057-1073.

91. Moons, E., *Conjugated polymer blends: linking film morphology to performance of light emitting diodes and photodiodes.* Journal of Physics: Condensed Matter, 2002. **14**(47): p. 12235.

92. Song, s. and J. Torkelson, *Phase separation phenomina in polysterene solution.* Korean Polymer Journal 1995. **3**: p. 86-93.

93. Ohe, T., M. Kuribayashi, A. Tsuboi, K. Satori, M. Itabashi, and K. Nomoto, *Organic thin-film transistors with phase separation of polymer-blend small-molecule semiconductors: Dependence on molecular weight and types of polymer.* Applied Physics Express, 2009. **2**(12): p. 121502.

94. Wang, Z., Y. Liu, and Z. Zhang, *Handbook of Nanophase and Nanostructured Materials.* Kluwer Acadimic/Plenum Publisher. New York,USA, 2003. **Volume I: Synthesis**.

95. Burke, J., *Solubility parameters: theory and application.* 1984.

96. Brandrup, J., E.H. Immergut, E.A. Grulke, A. Abe, and D.R. Bloch, *Polymer handbook*. Vol. 89. 1999: Wiley New York.

97. Abu-Sen, L., *Environmental Stability Studies of an Organic Semiconductor.* 2013.

98. Keddie, J.L. and A.F. Routh, *Fundamentals of latex film formation: processes and properties*. 2010: Springer.

99. Yang, H., S.W. LeFevre, C.Y. Ryu, and Z. Bao, *Solubility-driven thin film structures of regioregular poly (3-hexyl thiophene) using volatile solvents.* Applied Physics Letters, 2007. **90**(17): p. 172116-172116-3.

100. Kim, J., J. Jeong, H.D. Cho, C. Lee, S.O. Kim, S.-K. Kwon, and Y. Hong, *All-solution-processed bottom-gate organic thin-film transistor with improved subthreshold behaviour using functionalized pentacene active layer.* Journal of Physics D: Applied Physics, 2009. **42**(11): p. 115107.

101. Mannsfeld, S.C., M.L. Tang, and Z. Bao, *Thin film structure of triisopropylsilylethynyl-functionalized pentacene and tetraceno [2,3-b] thiophene from grazing incidence X-Ray diffraction.* Advanced Materials, 2011. **23**(1): p. 127-131.

102. Akkerman, H.B., H. Li, and Z. Bao, *TIPS-pentacene crystalline thin film growth.* Organic Electronics, 2012. **13**(10): p. 2056-2062.

103. Lim, J.A., W.H. Lee, H.S. Lee, J.H. Lee, Y.D. Park, and K. Cho, *Self-Organization of Ink-jet-Printed Triisopropylsilylethynyl Pentacene via Evaporation-Induced Flows in a Drying Droplet.* Advanced Functional Materials, 2008. **18**(2): p. 229-234.

104. De Gans, B.-J. and U.S. Schubert, *Inkjet printing of well-defined polymer dots and arrays.* Langmuir, 2004. **20**(18): p. 7789-7793.

105. Kimura, M., M.J. Misner, T. Xu, S.H. Kim, and T.P. Russell, *Long-range ordering of diblock copolymers induced by droplet pinning.* Langmuir, 2003. **19**(23): p. 9910-9913.

106. Lee, W.H., D.H. Kim, Y. Jang, J.H. Cho, M. Hwang, Y.D. Park, Y.H. Kim, J.I. Han, and K. Cho, *Solution-processable pentacene microcrystal arrays for high performance organic field-effect transistors.* Applied Physics Letters, 2007. **90**(13): p. 132106.

107. Lim, J.A., H.S. Lee, W.H. Lee, and K. Cho, *Control of the Morphology and Structural Development of Solution-Processed Functionalized Acenes for High-Performance Organic Transistors.* Advanced Functional Materials, 2009. **19**(10): p. 1515-1525.

108. Park, J. and J. Moon, *Control of colloidal particle deposit patterns within picoliter droplets ejected by ink-jet printing.* Langmuir, 2006. **22**(8): p. 3506-3513.

109. Lee, M.W., G.S. Ryu, Y.U. Lee, C. Pearson, M.C. Petty, and C.K. Song, *Control of droplet morphology for inkjet-printed TIPS-pentacene transistors.* Microelectronic Engineering, 2012. **95**: p. 1-4.

110. Takazawa, K., Y. Kitahama, Y. Kimura, and G. Kido, *Optical waveguide self-assembled from organic dye molecules in solution.* Nano Letters, 2005. **5**(7): p. 1293-1296.

111. Madec, M.B., D. Crouch, G.R. Llorente, T.J. Whittle, M. Geoghegan, and S.G. Yeates, *Organic field effect transistors from ambient solution processed low molar mass semiconductor–insulator blends.* Journal of Materials Chemistry, 2008. **18**(27): p. 3230-3236.

112. James, D.T., B.C. Kjellander, W.T. Smaal, G.H. Gelinck, C. Combe, I. McCulloch, R. Wilson, J.H. Burroughes, D.D. Bradley, and J.-S. Kim, *Thin-film morphology of inkjet-printed single-droplet organic transistors using polarized raman spectroscopy: effect of blending TIPS-pentacene with insulating polymer.* Acs Nano, 2011. **5**(12): p. 9824-9835.

113. Claudia Arias, A., *Vertically segregated polymer blends: Their use in organic electronics.* Journal of Macromolecular Science Part C: Polymer Reviews, 2006. **46**(1): p. 103-125.

114. Smith, J., R. Hamilton, I. McCulloch, N. Stingelin-Stutzmann, M. Heeney, D.D. Bradley, and T.D. Anthopoulos, *Solution-processed organic transistors based on semiconducting blends.* Journal of Materials Chemistry, 2010. **20**(13): p. 2562-2574.

115. Kim, Y.H., J.E. Anthony, and S.K. Park, *Polymer blended small molecule organic field effect transistors with improved device-to-device uniformity and operational stability.* Organic Electronics, 2012. **13**(7): p. 1152-1157.

116. Lee, W.H., J.A. Lim, D. Kwak, J.H. Cho, H.S. Lee, H.H. Choi, and K. Cho, *Semiconductor-Dielectric Blends: A Facile All Solution Route to Flexible All-Organic Transistors.* Advanced Materials, 2009. **21**(42): p. 4243-4248.

117. Chou, W.Y., C.W. Kuo, H.L. Cheng, Y.R. Chen, F.C. Tang, F.Y. Yang, D.Y. Shu, and C.C. Liao, *Effect of surface free energy in gate dielectric in pentacene thin-film transistors.* Applied Physics Letters, 2006. **89**(11): p. 112126.

118. Pitsalidis, C., N. Kalfagiannis, N.A. Hastas, P. Karagiannidis, C. Kapnopoulos, A. Ioakeimidis, and S. Logothetidis, *High performance transistors based on the controlled growth of triisopropylsilylethynyl-pentacene crystals via non-isotropic solvent evaporation.* RSC Advances, 2014. **4**(40): p. 20804-20813.

119. Li, X., W.T. Smaal, C. Kjellander, B. van der Putten, K. Gualandris, E.C. Smits, J. Anthony, D.J. Broer, P.W. Blom, and J. Genoe, *Charge transport in high-performance ink-jet printed single-droplet organic transistors based on a silylethynyl substituted pentacene/insulating polymer blend.* Organic Electronics, 2011. **12**(8): p. 1319-1327.

120. Yoon.D, Chuang.Y, Shen.N, Jo.Y, Kang.J, Prabho.V, Delonchamp.D, Kline.J, Richter.L, Gundlach.D, and Anthony.J, MRS Fall Meeting Boston USA 2010.

121. Lee, D.H., Y.J. Chang, G.S. Herman, and C.H. Chang, *A General Route to Printable High-Mobility Transparent Amorphous Oxide Semiconductors.* Advanced Materials, 2007. **19**(6): p. 843-847.

122. Jin, J., *Metal-oxide-based electronic devices*. 2013, The University of Manchester.

123. Prins, M., K.O. Grosse-Holz, G. Müller, J. Cillessen, J. Giesbers, R. Weening, and R. Wolf, *A ferroelectric transparent thin-film transistor.* Applied Physics Letters, 1996. **68**(25): p. 3650-3652.

124. Li, C.s., Y.n. Li, Y.l. Wu, B.S. Ong, and R.O. Loutfy, *Fabrication conditions for solution-processed high-mobility ZnO thin-film transistors.* Journal of Materials Chemistry, 2009. **19**(11): p. 1626-1634.

125. Zhang, H.Z., H.T. Cao, A.H. Chen, L.Y. Liang, Z.M. Liu, and Q. Wan, *Enhancement of electrical performance in In_2O_3 thin-film transistors by improving the densification and surface morphology of channel layers.* Solid-State Electronics, 2010. **54**(4): p. 479-483.

126. Paine, D.C., B. Yaglioglu, Z. Beiley, and S. Lee, *Amorphous IZO-based transparent thin film transistors.* Thin Solid Films, 2008. **516**(17): p. 5894-5898.

127. Wang, Y., X.W. Sun, G.K.L. Goh, H.V. Demir, and H.Y. Yu, *Influence of channel layer thickness on the electrical performances of inkjet-printed InGaZn oxide thin-film transistors.* Electron Devices, IEEE Transactions on, 2011. **58**(2): p. 480-485.

128. Noh, J.H., S.Y. Ryu, S.J. Jo, C.S. Kim, S.-W. Sohn, P.D. Rack, D.-J. Kim, and H.K. Baik, *Indium oxide thin-film transistors fabricated by RF sputtering at room temperature.* Electron Device Letters, IEEE, 2010. **31**(6): p. 567-569.

129. Kang, D.H., J.U. Han, M. Mativenga, S.H. Ha, and J. Jang, *Threshold voltage dependence on channel length in amorphous-indium-gallium-zinc-oxide thin-film transistors.* Applied Physics Letters, 2013. **102**(8): p. 083508.

130. Lan, L., M. Xu, J. Peng, H. Xu, M. Li, D. Luo, J. Zou, H. Tao, L. Wang, and R. Yao, *Influence of source and drain contacts on the properties of the indium-zinc oxide thin-film transistors based on anodic aluminum oxide gate dielectrics.* Journal of Applied Physics, 2011. **110**(10): p. 103703.

131. Kim, H.S., P.D. Byrne, A. Facchetti, and T.J. Marks, *High performance solution-processed indium oxide thin-film transistors.* Journal of the American Chemical Society, 2008. **130**(38): p. 12580-12581.

132. Choi, J.H., U.B. Han, K.C. Lee, J.H. Lee, J.J. Kim, I.T. Cho, J.H. Lee, and Y.W. Heo, *Transfer characteristics and bias-stress stability of amorphous indium zinc oxide thin-film transistors.* Journal of Vacuum Science & Technology B, 2009. **27**(2): p. 622-625.

133. Cheng, H.C., C.F. Chen, and C.C. Lee, *Thin-film transistors with active layers of zinc oxide (ZnO) fabricated by low-temperature chemical bath method.* Thin Solid Films, 2006. **498**(1): p. 142-145.

134. Nakazawa, H., Y. Ito, E. Matsumoto, K. Adachi, N. Aoki, and Y. Ochiai, *The electronic properties of amorphous and crystallized In_2O_3 films.* Journal of Applied Physics, 2006. **100**(9): p. 093706.

135. Weiher, R. and R. Ley, *Optical properties of indium oxide.* Journal of Applied Physics, 1966. **37**(1): p. 299-302.

136. Dhananjay, C., *Realization of In_2O_3 thin film transistors through reactive evaporation process.* Applied Physics Letters, 2007. **91**(13): p. 2111.

137. Jiao, Y., X. Zhang, J. Zhai, X. Yu, L. Ding, and W. Zhang, *Bottom-gate amorphous In_2O_3 thin film transistors fabricated by magnetron sputtering.* Electronic Materials Letters, 2013. **9**(3): p. 279-282.

138. Faber, H., Y.H. Lin, S.R. Thomas, K. Zhao, N. Pliatsikas, M.A. McLachlan, A. Amassian, P.A. Patsalas, and T.D. Anthopoulos, *Indium Oxide Thin-Film Transistors Processed at Low Temperature via Ultrasonic Spray Pyrolysis.* ACS Applied Materials & Interfaces, 2014. **7**(1): p. 782-790.

139. Chung, J., J. Lee, H. Kim, N. Jang, and J. Kim, *Effect of thickness of ZnO active layer on ZnO-TFT's characteristics.* Thin Solid Films, 2008. **516**(16): p. 5597-5601.

140. Hsieh, H.H. and C.C. Wu, *Scaling behavior of ZnO transparent thin-film transistors.* Applied Physics Letters, 2006. **89**(4): p. 1109.

141. Cheng, S.S., C.Y. Yang, C.W. Ou, Y.C. Chuang, M.C. Wu, and C.W. Chu, *Dependence of channel thickness on the performance of In_2O_3 thin film transistors.* Journal of Physics D: Applied Physics, 2008. **41**(9): p. 092006.

142. Hoshino, S., T. Kamata, and K. Yase, *Effect of active layer thickness on device properties of organic thin-film transistors based on Cu (II) phthalocyanine.* Journal of Applied Physics, 2002. **92**(10): p. 6028-6032.

143. Barquinha, P., A. Pimentel, A. Marques, L. Pereira, R. Martins, and E. Fortunato, *Influence of the semiconductor thickness on the electrical properties of transparent TFTs based on indium zinc oxide.* Journal of Non-crystalline Solids, 2006. **352**(9): p. 1749-1752.

144. Jeong, J. and Y. Hong, *Debye length and active layer thickness-dependent performance variations of amorphous oxide-based TFTs.* Electron Devices, IEEE Transactions on, 2012. **59**(3): p. 710-714.

145. Libsch, F. and J. Kanicki, *Bias-stress-induced stretched-exponential time dependence of charge injection and trapping in amorphous thin-film transistors.* Applied Physics Letters, 1993. **62**(11): p. 1286-1288.

146. Lee, J.M., I.T. Cho, J.H. Lee, and H.I. Kwon, *Bias-stress-induced stretched-exponential time dependence of threshold voltage shift in InGaZnO thin film transistors.* Applied Physics Letters, 2008. **93**(9): p. 093504.

147. Zafar, S., A. Callegari, E. Gusev, and M.V. Fischetti, *Charge trapping related threshold voltage instabilities in high permittivity gate dielectric stacks.* Journal of Applied physics, 2003. **93**: p. 9298-9303.

148. Shih, C.C., Y.S. Lee, K.L. Fang, C.H. Chen, and F.Y. Gan, *A current estimation method for bias-temperature stress of a-Si TFT device.* Device and Materials Reliability, IEEE Transactions on, 2007. **7**(2): p. 347-350.

149. Suresh, A. and J. Muth, *Bias stress stability of indium gallium zinc oxide channel based transparent thin film transistors.* Applied Physics Letters, 2008. **92**(3): p. 033502.

150. Kaftanoglu, K., S.M. Venugopal, M. Marrs, A. Dey, E.J. Bawolek, D.R. Allee, and D. Loy, *Stability of IZO and a-Si: H TFTs processed at low temperature (200 C).* Journal of Display Technology, 2011. **7**(6): p. 339-343.

151. Mathews, W.P., R.N. Vemuri, and T.L. Alford, *Influence of extended bias stress on the electrical parameters of mixed oxide thin film transistors.* 2012: p. 295-299.

152. Lopes, M., H.L. Gomes, M. Medeiros, P. Barquinha, L. Pereira, E. Fortunato, R. Martins, and I. Ferreira, *Gate-bias stress in amorphous oxide semiconductors thin-film transistors.* Applied Physics Letters, 2009. **95**(6): p. 063502.

153. Vygranenko, Y., K. Wang, R. Chaji, M. Vieira, J. Robertson, and A. Nathan, *Stability of indium-oxide thin-film transistors by reactive ion beam assisted deposition.* Thin Solid Films, 2009. **517**(23): p. 6341-6344.

154. Mathijssen, S.G., M.J. Spijkman, A.M. Andringa, P.A. van Hal, I. McCulloch, M. Kemerink, R.A. Janssen, and D.M. de Leeuw, *Revealing Buried Interfaces to*

Understand the Origins of Threshold Voltage Shifts in Organic Field-Effect Transistors. Advanced Materials, 2010. **22**(45): p. 5105-5109.

155. Okamura, K., N. Mechau, D. Nikolova, and H. Hahn, *Influence of interface roughness on the performance of nanoparticulate zinc oxide field-effect transistors.* Applied Physics Letters, 2008. **93**(8): p. 083105.

156. Jo, G., J. Maeng, T. Kim, W. Hong, B. Choi, and T. Lee, *Channel-length and gate-bias dependence of contact resistance and mobility for In_2O_3 nanowire field effect transistors.* Journal of Applied Physics, 2007. **102**(8): p. 084508.

157. Shimura, Y., K. Nomura, H. Yanagi, T. Kamiya, M. Hirano, and H. Hosono, *Specific contact resistances between amorphous oxide semiconductor InGaZnO and metallic electrodes.* Thin Solid Films, 2008. **516**(17): p. 5899-5902.

158. Okamura, K. and H. Hahn, *Carrier transport in nanocrystalline field-effect transistors: Impact of interface roughness and geometrical carrier trap.* Applied Physics Letters, 2010. **97**(15): p. 153114.

159. Lee, K., J.H. Kim, S. Im, C.S. Kim, and H.K. Baik, *Low-voltage-driven top-gate ZnO thin-film transistors with polymer/high-k oxide double-layer dielectric.* Applied Physics Letters, 2006. **89**(13): p. 3507.

160. Beena, D., K. Lethy, R. Vinodkumar, A. Detty, V.M. Pillai, and V. Ganesan, *Photoluminescence in laser ablated nanostructured indium oxide thin films.* Journal of Alloys and Compounds, 2010. **489**(1): p. 215-223.

161. Remashan, K., D.K. Hwang, S.J. Park, and J.H. Jang, *Effect of rapid thermal annealing on the electrical characteristics of ZnO thin-film transistors.* Japanese Journal of Applied Physics, 2008. **47**(4S): p. 2848.

162. Hong, D., G. Yerubandi, H. Chiang, M. Spiegelberg, and J. Wager, *Electrical modeling of thin-film transistors.* Critical Reviews in Solid State and Materials Sciences, 2008. **33**(2): p. 101-132.

163. Fortunato, E., P. Barquinha, A. Pimentel, A. Goncalves, A. Marques, L. Pereira, and R. Martins, *Recent advances in ZnO transparent thin film transistors.* Thin Solid Films, 2005. **487**(1): p. 205-211.

164. Zhang, X.A., J.W. Zhang, W.F. Zhang, D. Wang, Z. Bi, X.M. Bian, and X. Hou, *Enhancement-mode thin film transistor with nitrogen-doped ZnO channel layer deposited by laser molecular beam epitaxy.* Thin Solid Films, 2008. **516**(10): p. 3305-3308.

165. Krupanidhi, S., *Low threshold voltage ZnO thin film transistor with a Zn0. 7Mg0.3O gate dielectric for transparent electronics.* Journal of Applied Physics, 2007. **101**(12): p. 123717.

166. Hoffman, R., B.J. Norris, and J. Wager, *ZnO-based transparent thin-film transistors.* Applied Physics Letters, 2003. **82**(5): p. 733-735.

167. Yaglioglu, B., H. Yeom, R. Beresford, and D. Paine, *High-mobility amorphous In_2O_3 10wt% ZnO thin film transistors.* Applied Physics Letters, 2006. **89**(6): p. 062103.

168. Park, J.-S., J.K. Jeong, Y.-G. Mo, H.D. Kim, and C.-J. Kim, *Control of threshold voltage in ZnO-based oxide thin film transistors.* Applied Physics Letters, 2008. **93**(3): p. 3513.

169. Oh, B.Y., M.C. Jeong, M.H. Ham, and J.M. Myoung, *Effects of the channel thickness on the structural and electrical characteristics of room-temperature fabricated ZnO thin-film transistors.* Semiconductor Science and Technology, 2007. **22**(6): p. 608.

170. Nomura, K., T. Kamiya, M. Hirano, and H. Hosono, *Origins of threshold voltage shifts in room-temperature deposited and annealed a-InGaZnO thin-film transistors.* Applied Physics Letters, 2009. **95**(1): p. 3502.

171. Merticaru, A. and A. Mouthaan, *Dynamics of metastable defects in a-Si: H/SiN TFTs.* Thin Solid Films, 2001. **383**(1): p. 122-124.

172. Jeong, Y., K. Song, D. Kim, C.Y. Koo, and J. Moon, *Bias stress stability of solution-processed zinc tin oxide thin-film transistors.* Journal of The Electrochemical Society, 2009. **156**(11): p. H808-H812.

173. Young, N. and A. Gill, *Electron trapping instabilities in polycrystalline silicon thin film transistors.* Semiconductor Science and Technology, 1990. **5**(1): p. 72.

174. Cross, R. and M. De Souza, *Investigating the stability of zinc oxide thin film transistors.* Applied Physics Letters, 2006. **89**(26): p. 263513.

175. Berberan-Santos, M., E. Bodunov, and B. Valeur, *Mathematical functions for the analysis of luminescence decays with underlying distributions 1. Kohlrausch decay function (stretched exponential).* Chemical Physics, 2005. **315**(1): p. 171-182.

176. Mathijssen, S.G., M. Cölle, H. Gomes, E.C. Smits, B. de Boer, I. McCulloch, P.A. Bobbert, and D.M. de Leeuw, *Dynamics of Threshold Voltage Shifts in Organic and Amorphous Silicon Field-Effect Transistors.* Advanced Materials, 2007. **19**(19): p. 2785-2789.

177. Merticaru, A.R., A.J. Mouthaan, and F.G. Kuper, *Current degradation of a-Si: H/SiN TFTs at room temperature and low voltages.* Electron Devices, IEEE Transactions on, 2006. **53**(9): p. 2273-2279.

178. Schoonveld, W., J. Oostinga, J. Vrijmoeth, and T. Klapwijk, *Charge trapping instabilities of sexithiophene thin film transistors.* Synthetic metals, 1999. **101**(1): p. 608-609.

179. Ng, T.N., J.A. Marohn, and M.L. Chabinyc, *Comparing the kinetics of bias stress in organic field-effect transistors with different dielectric interfaces.* Journal of Applied Physics, 2006. **100**(8): p. 084505.

180. Bürgi, L., T. Richards, M. Chiesa, R.H. Friend, and H. Sirringhaus, *A microscopic view of charge transport in polymer transistors.* Synthetic Metals, 2004. **146**(3): p. 297-309.

181. Ha, S.H., D.H. Kang, I. Kang, J.U. Han, M. Mativenga, and J. Jang, *Channel length dependent bias-stability of self-aligned coplanar a-IGZO TFTs.* Display Technology, Journal of, 2013. **9**(12): p. 985-988.

182. Kolawa, E., C. Garland, L. Tran, C. Nieh, J. Molarius, W. Flick, M.A. Nicolet, and J. Wei, *Indium oxide diffusion barriers for Al/Si metallizations.* Applied Physics Letters, 1988. **53**(26): p. 2644-2646.

183. Ma, T.Y., *Effects of an Aluminum Contact on the Carrier Mobility and Threshold Voltage of Zinc Tin Oxide Transparent Thin Film Transistors.* Journal of Electrical Engineering & Technology, 2014. **9**(2): p. 609-614.

184. *Atlas User's Manual.* 2007.

185. Lord, A.M., T.G. Maffeis, O. Kryvchenkova, R.J. Cobley, K. Kalna, D.M. Kepaptsoglou, Q.M. Ramasse, A.S. Walton, M.B. Ward, and J.r. Köble, *Controlling the electrical transport properties of nanocontacts to nanowires.* Nano Letters, 2015. **15**(7): p. 4248-4254.

186. Liscio, A., V. Palermo, K. Müllen, and P. Samorì, *Tip− sample interactions in Kelvin probe force microscopy: quantitative measurement of the local surface potential.* The Journal of Physical Chemistry C, 2008. **112**(44): p. 17368-17377.

187. Valdre, G. and D. Moro, *3D finite element analysis of electrostatic deflection of commercial and FIB-modified cantilevers for electric and Kelvin force microscopy: I. Triangular shaped cantilevers with symmetric pyramidal tips.* Nanotechnology, 2008. **19**(40): p. 405501.

188. Hamberg, I. and C.G. Granqvist, *Evaporated Sn-doped In_2O_3 films: Basic optical properties and applications to energy-efficient windows.* Journal of Applied Physics, 1986. **60**(11): p. R123-R160.

189. Lang, O., C. Pettenkofer, J.F. Sánchez Royo, A. Segura, A. Klein, and W. Jaegermann, *Thin film growth and band lineup of In_2O_3 on the layered semiconductor InSe.* Journal of Applied Physics, 1999. **86**(10).

190. Sacha, G., A. Verdaguer, J. Martinez, J. Sáenz, D. Ogletree, and M. Salmeron, *Effective tip radius in electrostatic force microscopy.* Applied Physics Letters, 2005. **86**(12): p. 123101.

191. Lei, C., S. Minne, Y. HU, M. Ji, J. He, H. Mittel, V. Kelly, N. Erina, S. Guo, and T. Muller, *Peak Force Kelvin probe Force Microscopy.* Bruker App, 2013. **140**: p. 1-14.

192. Martin, Y., D.W. Abraham, and H.K. Wickramasinghe, *High-resolution capacitance measurement and potentiometry by force microscopy.* Applied Physics Letters, 1988. **52**(13): p. 1103-1105.

193. Sarid, D., *Scanning force microscopy: with applications to electric, magnetic, and atomic forces.* 1994.

194. Annibale, P., C. Albonetti, P. Stoliar, and F. Biscarini, *High-resolution mapping of the electrostatic potential in organic thin-film transistors by phase electrostatic force microscopy.* The Journal of Physical Chemistry A, 2007. **111**(49): p. 12854-12858.

195. Ando, M., S. Heike, M. Kawasaki, and T. Hashizume, *Trapped charge mapping in crystalline organic transistors by using scanning Kelvin probe force microscopy.* Applied Physics Letters, 2014. **105**(19): p. 193303.

196. Mélin, T., M. Zdrojek, and D. Brunel, *Electrostatic force microscopy and Kelvin force microscopy as a probe of the electrostatic and electronic properties of carbon nanotubes*, in *Scanning Probe Microscopy in Nanoscience and Nanotechnology*. 2010, Springer. p. 89-128.

197. Cox, P.A., M.S. Glaz, J.S. Harrison, S.R. Peurifoy, D.C. Coffey, and D.S. Ginger, *Imaging Charge Transfer State Excitations in Polymer/Fullerene Solar Cells with Time-Resolved Electrostatic Force Microscopy.* The journal of Physical Chemistry Letters, 2015. **6**(15): p. 2852-2858.

198. Berger, R., A.L. Domanski, and S.A. Weber, *Electrical characterization of organic solar cell materials based on scanning force microscopy.* European Polymer Journal, 2013. **49**(8): p. 1907-1915.

199. Lu, Y., M. Muñoz, C. Steplecaru, C. Hao, M. Bai, N. Garcia, K. Schindler, and P. Esquinazi, *Electrostatic force microscopy on oriented graphite surfaces: coexistence of insulating and conducting behaviors.* Physical Review Letters, 2006. **97**(7): p. 076805.

200. Schaadt, D., E. Yu, S. Sankar, and A. Berkowitz, *Charge storage in Co nanoclusters embedded in SiO2 by scanning force microscopy.* Applied Physics Letters, 1999. **74**(3): p. 472-474.

201. Guillemot, C., P. Budau, J. Chevrier, F. Marchi, F. Comin, C. Alandi, F. Bertin, N. Buffet, C. Wyon, and P. Mur, *Imaging of stored charges in Si quantum dots by tapping and electrostatic force microscopy.* EPL (Europhysics Letters), 2002. **59**(4): p. 566.

202. Das, A., C. Lei, H.E. Thomas, M. Elliott, J.E. Macdonald, P. Glarvey, and M. Turner, *EFM phase investigation of the metal–organic film interface.* Applied Surface Science, 2006. **252**(15): p. 5477-5480.

203. Saive, R., M. Scherer, C. Mueller, D. Daume, J. Schinke, M. Kroeger, and W. Kowalsky, *Imaging the electric potential within organic solar cells.* Advanced Functional Materials, 2013. **23**(47): p. 5854-5860.

204. Lei, C., A. Das, M. Elliott, and J.E. Macdonald, *Quantitative electrostatic force microscopy-phase measurements.* Nanotechnology, 2004. **15**(5): p. 627.

205. Qi, G., H. Yan, L. Guan, Y. Yang, X. Qiu, C. Wang, Y. Li, and Y. Jiang, *Characteristic capacitance in an electric force microscope determined by using sample surface bias effect.* Journal of Applied Physics, 2008. **103**(11): p. 114311.

206. Qiu, X., G. Qi, Y. Yang, and C. Wang, *Electrostatic characteristics of nanostructures investigated using electric force microscopy.* Journal of Solid State Chemistry, 2008. **181**(7): p. 1670-1677.

207. Krayev, A. and R. Talroze, *Electric force microscopy of dielectric heterogeneous polymer blends.* Polymer, 2004. **45**(24): p. 8195-8200.

208. Gupta, S., O.A. Williams, and E. Bohannan, *Electrostatic force microscopy studies of boron-doped diamond films.* Journal of Materials Research, 2007. **22**(11): p. 3014-3028.

209. Castellano-Hernández, E., J. Moreno-Llorena, J. Sáenz, and G.M. Sacha, *Enhanced dielectric constant resolution of thin insulating films by electrostatic force microscopy.* Journal of Physics: Condensed Matter, 2012. **24**(15): p. 155303.

210. Lilliu, S., C. Maragliano, M. Hampton, M. Elliott, M. Stefancich, M. Chiesa, M. Dahlem, and J.E. MacDonald, *EFM data mapped into 2D images of tip-sample contact potential difference and capacitance second derivative.* Scientific Reports, 2013. **3**.

211. Cherniavskaya, O., L. Chen, V. Weng, L. Yuditsky, and L.E. Brus, *Quantitative noncontact electrostatic force imaging of nanocrystal polarizability.* The Journal of Physical Chemistry B, 2003. **107**(7): p. 1525-1531.

212. Li, Z.-Y., B.-Y. Gu, and G.-Z. Yang, *Scanning-electrostatic-force microscopy: Self-consistent method for mesoscopic surface structures.* Physical Review B, 1998. **57**(15): p. 9225.

213. Chavez-Pirson, A., O. Vatel, M. Tanimoto, H. Ando, H. Iwamura, and H. Kanbe, *Nanometer-scale imaging of potential profiles in optically excited n-i-p-i heterostructure using Kelvin probe force microscopy.* Applied Physics Letters, 1995. **67**(21): p. 3069-3071.

214. Gil, A., J. Colchero, J. Gómez-Herrero, and A. Baró, *Electrostatic force gradient signal: resolution enhancement in electrostatic force microscopy and improved Kelvin probe microscopy.* Nanotechnology, 2003. **14**(2): p. 332.

215. Lei, C., A. Das, M. Elliott, and J.E. Macdonald, *Conductivity of macromolecular networks measured by electrostatic force microscopy.* Applied Physics Letters, 2003. **83**(3): p. 482-484.

216. Jackson, J.D., *Classical electrodynamics*. 1999: Wiley.

217. Colchero, J., A. Gil, and A. Baró, *Resolution enhancement and improved data interpretation in electrostatic force microscopy.* Physical Review B, 2001. **64**(24): p. 245403.

218. Garcıa, R. and R. Perez, *Dynamic atomic force microscopy methods.* Surface Science Reports, 2002. **47**(6): p. 197-301.

219. Lilliu, S., *Organic Photodetectors Optimization and Nanoscale Investigation*. 2011, Cardiff University.

220. Hoppe, H., T. Glatzel, M. Niggemann, A. Hinsch, M.C. Lux-Steiner, and N. Sariciftci, *Kelvin probe force microscopy study on conjugated polymer/fullerene bulk heterojunction organic solar cells.* Nano Letters, 2005. **5**(2): p. 269-274.

221. Glatzel, T., S. Sadewasser, and M.C. Lux-Steiner, *Amplitude or frequency modulation-detection in Kelvin probe force microscopy.* Applied Surface Science, 2003. **210**(1): p. 84-89.

222. Jacobs, H., P. Leuchtmann, O. Homan, and A. Stemmer, *Resolution and contrast in Kelvin probe force microscopy.* Journal of Applied Physics, 1998. **84**(3): p. 1168-1173.

223. Sugimura, H., Y. Ishida, K. Hayashi, O. Takai, and N. Nakagiri, *Potential shielding by the surface water layer in Kelvin probe force microscopy.* Applied Physics Letters, 2002. **80**(8): p. 1459-1461.

224. Garcia-Martin, A. and R. Garcia, *Formation of nanoscale liquid menisci in electric fields.* Applied Physics Letters, 2006. **88**(12): p. 123115.

Veeco, MultiMode SPM Instruction Manual 2004,
http://msc.engr.wisc.edu/manuals/SPM/MltiMode.pdf