Morphological and electrical comparison of Ti and Ta based ohmic contacts for AlGaN/GaN-on-SiC HFETs

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Abstract

The morphology and impact on leakage currents of two different ohmic metal stacks for GaN based transistor devices is investigated in this work. The results have implications for the performance and reliability of a GaN transistor device. A low temperature Ta based and a higher temperature anneal Ti based metallization are compared. The low temperature process shows a smoother metal semiconductor interface together with several orders of magnitude lower vertical and lateral leakage compared to the conventional higher temperature process. In addition to the leakage tests, back bias ramping experiments are performed unveiling potential advantages of the conventional approach in mitigating current collapse. However the low leakage will enable higher voltage operation making the low temperature process the preferable choice for high power RF applications, if simultaneously current collapse can be controlled.

Introduction

The commonly used metal stacks on GaN HFET epitaxial material for ohmic contact formation are Ti/Al based stacks like Ti/Al/Ni/Au, which need to be annealed at high temperatures of 800°C and above [1]. Recently, Ta based approaches to develop alternative metallization schemes have succeeded in achieving very reasonable contact resistances while annealing temperatures were kept low (~600°C) resulting in a smoother contact surface besides other benefits [2]. The impact of a low temperature ohmic process in comparison to the conventional Ti based one on lateral leakage currents and breakdown of GaN based HFET structures has been investigated in [3] for an InAlN/GaN double hetero structure on semi-insulating Si substrate showing superior lateral leakage and breakdown.

In this work we compare high and low temperature annealed stacks and besides the lateral leakage we also investigate vertical leakage, which normally defines the overall breakdown performance [4]. Back bias ramping experiments were performed to provide information on charging effects in the buffer region [5].

Structure and Morphology details

The epitaxial layers consist of a single hetero structure AlGaN/GaN HFET, typical of that used for RF applications, grown on n-type conducting SiC with an AlN nucleation layer. Normally semi-insulating substrates are used for RF GaN-on-SiC, but here we use a conducting substrate to measure vertical currents and enable back biasing tests. Both metallizations have been processed on pieces of the same epi-wafer. Total thickness of the epitaxial layers is ~2µm. Before contact formation a SiN passivation layer has been deposited by low pressure chemical vapour deposition. The metal stacks used are Ta/Al/Ta and Ti/Al/Ni/Au with thicknesses of 10/280/20nm and 20/110/40/40nm respectively. Both metallizations were deposited after a recess-etch through the passivation and part way through the AlGaN barrier. The Ta stack was annealed in a nitrogen atmosphere for ~20min with a maximum temperature of 600°C. Whereas the Ti stack was annealed also in nitrogen for 30s at 830°C. Both metallizations showed ohmic behavior. The contact resistances measured are 0.4Ωmm for the Ta stack and 1.6Ωmm for the Ti stack.

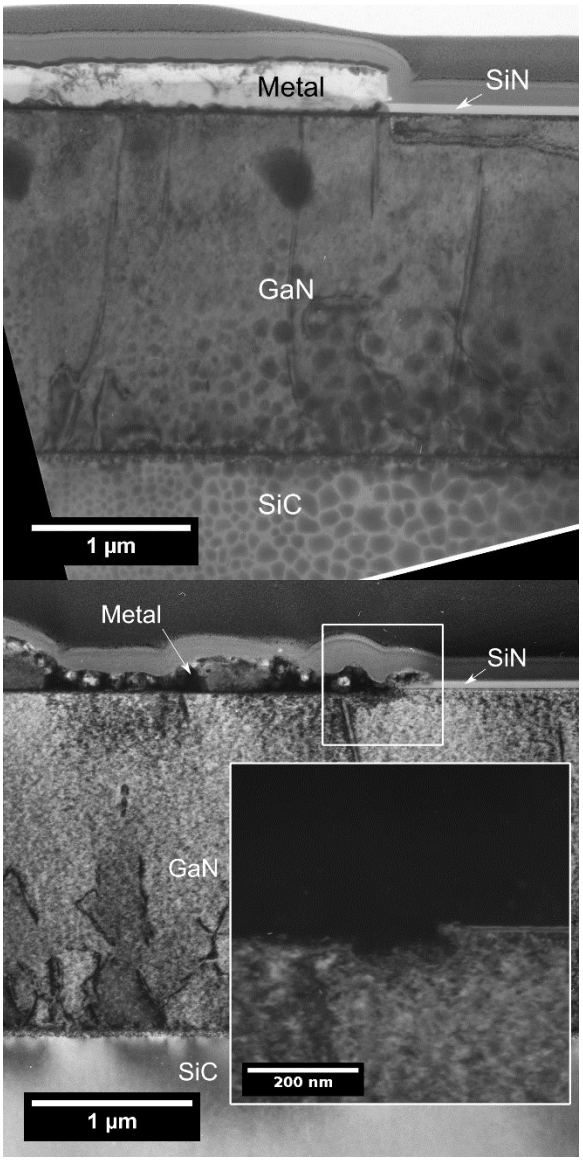


Fig. 1. TEM cross sections of Ta based ohmic (a) and Ti based ohmic (b). The inset in (b) shows a magnified dark field image of the highlighted region.

The contact surface roughness is 101nm and 268nm root mean square for Ta and Ti stack respectively measured on similar areas of about 500µm^2. The formation of TiN protrusions that penetrate the upper epitaxial layers has been reported to occur during the annealing of the Ti contact [1] and is likely to cause localized low resistivity paths. In Fig. 1 TEM cross-section images of both metal stacks are depicted. The inset of Fig. 1b shows a dark area within the epitaxial part is visible in a dark field image. Similar findings in [1] have been identified as TiN. In contrast no such area was observed for the Ta sample shown in Fig. 1b.

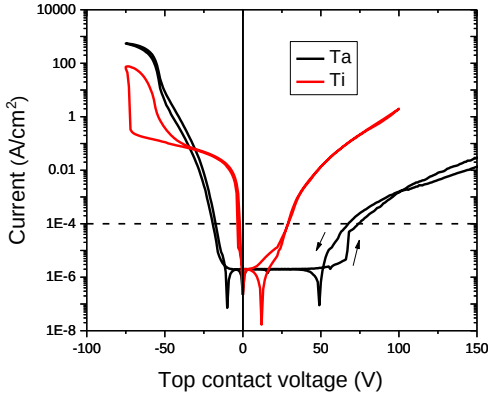
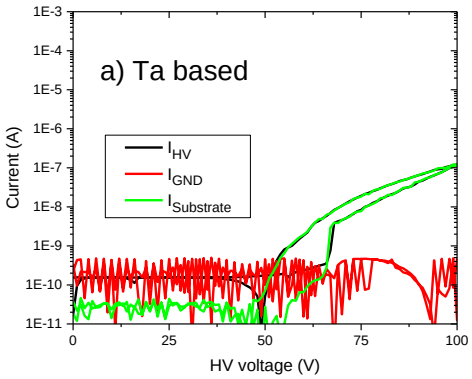


Fig. 2. Absolute vertical currents. Both polarities. Substrate grounded. The dashed line indicates 0.1mA/cm^2 current density for the rectangular contact of 100µm x 70µm size on a 104µm x 74µm mesa.

Electrical characterization

Fig. 2 shows the vertical currents measured for the different contact metallizations when biased with the substrate grounded. Asymmetric behavior is observed in response to either positive or negative bias, related to effects at the 2DEG buffer interface. With a negative voltage on the top contact 2DEG electrons are injected into the buffer structure causing the difference in the onset of leakage. At positive voltages corresponding to typical device operation the vertical currents are generally lower than for negative voltages, but also a huge difference between the two contacts of about three orders of magnitude can be seen. The high temperature process obviously leads to much stronger vertical leakage. The high leakage of the Ti contact is likely to be associated with the TiN protrusions and the rougher metal semiconductor interface compared to the much smoother Ta metal stack. Under the commonly applied failure criterion of <0.1mA/cm^2 the Ta sample can operate at up to 75V before the limit is reached compared to about 25V for the Ti sample as can be seen in Fig. 2.



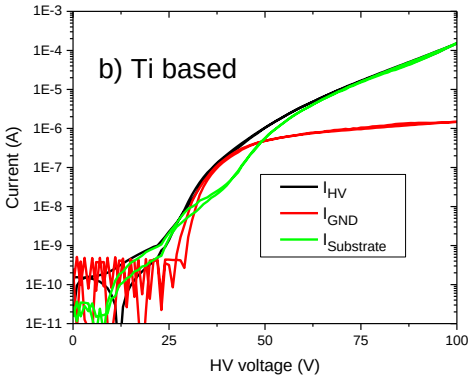


Fig. 3. Absolute vertical and lateral leakage for Ta (a) and Ti (b) based contacts. Both were probed on mesa isolated contacts of 100µm x 70µm area with 50µm distance between the 100µm edges.

In Fig. 3a the currents of a three terminal measurement are shown for the Ta based ohmic. Fig. 4 describes the measurement setup. Two contacts isolated by a mesa etch are used. One contact is biased while substrate and the other contact are grounded with currents recorded at all terminals. For the Ta sample the lateral leakage current measured at the grounded top contact did not exceed 1nA with all current flowing vertically between biased contact and substrate. In contrast, the Ti contact sample shown in Fig. 3b shows a significant lateral contribution to the leakage, apparent in the much higher current at the grounded top contact. Fig. 5 gives a closer look at the voltage regime between 25V and 60V on a linear current scale. Up to ~47V lateral current between the top contacts is dominating the leakage in the Ti contact sample. Similar leakage currents have been observed on another piece of the same wafer processed in a different lab also with a Ti based ohmic stack (results not shown here). In contrast to the conventional Ti metallization the Ta based ohmic completely suppresses lateral leakage that can hamper device performance.

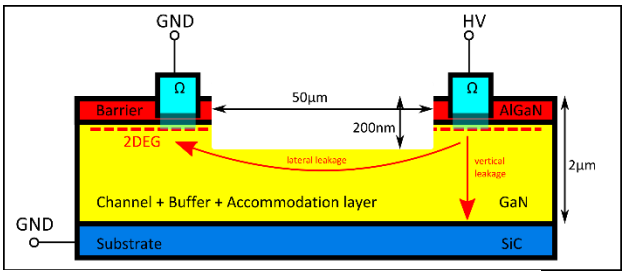


Fig. 4. Experimental setup.

The experiments also demonstrate a significant reduction in vertical currents with the low temperature contacts. The reduced lateral leakage as reported in [3] has been confirmed for the AlGaN/GaN on SiC structure.

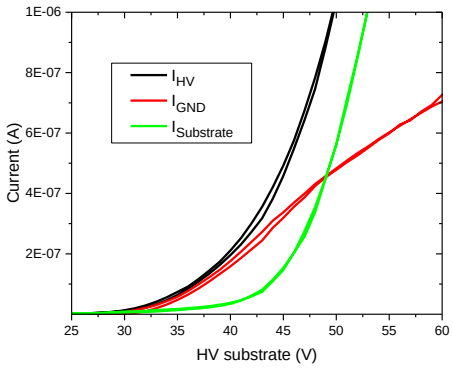


Fig. 5. Close up of leakage currents of Ti contacts on a linear scale showing the lateral leakage exceeding vertical leakage for up to 47V bias.

Back bias ramp results for both metallizations are shown in Fig. 6. Detailed information on the technique can be found in [6,7]. Essentially two ohmic contacts, not isolated from each other, are used to impose a 2DEG current by applying a small voltage between them. The change in this current is then monitored during a substrate bias ramp to reveal information on the charges in the buffer region. The black curve in Fig. 6 is representative for the Ta based ohmics where the results are very consistent between test structures distributed across the sample of 1cm^2 total area. In contrast, different devices on the Ti based ohmic sample showed very different

responses to the back bias. The red curves in Fig. 5 give the largest and smallest current collapse observed with Ti based ohmics. The current collapse is defined as the loss in current after returning to zero applied substrate bias. The Ta devices show a current collapse of ~20%, whereas in the Ti devices the current collapse varies between 10 and 20%. The reduced current collapse in some Ti devices can be explained by the presence of a leakage path between 2DEG and buffer in these devices enabling neutralization of trapped buffer charges [8]. The leakage associated with the Ti based ohmic can in some circumstances have a positive effect on the current collapse.

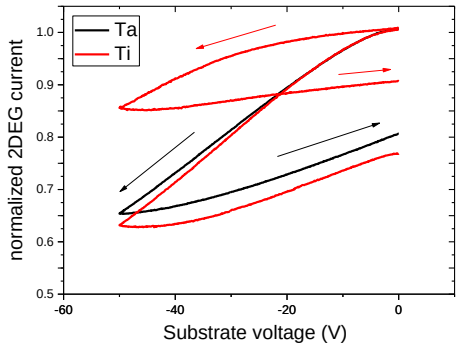


Fig. 6. Back bias ramps measured on simple TLM structures with a 50µm gap and 100µm width. The red curves represent strongest and least measured current collapse on the Ti sample. Ramp rate: 0.5V/s.

Conclusion

Low and high anneal temperature ohmic metal processes for GaN based transistors have been tested for buffer leakage. The results, for both vertical and lateral leakage, suggest great improvements in maximum achievable voltage in a typical RF structure using the low temperature process. Higher power at high frequencies will be achievable with such a contact compared to the conventional process assuming that RF performance is not affected by potentially increased buffer related current collapse. Similar effects are expected for GaN-on-Si power devices, but remain to be tested.

Acknowledgments

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